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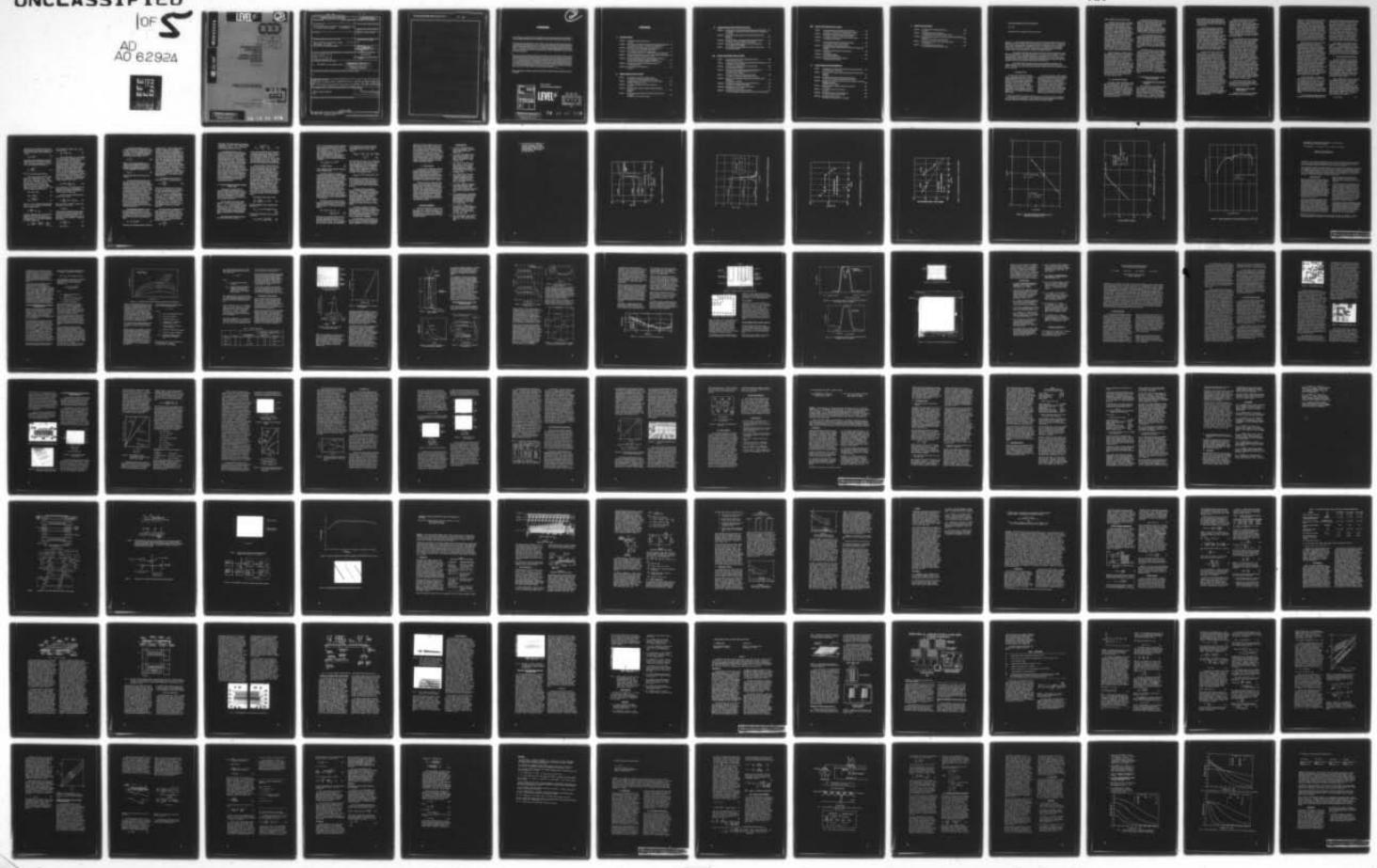
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29-31 October

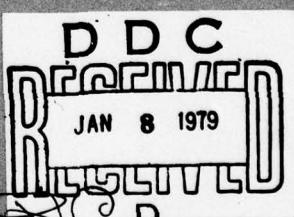
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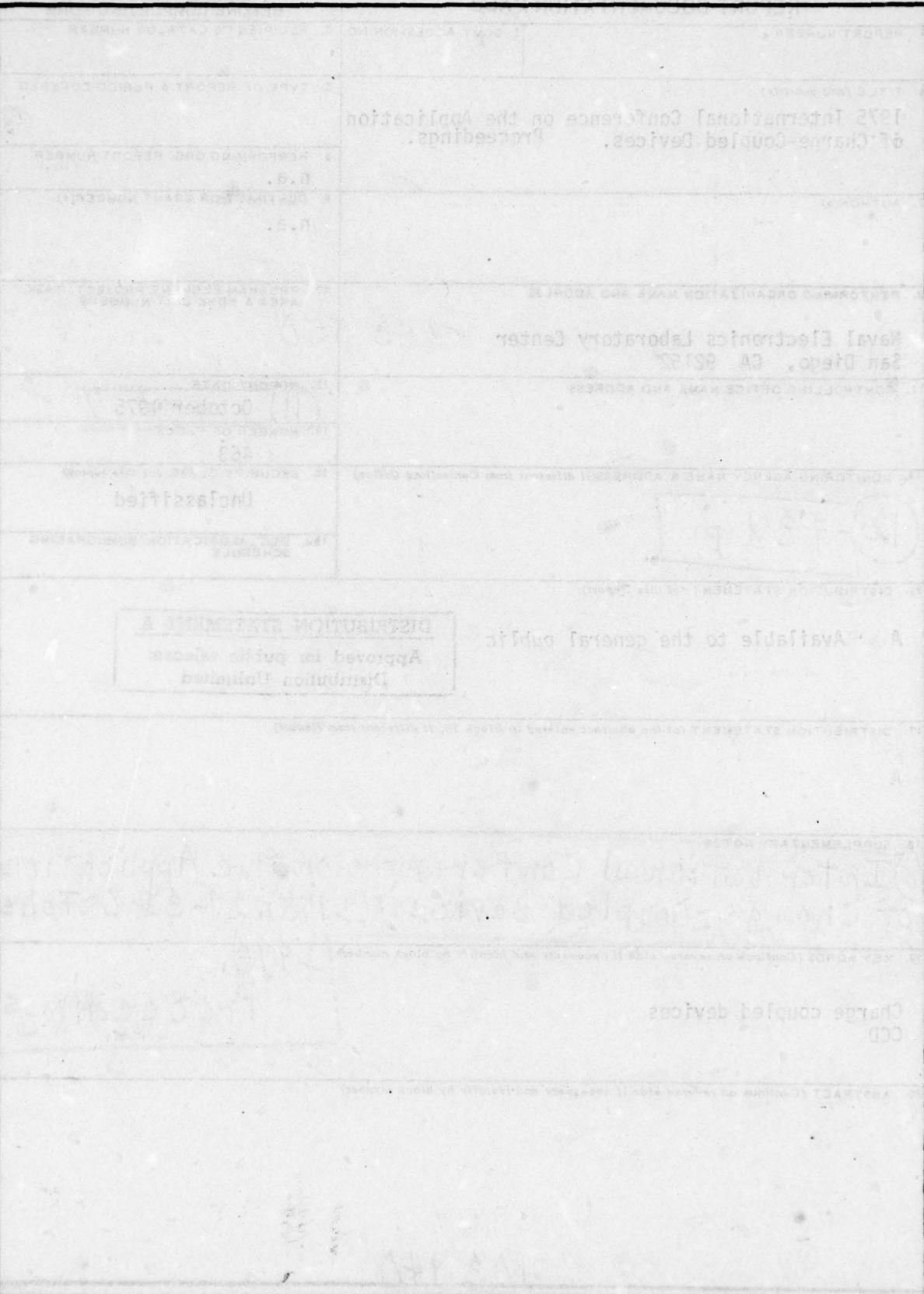
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FOREWORD

The 1975 Charge-Coupled Device (CCD) Applications Conference marks the third such event entirely devoted to presentation of ideas, problems and solutions in this new phase of the semiconductor technology.

Pursuing the guidelines established at the first Conference which was held in 1973 at the Naval Electronics Laboratory Center, San Diego, California, this Conference aims to reflect the impact of device concept in design for improved performance and lower cost of present and future systems. Technology has been extended to a high level of sophistication in the move from the laboratory demonstration to varied applications, such as development of focal plane infrared (IR) arrays, analog and digital signal processors, imagers and memory components.

This year the technical presentations reflect the fact that there is more to CCD than the television camera. There are five main sessions including a double session on signal processors. The assortment of areas illustrates the wide technical scope of CCD development at this period of time. Each session is structured around one or two invited papers which are followed by the contribution papers. The invited papers describe the device technological approach and its characteristics and in general the contributed papers state current system limitations and demonstrate how the inclusion of a CCD device results in an enhanced overall performance. The "Characterization" session has been included to cover specific topics common to various application areas such as radiation effects or techniques for signal linearization.

Special appreciation is expressed to members of the Program Committee for their contributions to produce this program.

ISAAC LAGNADO

CCD '75 Conference Chairman

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CONTENTS

I. IR APPLICATIONS

PAPER I	— InSb MIS Technology and CID Devices	1
	J. C. Kim	
PAPER II	— Extrinsic Silicon Monolithic Focal Plane Array Technology and Applications	19
	K. Nummedal, J. C. Fraser, S. C. Su, R. Baron, and R. M. Finnila	
PAPER III	— InSb CCDs and Other MIS Devices for Infrared Applications	31
	R. D. Thom, R. E. Eck, J. D. Phillips, and J. B. Scors	
PAPER IV	— A CCD Multiplexer With Forty AC Coupled Inputs	43
	S. P. Emmons, T. F. Cheek, Jr., J. T. Hall, P. W. Van Atta, and R. Balcerak	
PAPER V	— Integrated CCD-Bipolar Structure for Focal Plane Processing of IR Signals	53
	W. Grant, R. Balcerak, P. Van Atta, and J. T. Hall	
PAPER VI	— Infrared Imaging With Monolithic, CCD-Addressed Schottky-Barrier Detector Arrays: Theoretical and Experimental Results	59
	E. S. Kohn, S. A. Roosild, F. D. Shepherd, Jr., and A. C. Yang	
PAPER VII	— Series-Parallel Scan IR CID Focal Plane Array Concept	71
	A. F. Milton and M. Hess	
PAPER VIII	— Injection Efficiency in Hybrid IRCCD's	85
	A. J. Steckl	

II. VISIBLE IMAGING APPLICATIONS

PAPER I	— CID Imaging—Present Status and Opportunities	93
	G. J. Michon, H. K. Burke, D. M. Brown, and M. Ghezzo	
PAPER II	— A High Performance 190 x 244 CCD Area Image Sensor Array	101
	W. Steffe, L. Walsh, and C. K. Kim	
PAPER III	— Low Light Level Performance of CCD Image Sensors	109
	D. D. Wen	
PAPER IV	— Parametric System Analysis in Charge Coupled Device Imaging Applications	121
	R. Wight	
PAPER V	— Performance Analysis of EBS-CCD Imaging Tubes/Status of ICCD Development	133
	J. B. Barton, J. J. Cuny, and D. R. Collins	

II. VISIBLE IMAGING APPLICATIONS (Continued)

- PAPER VI — Development of a 400 x 400 Element, Backside Illuminated CCD Imager 147
G. A. Antcliffe, L. J. Horbeck, W. C. Rhines, W. W. Chan, J. W. Walker, and
D. R. Collins
- PAPER VII — An Intensified Charge Coupled Device for Extremely Low Light Level
Operation 155
D. G. Currie
- PAPER VIII — CCD Dynamically Focussed Lenses for Ultrasonic Imaging Systems 165
R. D. Melen, J. D. Shott, J. T. Walker, and J. D. Meindl
- PAPER IX — CCD-TV Cameras Utilizing Interline-Transfer Area Image Sensors 173
K. A. Hoagland and H. L. Balopole
- PAPER X — Diverse Electronic Imaging Applications for CCD Line Image Sensors 181
J. Hunt and H. Sadowski

III.A. SIGNAL PROCESSING APPLICATIONS

- PAPER I — Charge Coupled Device (CCD) Analog Signal Processing 189
M. H. White and D. R. Lampe
- PAPER II — Applying the Concept of a Digital Charge Coupled Device Arithmetic Unit . 199
C. S. Miller and T. A. Zimmerman
- PAPER III — Signal Processing Capabilities of a 100 x 100 CCD Array 209
S. P. Buchanan and R. R. Clark
- PAPER IV — The Use of Charge Coupled Devices in Electrooptical Processing 217
M. A. Monahan, R. P. Bocker, K. Bromley, A. C. H. Louie,
R. D. Martin, and R. G. Shepard
- PAPER V — Analogue Correlators Using Charge Coupled Devices 229
J. G. Harp, G. F. Vanstone, D. J. MacLennan, and J. Mavor
- PAPER VI — Discrete-Time Analog Signal Processing Devices Employing a Parallel
Architecture 237
R. R. Buss and G. P. Weckler
- PAPER VII — Multiple Filter Characteristics Using a Single CCD Structure 245
A. A. Ibrahim, G. J. Hupe, and L. P. Sellars
- PAPER VIII — Applications of a CCD Low-Pass Transversal Filter 251
R. D. Baertsch and J. J. Tiemann
- PAPER IX — Sampled Analog CCD Recursive Comb Filters 257
T. F. Tao, V. Iamsaad, S. Holmes, B. Freund, L. Saetre, and T. A. Zimmerman

III.B. SIGNAL PROCESSING APPLICATIONS

PAPER I	— Comparison Between the CCD CZT and the Digital FFT	267
	D. D. Buss, R. L. Veenkant, R. W. Brodersen, and C. R. Hewes	
PAPER II	— Radar Video Processing Using the CCD Chirp Z Transform	283
	W. H. Bailey, D. D. Buss, L. R. Hite, and M. W. Whatley	
PAPER III	— Linearisation of the Charge Coupled Device Transfer Function	291
	D. J. MacLennan and J. Mavor	
PAPER IV	— A CCD-SAW Processor for Pulse Doppler Radar Signals	295
	J. B. G. Roberts, R. Eames, and R. F. Simons	
PAPER V	— CCD Applications to Synthetic Aperture Radar	301
	W. Bailey, W. Eversole, J. Holmes, W. Arens, W. Hoover, J. McGhee, and R. Ridings	
PAPER VI	— A Self Contained 800 Stage CCD Transversal Filter	309
	C. R. Hewes	
PAPER VII	— A Swept Delay Correlator	319
	J. B. G. Roberts and R. Eames	
PAPER VIII	— A Time Domain Analysis of Video Integrators	323
	A. Chowaniec and G. S. Hobson	

IV. CHARACTERIZATION MEASUREMENTS

PAPER I	— The Measurement of Noise in Buried Channel Charge Coupled Devices	331
	R. W. Brodersen and S. P. Emmons	
PAPER II	— Noise Linearity and Trapped Charge Measurements with Charge Sensitive Amplifiers	351
	K. Kandiah	
PAPER III	— Anti-Aliasing Characteristics of the Floating Diffusion Input	361
	S. P. Emmons, D. D. Buss, R. W. Brodersen, and C. R. Hewes	
PAPER IV	— Limitations of a Threshold-Insensitive CCD Input Technique in a Total Dose Radiation Environment	369
	J. M. Killiany and W. D. Baker	
PAPER V	— Radiation Hardness of Surface and Buried Channel CCDs	375
	G. A. Hartsell	
PAPER VI	— Low Temperature Silicon CCD Operation	383
	A. J. Steckl	
PAPER VII	— Extremely High Speed CCD Analog Delay Line	389
	Y. T. Chan, B. T. French, and P. E. Green	
PAPER VIII	— High Speed Operation of CCD's	399
	D. A. Gradi, R. A. Groenwald, and T. J. Flanagan	

V. MEMORY APPLICATIONS

PAPER I — A CCD Memory for Radar Signal Processing	413
R. A. Belt	
PAPER II — A 16 Kilobit High Density CCD Memory	423
S. D. Rosenbaum, J. T. Caves, S. Poon, and C. H. Chan	
PAPER III — A Fast Access Bulk Memory System Using CCD's/A Recorder Buffer Memory Using CCD's	429
K. Siemens, C. R. Robinson, and J. Mastronardi	
PAPER IV — Cost Performance Aspects of CCD Fast Auxiliary Memory	435
D. P. Bhandarkar	
PAPER V — A CCD-Based Transient Data Recorder	443
T. E. Linnenbrink, M. J. Monahan, and J. L. Rea	

InSb MIS TECHNOLOGY AND CID DEVICES *

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Abstract: A metal-insulator-InSb (MIS) technology has been successfully developed; and MIS structures with excellent interface properties can be fabricated. The C-V characteristics of these structures show a completely inverted low-frequency type C-V response at about 10 Hz, an indication of low thermal generation. An analysis of the conductance measurements in the strong inversion region indicates that bulk generation dominates minority carrier thermal generation, leading to good MIS structures.

Conductance techniques were utilized to study the interface properties of these MIS structures leading to a detailed description of the surface state properties. The interface state density of our recent MIS structures is in the range of $10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$. It appears that the surface states are continuously distributed over the entire InSb bandgap. The experimental results strongly indicate that the InSb MIS interface characteristics are adequately described by the Shockley-Read-Hall treatment model.

These InSb MIS structures have been used as IR sensors operating in the charge injection mode. Their sensitivities approach background-limited performance (BLIP). InSb CID arrays have been fabricated and the results of these array measurements will be discussed.

I. INTRODUCTION

In recent years solid-state imaging devices operating on the basis of a surface charge-coupling principle in the silicon MOS structure have received considerable attention, and considerable progress has been made in both line and large-area imaging devices, with the silicon MOS technology. These devices are used in the visible region of the spectrum. For IR applications a similar approach has been applied to narrow-bandgap semiconductors, namely InSb.

The success of silicon charge-coupled devices is undoubtedly due to the advanced development of the silicon MOS technology, but a suitable dielectric technology for other semiconductors has not yet been fully developed. Most device development work on III-V compound semiconductor has been concerned with p-n junction fabrication and as a result, excellent InSb infrared photovoltaic detectors have been developed. For surface passivation of InSb p-n junction detectors, an anodic

*The early work of this program was supported by the Air Force Avionic Laboratory and Army Night Vision Laboratory. More recent work is being supported by the Naval Research Laboratory and Defense Advanced Research Projects Agency.

oxide of InSb has been commonly used.

A detailed study of anodic oxide InSb MOS structures (1) conducted in our laboratory indicates that majority carrier trapping in the oxide causes the surface state charges. For n-type InSb substrates the majority carrier electrons play the major role in charge trapping in the oxide, resulting in a negative surface state charge. On the other hand, for p-type materials, hole trapping is the dominant mechanism and results in positive surface charges. Both the indium and antimony atoms in anodized InSb oxide, therefore, may be responsible for charge trapping both types of carriers. This variable charge-trapping mechanism leads to an instability of the MOS structure and it is, thus, difficult to use the anodic oxide in MOS devices for stable surface charge-coupling operations.

It was, therefore, necessary that a new dielectric material and a suitable deposition technology be found, if successful InSb MIS surface charge-coupled devices were to be developed. As a result of our recent R&D efforts in this regard, we have found that a dielectric layer of silicon oxynitride (SiON) deposited pyrolytically on an InSb substrate, yields MIS interface properties (2) that allow us to operate the MIS structures as charge injection devices (CID) in the charge storage mode. This paper describes the interface properties of SiON-InSb MIS structure and the experimental results obtained using these structures in the charge injection mode.

II. InSb MIS STRUCTURES

The single crystals of InSb used in this work were grown by the Czochralski method with a (111) orientation. For n-type materials tellurium was used as the dopant with a carrier concentration ranging from $10^{13}/\text{cm}^3$ to $10^{16}/\text{cm}^3$; for p-type materials cadmium was the dopant at concentrations in the range of $10^{15}/\text{cm}^3$. The dislocation densities (EPD/cm^2) of these materials were less than $100/\text{cm}^2$.

The large ingots of InSb were cut into wafers about 35 mils thick and 2-4 cm in diameter. After the B face (Sb side) of the wafer was mechanically polished and chemically etched, SiON layers were deposited pyrolytically on the InSb surface. A typical oxide thickness is in the range of 1000\AA to 2000\AA . The SiON dielectric layer is extremely uniform and pin-hole free.

For a simple InSb MIS structure, a semi-transparent NiCr metal film less than 100\AA thick and 20 mils in diameter was vacuum deposited on the SiON layer of InSb wafer. The large wafer was diced into small chips which were, in turn, attached to transistor headers. The device header was mounted in a cryogenic dewar for evaluation.

The MIS structures were measured using a lock-in amplifier or phase-sensitive detection technique. The lock-in amplifier (PAR 124) can be used over a wide range of frequencies and is particularly useful at low frequencies. This admittance bridge permits us to easily measure not only C-V curves but also conductance-voltage characteristics of MIS structure. The conductance of the device can easily be measured by changing the phase angle of the instrument by 90° . The conductance technique was used exclusively to study the interface properties of the structures. All measurements were made at near 77°K , unless otherwise stated.

III. INTERFACE PROPERTIES OF InSb MIS STRUCTURES

1. C-V Characteristics of InSb MIS Structure

The capacitances of the MIS structures were measured as a function of the gate bias voltage at various frequencies, as shown in Figure 1 for an n-type substrate. These measurements were made in the dark condition; that is, the field of view (FOV) was equal to zero. The device could "see" only its own temperature so that no 300°K

photon radiation could have contributed to the minority carrier equilibration process. In this way only the thermal generation process of minority carriers in the device can be determined.

The C-V curves closely follow the simple ideal MIS capacitance model (3). At the positive gate bias the capacitance is approximately that of the insulator; and when the gate is biased negatively, the capacitance is decreased due to the creation of a depletion region on the InSb surface. Further increases in the negative bias cause a strong inversion where the depletion width is fixed, resulting in a minimum capacitance, shown in the high-frequency measurement. Note that the dashed line is a computer-calculated, theoretical C-V curve that follows closely the experimental result, indicating a low surface state density.

To operate this type of device as an optical sensor, e.g. CID and CCD, the strong inversion bias region is important, since the device operates normally here. As the MIS capacitor is biased into the heavy inversion region, it can be shown (4) that the MIS structure results in a simple equivalent circuit; the insulator capacitance (C_0) is in series with the parallel combination of the depletion capacitance (C_D) and a resistor (for the sake of simplicity, we use a conductance, G_g). This simple equivalent circuit can be derived only if the surface state density is relatively small, so that it can be assumed that the surface state capacitance is much smaller than the depletion capacitance. For single-level types of surface states, only those states located near the intrinsic Fermi level contribute significantly to the surface state capacitance, when the Fermi level is near this level; but at the surface of the strong inversion bias the Fermi level is near the top of the valence band (for n-type devices). Therefore, with a relatively low surface state density, the above assumptions are quite valid. Later, it will be shown quantitatively that these assumptions can be applied to our InSb MIS devices.

It has been shown that (5) the change in capacitance in the strong inversion region is due to the relative value of G_g compared to ωC_D . The inversion capacitance changes from the minimum capacitance, $C_0 C_D / (C_0 + C_D)$, to the maximum insulator capacitance, C_0 , as the measurement frequency varies from very high to very low values. Between these two limits the inversion capacitance is a function of frequency and increases with decreasing frequency, as shown in Figure 1.

It has been shown that the capacitance in the strong inversion bias region depends on the relative value of the conductance, G_g . It will be shown later that G_g can be related directly to the thermally generated minority carrier current. If the relaxation rate of the minority carriers is very small in the device, G_g is, indeed, very small and the capacitance results in the high frequency case. This is the case when the minority carrier generation rate cannot keep up with the small signal variation of the capacitance measurement, resulting in a high-frequency type C-V response (equivalent to $\omega C_D \gg G_g$). If, however, the minority carriers can follow the variation in the measurement signal the capacitance rises, approaching the insulator capacitance; this is the low-frequency type of C-V curve, in which case $\omega C_D \ll G_g$. Therefore, the low-frequency C-V data reveal, qualitatively, the minority carrier relaxation rate. The frequency at which the minority carriers completely follow the measurement signal variation is in the range of 10 Hz, indicating that the minority carrier relaxation rate in these devices is, indeed, small.

The interface state density of these MIS devices has been determined quantitatively and it will be shown that the surface state densities are also small.

2. Surface State Density of InSb MIS Structures

Typical conductance (G_m/ω)-voltage characteristics of an n-type InSb MIS

structure at various frequencies are shown in Figure 2. The rise in conductance in certain bias regions is due to the capture and emission process of carriers by the interface states. The sharp single conductance peak is typical of single-level states. If we, therefore, analyze the conductance values in the peak region (6), we can determine the interface state parameters. Since the conductance is caused by the steady-state loss due to the capture and emission of carriers by interface states, this technique is a more direct measure of the interface properties than the use of C-V data.

The conductance technique used here has been described in some detail in reference 2; it provides quite accurate determinations of surface state densities. At each bias point in the peak conductance region, equivalent parallel conductance values were computed from the measured conductance data as a function of frequency. From these conductance curves, then, the surface state densities were obtained for different bias points. The results are shown in Figure 3; the values of surface state density were plotted as a function of surface potential. The circle-dot points represent the values determined by the continuum model, whereas the triangle points were obtained from the single time constant model. It is interesting to point out that, in the depletion region, the experimental points follow the continuum model, whereas, in the weak inversion region, the measured data fit the single time constant model.

As shown in Figure 3, the surface state density varies from mid- 10^{10} cm $^{-2}$ eV $^{-1}$ to about mid- 10^{11} cm $^{-2}$ eV $^{-1}$. It is also interesting to note that the interface state density tends to become a minimum near the flatband, which is somewhat different from the silicon case. (6) This result is also evident from the C-V curves shown in Figure 1, where the surface state density in the flatband region appears to be lowest.

The corresponding surface state time constant values were also determined from

the equivalent parallel conductance data and measured as a function of the surface potential, as shown in Figure 4. Here, again, the separate data points represent the two models, as indicated. In both cases the time constant varies exponentially with the surface potential, but with different slopes; for the continuum model the slope is $\beta/2$, and for the single time constant case, it is $\beta/4$, where β is q/kT ; q is the electronic charge, k is Boltzman's constant, and T is the absolute temperature. The extrapolation of the two lines, however, meets at about the same point in the flatband voltage.

If the capture cross-section is independent of energy then the slope should be equal to β . A slope smaller than β may be due to the fact that the capture cross-section is energy dependent. For the single time constant data, an even slower increase in the time constant may be due to an additional contribution of minority carrier generation.

3. Thermal Generation Mechanism

As shown in Figure 2, in the strong inversion bias region the measured conductance becomes constant and independent of bias, but is a function of the measurement frequency, as in the case of the C-V data. It has been shown that the capacitance variation with frequency in the strong inversion bias region depends on the relative value of G_g with respect to ωC_D . Similarly, the bias-independent conductance values can be used to determine the thermal generation mechanism of these devices.

When an MIS structure with a relatively low interface state density is biased into a strong inversion region, a simple equivalent circuit (4) of the capacitor can be derived; the insulator capacitance (C_0) is in series with the parallel combination of the depletion capacitance (C_D) and a conductance, G_g . For the admittance measurements, the MIS structure is applied with a dc bias, V_g , and a small ac signal, $\Delta V(t)$. The total charge density, Q , is given by

$$Q = Q_p + Q_{sc} \quad (1)$$

where Q_p is the minority carrier charge density in the inversion layer and Q_{sc} is the semiconductor space-charge density. Q_{sc} is then

$$Q_{sc} = qN_D x . \quad (2)$$

where N_D is the concentration of the donor impurities and x is the surface depletion depth. The surface potential, ϕ_s , derived from the depletion approximation, is

$$\phi_s = \frac{qN_D x^2}{2\epsilon} , \quad (3)$$

where ϵ is the permittivity of InSb.

The time variation of the above quantities can be defined as $Q(t) = Q_0 + \Delta Q$, $Q_p(t) = Q_{po} + \Delta Q_p$, $Q_{sc}(t) = Q_{so} + \Delta Q_{sc}$, $x(t) = x_0 + \Delta x$, and $\phi_s(t) = \phi_{so} + \Delta \phi_s$, where Q_0 , Q_{po} , Q_{so} , x_0 , and ϕ_{so} are all established by the bias, and ΔQ , ΔQ_p , ΔQ_{sc} , Δx , and $\Delta \phi_s$ are caused by the ac signal and thus are a function of time. Thus, the time dependent quantities are,

$$\Delta Q = \Delta Q_p + \Delta Q_{sc} \quad (4)$$

$$\Delta Q_{sc} = qN_D \Delta x \quad (5)$$

$$\Delta \phi_s = \frac{qN_D x_0 \Delta x}{\epsilon} \quad (6)$$

since $x_0 \gg \Delta x$. The total ac current density, J , can be obtained by differentiating ΔQ with respect to time:

$$J = \frac{d\Delta Q}{dt} = J_p + J_{sc} , \quad (7)$$

where $J_p = d\Delta Q_p/dt$, the ac current density charging the inversion layer and $J_{sc} = d\Delta Q_{sc}/dt$, the ac current density charging the depletion layer. J_{sc} can be related to the surface potential by

$$J_{sc} = \frac{d\Delta Q_{sc}}{dt} = \frac{qN_D d\Delta x}{dt} = \frac{qN_D \Delta x}{x_0 dt} = \frac{d\Delta \phi_s}{x_0 dt} \quad (8)$$

For a sinusoidal ac signal, $\Delta \phi_s = A \exp(j\omega t)$ and, thus,

$$J_{sc} = j\omega \frac{\epsilon}{x_0} \Delta \phi_s . \quad (9)$$

The current density, J_p , that charges the inversion layer, should be equal to the ac current density of minority carrier generation. In general, the minority carrier generation can be divided into three separate generation currents, the surface generation current, the diffusion current outside the space-charge region and the generation current in the space-charge region. For an InSb MIS device operating at 77°K, the space-charge generation current dominates, as verified later. Assuming that the generation rate in the depletion layer, g , is constant over the space-charge region, the ac generation current density is equal to $qg\Delta x$ (7) and, thus,

$$J_p = qg\Delta x = \frac{\epsilon g}{N_D x_0} \Delta \phi_s , \quad (10)$$

from equation (6). It is interesting to note that the ac generation current density depends on x_0 , which is established by the dc bias surface potential, ϕ_{so} .

The total ac current density given in equation (7) is simply

$$J = \frac{\epsilon g}{N_D x_0} \Delta \phi_s + j\omega \frac{\epsilon}{x_0} \Delta \phi_s \quad (11)$$

thus, the total ac current ($I = JA_d$) in the structure of area = A_d is

$$I = Y_{in} \Delta \phi_s , \quad (12)$$

where Y_{in} is the admittance of the heavily inverted MIS (on the semiconductor side). Therefore, the equivalent circuit of the structure includes a conductance, G_g , and capacitance, C_D , in parallel. The G_g and C_D are then:

$$G_g = \frac{\epsilon g}{N_D x_0} A_d \quad (13)$$

$$C_D = \frac{\epsilon}{x_0} A_d . \quad (14)$$

Note that the conductance, G_g , is directly proportional to the generation rate, g , which, in the space-charge region where both types of carrier densities are small compared to n_i , is directly proportional to the intrinsic carrier density, n_i .⁽⁷⁾

$$g \approx \frac{n_i}{\tau}, \quad (15)$$

where τ is the carrier lifetime, it is assumed that the generation centers are located near the intrinsic Fermi level; therefore, G_g should be proportional to n_i in view of Equations (13) and (15), so,

$$G_g \propto n_i. \quad (16)$$

There is experimental evidence for this relation.

For the measurement of G_g the conductance values can be obtained by measuring the terminal conductance of the MIS structure at a fixed bias in the strong region as a function of frequency. Typical measurements are shown in reference (5). Thus, the G_g values are determined by this method as a function of temperature. Figure 5 shows the thermally generated conductance, G_g , as a function of the reciprocal of the absolute temperature; the experimental results yield a straight line on a semi-log plot. The slight departure from a straight line in the low temperature region is due to the noise of the measuring instrument since, in this region, the measurement frequencies used to determine G_g are quite low (less than 100 Hz).

The exponential dependence of G_g on the reciprocal temperature does ensure that the generation mechanism is thermal in nature. Furthermore, from the slope of the straight line, one can see that G_g indeed follows the n_i variation with temperature since

$$n_i \propto \exp(-E_g/2kT), \quad (17)$$

where E_g is the bandgap energy for InSb and

equal to 0.23 ev. The activation energy is correctly equal to $E_g/2$, as shown in Figure 5. Therefore, the dependence of the thermally generated conductance, G_g , on the intrinsic carrier concentration, n_i , indicates that G_g is dominated by generation in the space-charge region of the MIS structure, verifying our earlier assumption. The other generated components are, indeed, smaller than that of the space-charge generation. This means that the minority carrier generation, due to surface state density, does not contribute to the generation mechanism. Therefore, for the inverted InSb MIS structure minority carrier thermal generation is dominated by space-charge generation, which is a bulk generation process, thus leading to good MIS structures.

From Equations (13) and (14), the generation rate, g , is simply given by,

$$g = \frac{G_g N_D}{C_D}, \quad (18)$$

which can be calculated from the experimentally determined values of G_g and C_D . For an n-type InSb MIS structure ($N_D \approx 2 \times 10^{15} \text{ cm}^{-3}$, $C_0 = 72 \text{ pF}$ and $C_{\min} = 37 \text{ pF}$), for example, the depletion capacitance, C_D , and the thermally generated conductance, G_g , are equal to 76 pF and $3.2 \times 10^{-8} \text{ mhos}$, respectively, for a 20-mil diameter device. From these values, the lifetime (τ) can be computed to be approximately equal to 10^{-8} sec , which is well within the range of the reported values (8).

The dark current I_d , generated in the depletion region for the above device is, then, approximately equal to 10^{-8} A and when operated in the charge storage mode, this dark current limits the device's ultimate storage time. The dark current storage time, T_s , can then be related to the dark current (9) as,

$$T_s \approx \frac{C_0 \Delta V}{I_d g}, \quad (19)$$

where ΔV is the voltage swing from inversion to depletion. For $\Delta V = 10$ V, the dark current storage time is about 0.1 sec. This result is also evident from the C-V data.

It is significant that T_s , here, is roughly seven orders of magnitude greater than the carrier lifetime for InSb MIS devices, which is why the charge storage InSb MIS structure is so attractive as a charge integrating device, even though the carrier lifetime is short. Furthermore, for InSb devices operating in the IR region, the background photon flux that the device sees also generates additional current, which, then, causes a decrease in storage time. Our results (1, 5) indicate that the dark current of these structures is relatively small compared to that generated by the typical background photon flux encountered in the operation. Under this condition the dark current appears to be less important and the background photon-generated current should then determine the device operating storage time.

IV. InSb CID OPERATION USING THE MIS STRUCTURES

The physics of charge injection devices (CID) has been described in some detail (1), and the charge injection mode of operation of InSb MIS structures has been successfully demonstrated. We present here some of the optical measurements obtained on InSb CID devices.

For the signal-to-noise ratio measurements, we used a narrow band spike filter; $\lambda_0 = 4.5 \mu$, peak transmission = 41%, and $\Delta\lambda = 0.2 \mu$. The input signal radiation through the filter from a blackbody source was computed to be 3.9×10^{-10} watts (peak value). The estimated background photon flux was approximately 10^{13} photons/sec-cm².

The conventional sensitivity notation for IR detectors uses D^* , given by

$$D^*_{\lambda_0} = \frac{(A_d \Delta f)^{1/2}}{P_s} \frac{V_s}{V_n}, \quad (20)$$

where Δf is the bandwidth of the instrument to measure the noise, V_n (volts), and P_s is the input photon signal (watts) to produce the output electric signal, V_s (volts). $D^*_{\lambda_0}$ is equal to $2.8 \times 10^{-8} \times V_s/V_n$, where V_s is the peak-to-peak value. We will compare the measured $D^*_{\lambda_0}$ value of Equation (20) with the best possible theoretical value.

For our results, the best signal was 30 mV (measured at dc and, thus, the peak value) at an integration time of 1 msec. If we operate an array of 32 elements for one msec, the sampling frequency is 3.2×10^4 Hz. For single device measurements, this is the same as a sample pulse period of about 30 μ sec, as far as the sampling rate is concerned. Therefore, the noise was measured at this sampling rate, although the signal was measured with a one msec period (= one msec storage time). A wave analyzer with a $\Delta f = 6$ Hz bandwidth was employed to determine the noise values. At the above sampling rate, the measured noise value varies from 3 μ v at 100 Hz to 2 μ v at 10^4 Hz. We then use an average noise of 2.5 μ v in the information bandwidth (= sampling frequency/2) for the measurements.

The signal-to-noise ratio is then,

$$\frac{V_s}{V_n} = \frac{30 \text{ mv}}{2.5 \mu\text{v}} = 1.2 \times 10^4. \quad (21)$$

Substituting Equation (21) in Equation (20), the $D^*_{\lambda_0}$ is,

$$D^*_{\lambda_0} = 3.4 \times 10^{12} \text{ cm(Hz)}^{1/2}/\text{watt} \quad (22)$$

The theoretical expression of $D^*_{\lambda_0}$ (BLIP) is given by,

$$D^*_{\lambda_0} (\text{BLIP}) = \frac{\lambda_0}{hc} \sqrt{\eta/2Q_B}, \quad (23)$$

where η is the quantum collection efficiency, Q_B , is the background photon flux and the other quantities are well-known. The collection efficiency, η , for our MIS structures was, generally, equal to 50%. For the above background photon flux level, ($Q_B \approx 10^{13}$ photons/sec-cm²), therefore, the theoretical value of the background-limited $D^*_{\lambda_0}$, the best possible sensitivity, is equal to

$$D^*_{\lambda_0} \text{ (BLIP)} = 3.6 \times 10^{12} \text{ cm (Hz)}^{1/2}/\text{watt} \quad (24)$$

which compares closely with the measured value of Equation (22).

In order to measure the device's saturation characteristic, we increased the number of input signal photons and raised the blackbody source temperature to 800°C so that the source signal photons were much larger than the background photons (Q_B). Under this condition, then, the saturation point depends only on the signal photons and can be determined quite accurately. The measured saturation characteristic of a device is shown in Figure 6; the saturation starts at a photon flux density of about 6×10^{14} photons/sec-cm². Thus the maximum number of the stored charges with a quantum efficiency of 50% and the integration time of 500 μ sec is equal to approximately 3×10^8 carriers.

The above maximum stored charges can be compared with the maximum storage capacity of the MIS capacitor. The stored carrier density, N , in the potential well is given by

$$qN = C'_o (V_g - V_{fb} - \phi_s) - (2qN_D \epsilon \phi_s)^{1/2}, \quad (25)$$

where V_{fb} is the flatband voltage and C'_o is the oxide capacitance per unit area. The maximum stored carrier density, N_{max} , for a given gate voltage, V_g , is determined when the system reaches the steady state,

which occurs when the surface potential, ϕ_s , is approximately equal to twice the bulk potential, ϕ_F ; $\phi_s \approx 2\phi_F$. Thus, N_{max} is

$$qN_{max} \approx C'_o (V_g - V_{fb} - 2\phi_F) - (4qN_D \epsilon \phi_F)^{1/2} \quad (26)$$

For the device used, $C'_o = 3.2 \times 10^{-8}$ F/cm². $V_g - V_{fb} - 2\phi_F \approx 2$ volts and $N_D \approx 10^{16}$ cm³. Since the bulk Fermi level of n-type InSb at this doping level is near the conduction band, the bulk potential, ϕ_F , is equal to about 0.1 volts. Using these values, the maximum carrier density, N_{max} , that can be stored in the MIS structure is,

$$N_{max} \approx 2 \times 10^{11} \text{ carriers/cm}^2, \quad (27)$$

which leads to the maximum number of stored carriers for an area of 2×10^3 cm², i.e. 4×10^8 carriers. This value agrees with the experimentally determined value of 3×10^8 carriers within the experimental accuracy.

As shown in the above equation, N_{max} is directly proportional to the gate voltage, V_g . To increase the storage capacity, however, V_g cannot be increased to any arbitrary higher value, because the avalanche breakdown voltage of InSb materials appears to be relatively small. It should be pointed out, however, that the measured dynamic range for $\Delta f = 6$ Hz is already in the range of six orders of magnitude.

The spectral response of InSb CID devices was also measured; the results are shown in Figure 7. For these measurements an integration time of 100 μ s was used. The device output signal voltage, corrected for the thermocouple readings, was measured as a function of wavelength.

It is interesting to note that there is no sharp peak in the spectral response and that the response in the shorter wavelength region is excellent. In fact, the quantum

efficiency is almost constant from 5μ to 1μ . This is due to the fact that, for such a device structure, high collection efficiencies can be obtained since the depletion region is formed at the surface. No carrier diffusion is required for collection, as is normally required in a p-n junction photodiode, because most of the carriers are generated in the high field region. This is why, for the higher energy photons (shorter wavelength region), the quantum efficiency is as good as that for the peak response.

V. CONCLUSIONS

A metal-insulator-InSb MIS technology has been developed. The interface state density of these structures conforms to the Shockley-Read-Hall theory of interface states; experimentally the density has been measured in the range of $10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ (varying with the surface potential from the mid- 10^{10} to mid- $10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ range).

Because of the low surface state densities, we have been able to fabricate InSb MIS structures that operate in the charge injection mode. The quality of the interface of these devices makes possible low dark currents, near background-limited performance, and a saturation characteristic that follows the theoretically expected storage capacity of an MIS capacitor. A detailed analysis of the interface properties based on conductance measurements agreed well with theoretical models.

ACKNOWLEDGEMENT

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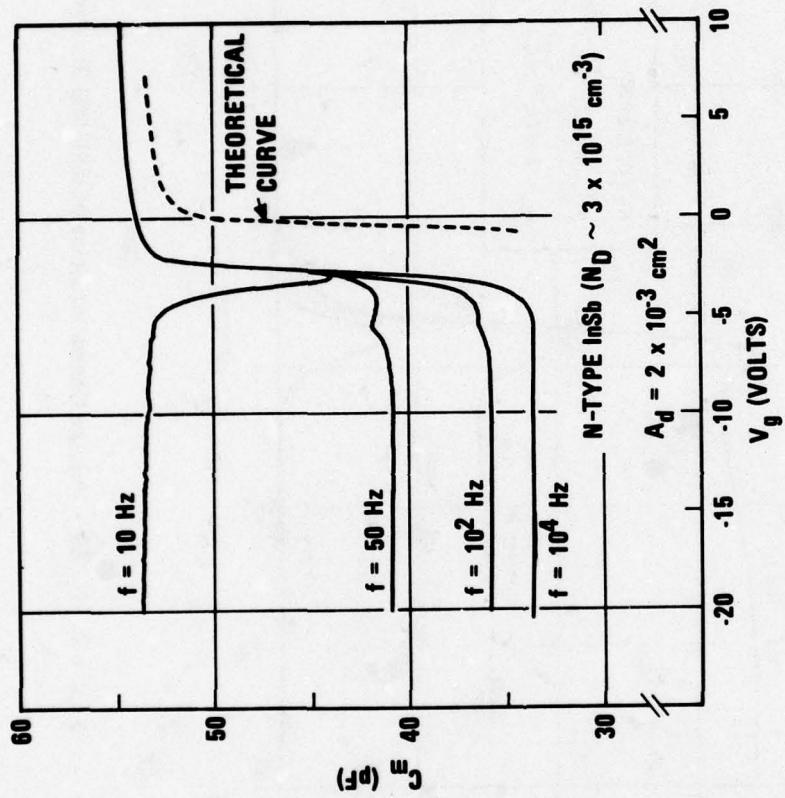


Figure 1. C-V Characteristics of InSb MIS Structure

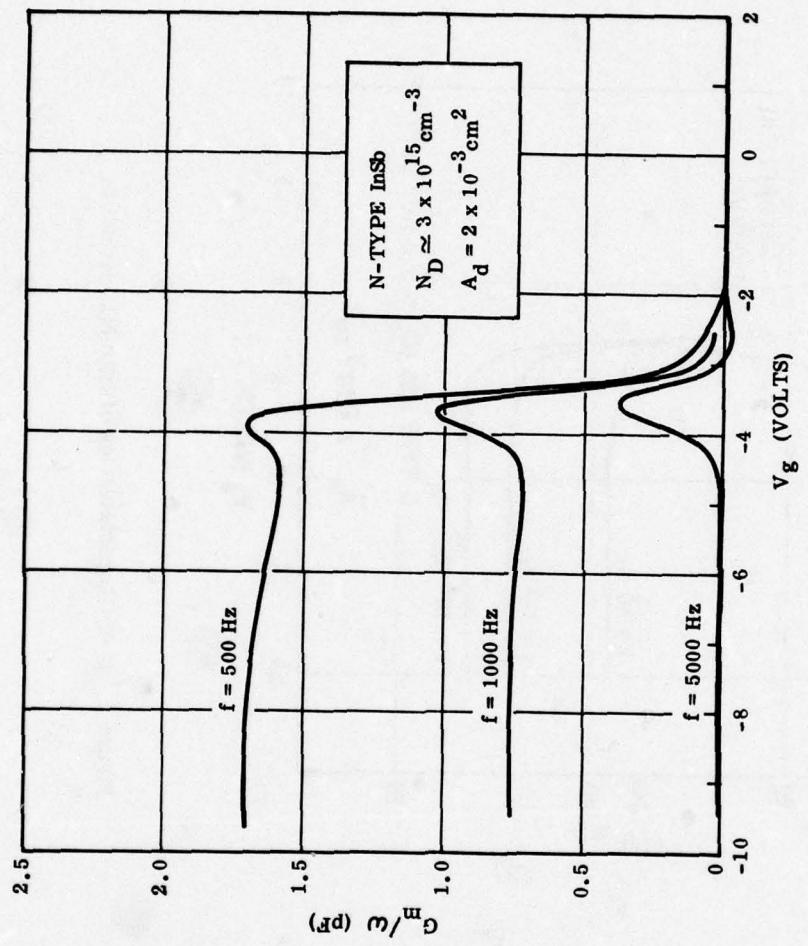


Figure 2. G_m/ω - Voltage Characteristics of InSb MIS Structure.

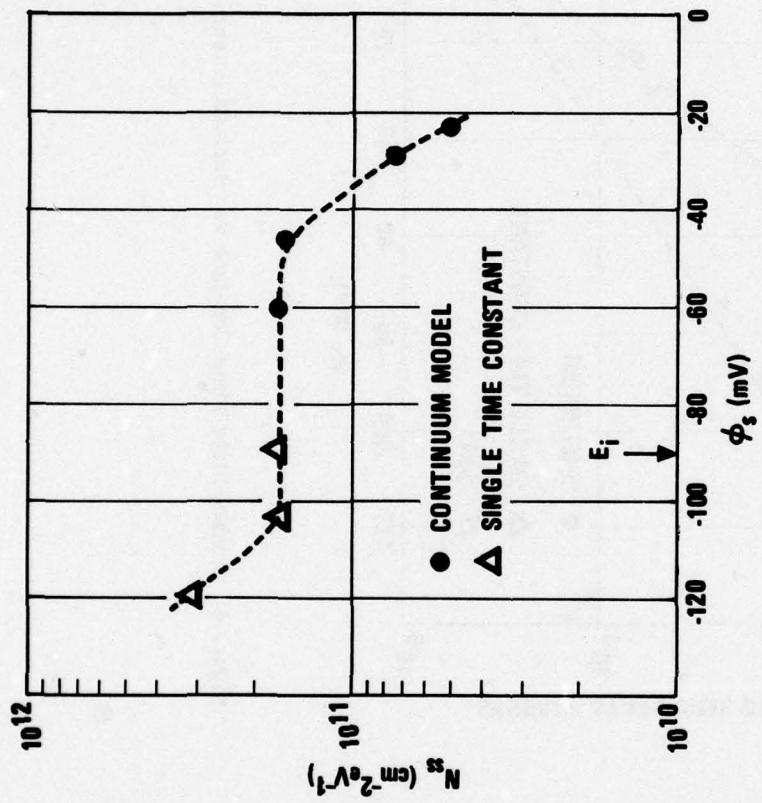


Figure 3. Surface State Density (N_{ss}) vs. Surface Potential (ϕ_s).

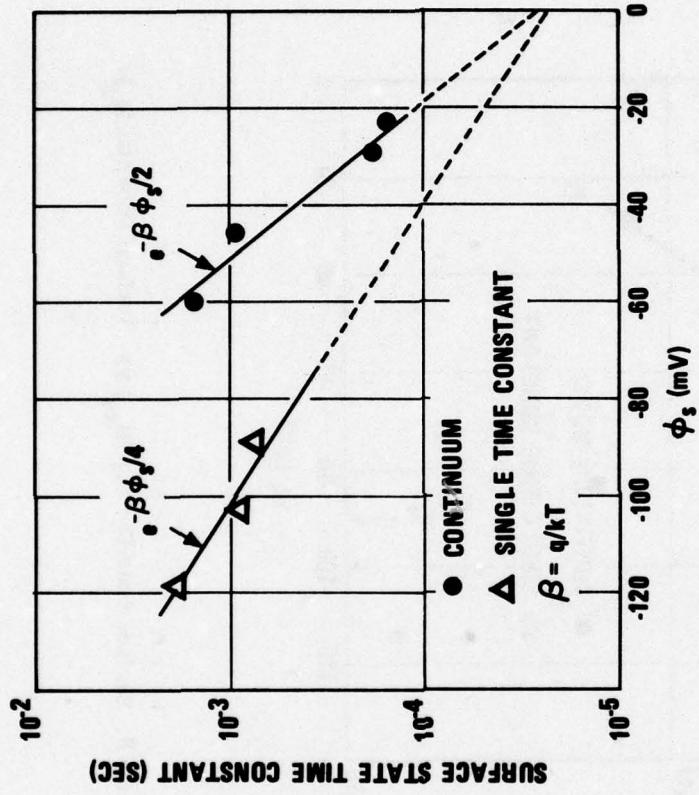


Figure 4. Surface State Time Constant vs Surface Potential.

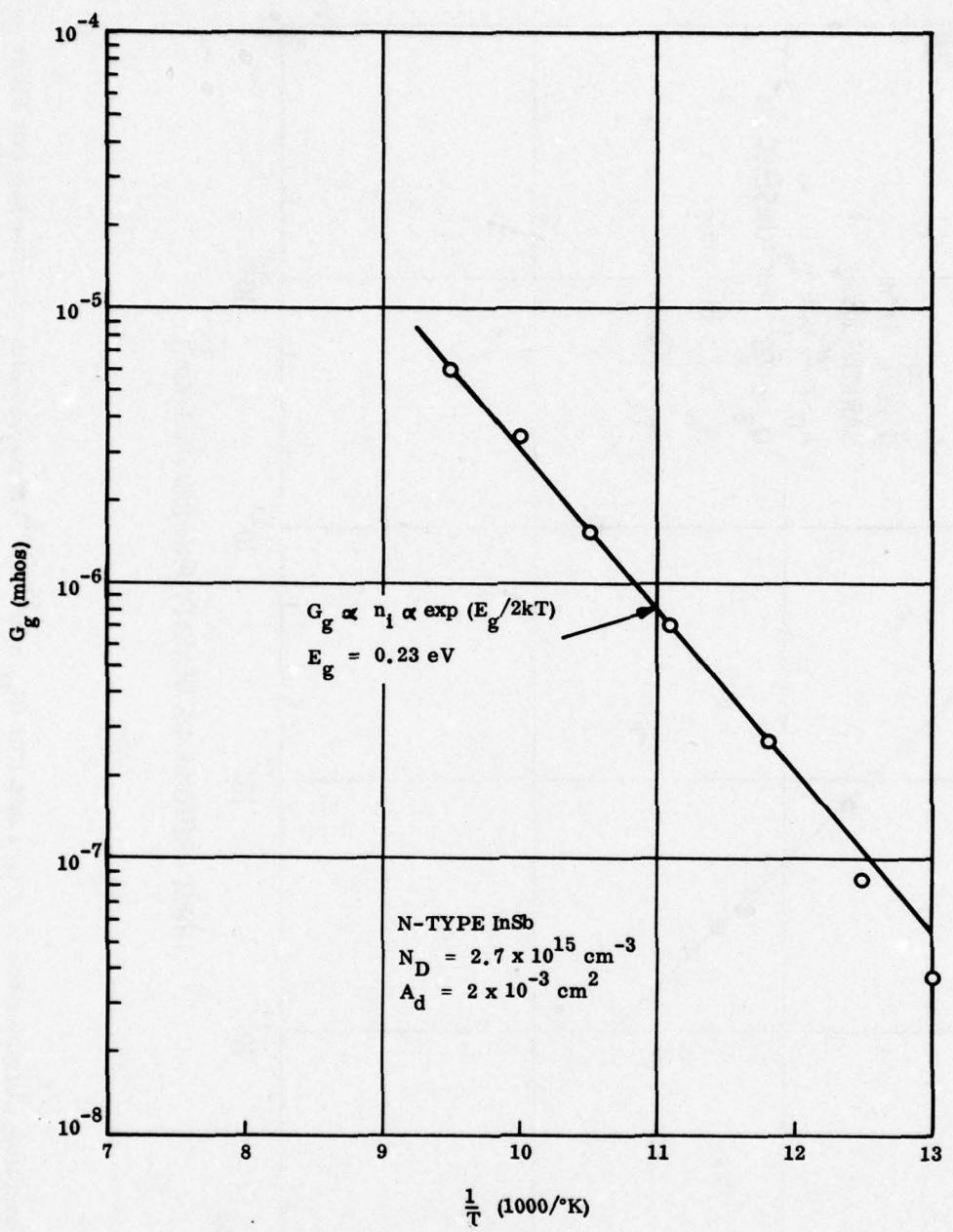


Figure 5. Thermally Generated Conductance (G_g) vs Reciprocal Temperature ($1/T$).

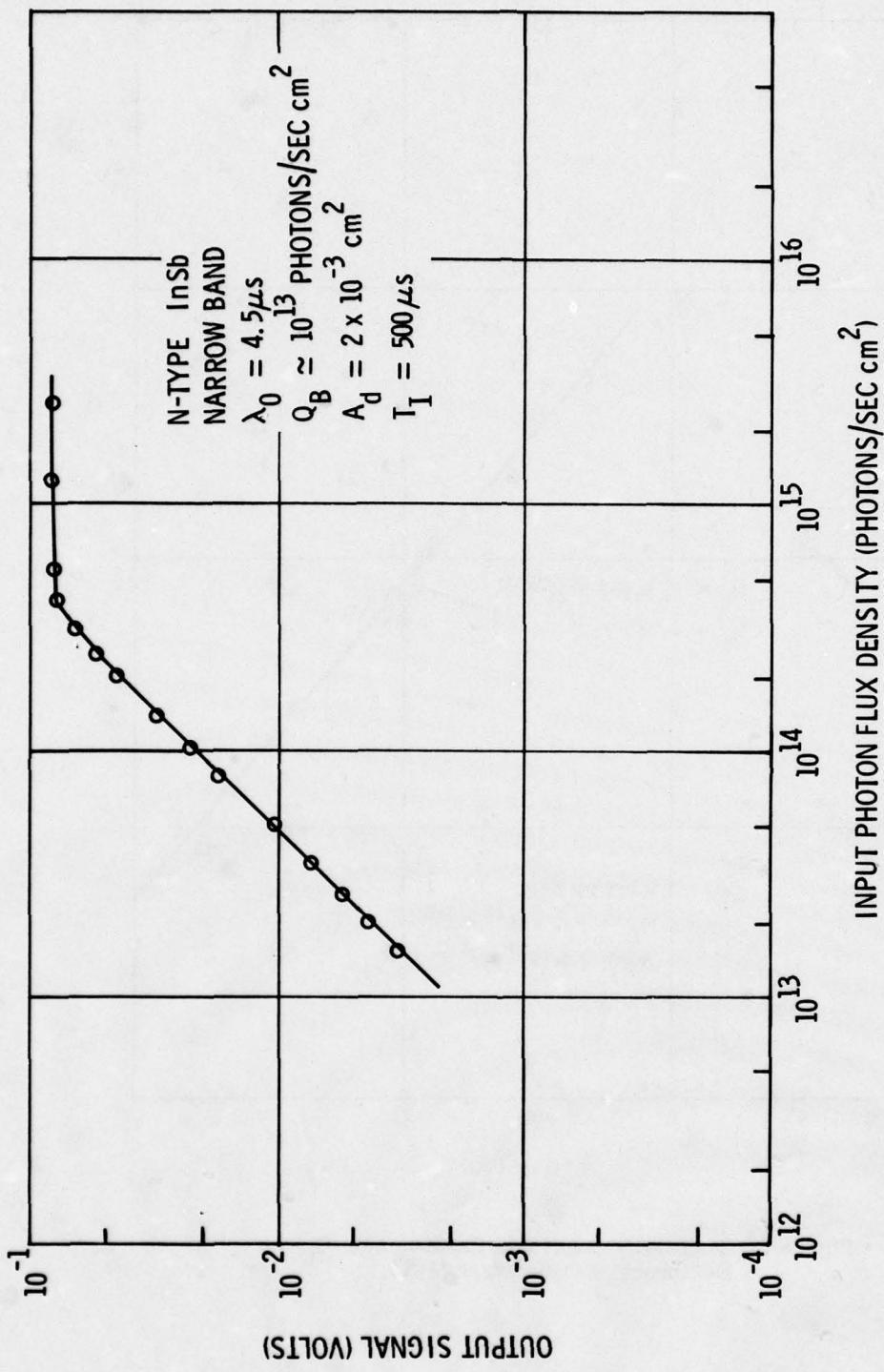


Figure 6. Saturation Characteristic of N-type InSb CID ($N_D \approx 10^{15} \text{ cm}^{-3}$) Measured with a Narrow Spectral Filter

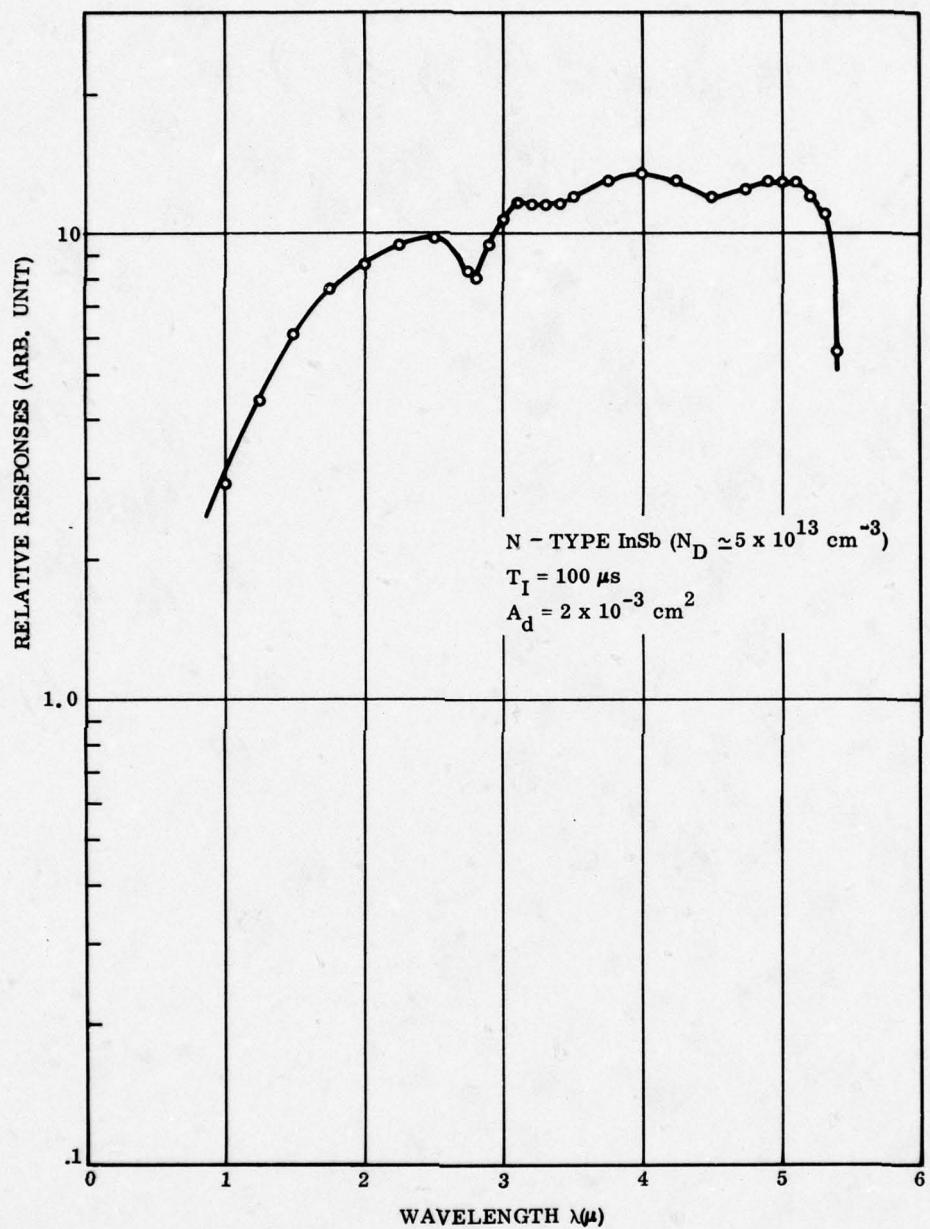


Figure 7. Spectral Response of N-type InSb CID ($N_D \approx 5 \times 10^{13} \text{ cm}^{-3}$).

EXTRINSIC SILICON MONOLITHIC FOCAL PLANE ARRAY
TECHNOLOGY AND APPLICATIONS*

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ABSTRACT. The purpose of developing extrinsic silicon monolithic infrared focal plane arrays is to improve the performance and reduce the cost of electro-optical sensors. The technology for making 1024-element mosaic arrays is discussed.

Data on quantum efficiency and detectivity (D^*) as a function of wavelength and temperature is presented for gallium- and indium-doped silicon. The effect of compensation on detector responsivity is reviewed. The results of measuring the crosstalk of $1 \times 2 \text{ mil}^2$ and $4 \times 4 \text{ mil}^2$ monolithic detectors are also presented. Low-temperature ($<20^\circ\text{K}$) CCD operation has been demonstrated, and a relative transfer loss of less than 4×10^{-5} has been observed. Various chip designs are shown and discussed.

INTRODUCTION

Most current high-performance infrared electro-optical sensors consist of infrared telescopes, mechanical azimuth (and elevation) scanners, and linear (or small, two-dimensional) infrared-sensitive arrays with their associated detector preamplifiers and video multiplexers. The performance of well designed infrared sensors is close to that theoretically predicted⁽¹⁾. Performance is usually expressed as noise equivalent temperature difference (NETD), minimum resolvable temperature difference (MRTD), or noise equivalent target (NET) for point sources.

By using the standard performance equations one can trade off signal-to-noise ratio (SNR) and resolution against the diameter of the optics, the field of view (FOV), scan rates, number of detector elements, etc. Such tradeoffs are usually made in order to optimize a sensor for a specific application. The principal limitations on sensor performance are the diffraction limit of the optics in the infrared

spectral region and the number N of infrared-sensitive detector elements, which for state-of-the-art sensors is less than 1000.

In order to improve infrared sensor performance without increasing the diameter of the optics beyond a typical value, the number of detector elements in the FOV must be increased. For a given FOV and angle subtended by one detector element, the value of SNR increases with the number of such elements as \sqrt{N} . For a given value of SNR and angle subtended by one detector element, the sensor FOV increases linearly with the number of such elements within the limits imposed by the properties of geometrical optics.

The purpose of developing extrinsic silicon monolithic focal plane arrays⁽²⁾ (MFPA) or infrared charge coupled devices (IRCCD) is to improve performance beyond that of current electro-optical sensors without increasing the number of components and therefore the cost of such sensors. A realistic goal is to develop MFPA

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containing 32 x 32 or 1024 detector elements per chip. Such arrays are illustrated in this paper. By stacking these chips in the focal plane in the same way as detector elements are now stacked, it appears reasonable to assume that an order-of-magnitude improvement in performance can be achieved in the near future.

Several hybrid and monolithic IRCCD devices have been previously discussed^(2, 3, 4-7). These devices are classified as hybrid or monolithic infrared CCDs, respectively, depending on whether they consist of infrared detector materials, such as InSb, HgCdTe, PbSnTe, PbS, etc. combined with silicon CCDs, or whether these detector elements and the CCD readout registers are processed in the same material. The emphasis in this paper is on monolithic extrinsic silicon focal plane arrays which have the obvious advantage of being based on the highly developed "standard" silicon processing technology.

QUANTUM EFFICIENCY OF EXTRINSIC SILICON MFPA'S

Extrinsic silicon MFPA's use the CCD substrate as the infrared-sensitive detector. Such a detector is operated in the photoconductive mode. Other structures, such as diffused junctions, photocapacitive devices, MOS junctions, and Schottky barrier junctions, have been considered⁽⁵⁾ for use in IRCCDs.

The photoconductive detector is the only detector having an absorption thickness that is large enough to provide an acceptable detector quantum efficiency with the weak transitions^(8, 9) characteristic of extrinsic silicon. A typical absorption cross section σ for gallium-doped silicon at 10 μm , for example, is $\sigma = 4 \times 10^{-16} \text{ cm}^2$. An acceptable quantum efficiency (≥ 50 percent) is obtained if $\sigma (N_A - N_D) l \geq 1$, where $N_A - N_D$ is the acceptor minus the donor concentration ($3 \times 10^{16} \text{ cm}^{-3}$) and l is the thickness of the sample in the direction of the incident radiation. On the basis of these values, one finds that the required thickness is $l \geq 0.8 \text{ mm}$.

Figure 1 shows the theoretical and measured values of quantum efficiencies of

Si:Ga arrays for doping concentrations in the range as a function of wavelength,

$$10^{16} < N_{\text{Ga}} < 10^{17} \text{ gallium ions/cm}^3$$

The calculation is based on the wavelength dependence⁽⁸⁾ of σ and the classical expression for the external quantum efficiency, i. e.,

$$\eta = \frac{(1 - R)(1 - e^{-N\sigma l})}{(1 - Re^{-N\sigma l})}$$

where

R = single-surface reflection coefficient

N = density of absorbing centers

σ = absorption cross section

l = thickness of detector

This relation holds for a transverse detector and it approaches a maximum value of $1 - R$ (≈ 0.5 for silicon) for large values of $N\sigma l$. In MFPA structures, such as those discussed here, the current flows parallel to the direction of the incident radiation. In this case the expression is slightly modified.

The main considerations in regard to the expected quantum efficiency of extrinsic silicon detectors are (1) the maximum solid solubility of the impurity in silicon and (2) the way in which impurity banding affects detector performance when the detector is doped near the solid solubility limit.

The photoconductive gain of extrinsic silicon is directly proportional to the product of mobility and lifetime $\mu\tau$ and to a frequency response factor $g(f, Q_B)$ which derives from the space charge relaxation near the injecting contacts. The 3-db cut-off frequency $f_{3\text{db}} (Q_B)$ is a function of the average background photon flux density Q_B (photons/ $\text{cm}^2\text{-sec}$) incident on the detector. The transient response of extrinsic silicon detectors also depends on the space charge relaxation near the contacts.

The photoconductive lifetime of extrinsic silicon is inversely proportional to the

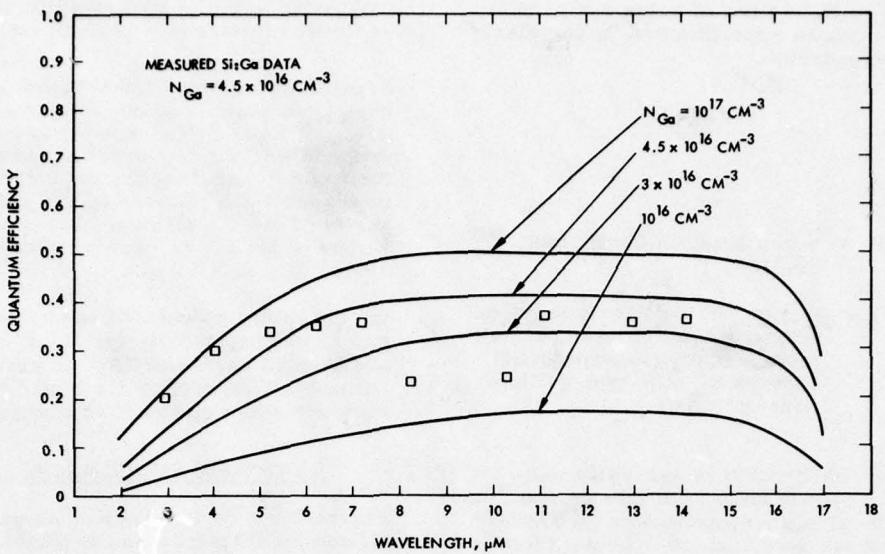


Figure 1. Theoretical and measured quantum efficiency of Si:Ga MFPAs

number of compensating impurities in this material. In gallium-doped silicon, these impurities are phosphorous having a concentration of about $2 \times 10^{13} \text{ cm}^{-3}$. Such impurities (donors) are introduced into the crystal in order to compensate for the residual boron (acceptor) impurities that are always present in the polycrystalline silicon starting material with a concentration of about 10^{13} cm^{-3} . In typical extrinsic silicon materials, the lifetimes range from 10 to 100 nsec, depending on the details of the particular crystal parameters.

The hole mobility of gallium-doped silicon from $50^\circ\text{K} < T < 250^\circ\text{K}$ is approximately $1 \times 10^4 \text{ cm}^2/\text{volt}\cdot\text{sec}$ for $N_{\text{Ga}} = 3 \times 10^{16} \text{ cm}^{-3}$.

Selected values of the product $\mu\tau$ or photoconductive gains have been presented for extrinsic silicon detectors for different values of background photon flux density and temperature for both gallium- and indium-doped crystals(10). Hall effect data on the crystals shows that the carrier concentration is a function of $1/T$ and that the activation energy for the various levels (gallium, boron, etc.) appears as the slopes of the curves expressing this function.(9).

The relaxation time due to space charge effects can be approximated by

$$\tau_s = 2G\tau_p$$

where

$G = \mu\tau E/d$ = photoconductive gain

E = bias field, volts/cm

d = detector thickness, cm

$\tau_p = \epsilon\epsilon_0 d(\mu\tau Q_B)^{-1}$ = dielectric relaxation time, sec.

ϵ = relative dielectric constant (12 for silicon)

ϵ_0 = dielectric constant of free space

q = electronic charge, coulombs

Q_B = background photon flux at focal plane, photons/cm²-sec

Note that the term $\mu\tau/d$ is cancelled out in the expression for τ_s ; hence
 $\tau_s = \tau_p (E, Q_B) = 2 \epsilon\epsilon_0 E/(qQ_B)$

The relaxation time of holes due to bulk effects can be approximated by the classical expression

$$\tau = (BN_p)^{-1}$$

where

B = recombination coefficient,
 cm^3/sec

N_p = number of negatively ionized trapping centers per cm^3 . (compensating phosphorous centers N_p in p-type gallium-doped silicon)

This approximation is generally valid for $N_p > 10^{11}$ phosphorous centers per cm^3 and for typical background photon flux levels Q_B that are less than 10^{16} photons/ $\text{cm}^2\text{-sec}$.

Typical values of τ are $10 < \tau < 100$ nsec and $\tau_s = 1.35 \times 10^7 E/Q_B$. For a typical bias field E of 200 v/cm and for a background photon flux Q_B of 10^{14} photons/ $\text{cm}^2\text{-sec}$, $\tau_s = 27 \mu\text{sec}$. Except for very high values of Q_B , the dominant time constant is the space charge relaxation time constant.

The static responsivity $R_\lambda = 0.804 \lambda \eta G$ amperes/watt (where λ is measured in μm and η is the quantum efficiency) can be measured directly and compared with the

calculated value of responsivity based on known parameters of the material.

Several lots of the 2096 MFPA's (see below) have been processed on both Czochralski-grown (CZ) and float-zone grown (FZ) materials. This has provided an opportunity for measuring the expected increase in responsivity because of the greater purity of the FZ silicon. Table 1 shows values of MFPA responsivity for four device lots at $\lambda = 4 \mu\text{m}$.

In this table, calculated and measured values of responsivity for the FZ material are in good agreement for an assumed recombination coefficient B of 6.4×10^{-6} cm^3/sec and a quantum efficiency η of 0.25.

EXTRINSIC SILICON MFPA

Figure 2 shows a portion of an extrinsic silicon MFPA array on the Hughes CCD 2063 test chip. This chip has several linear arrays with integral CCD readout. The performance of this test chip has been previously reported. (11) Crosstalk characteristics have recently been investigated and are described here.

Figure 3 shows the measured and calculated spot scan of a detector in the 32-element MFPA on CCD 2063. The calculated response is the convolution of the effective detector width and the blur spot size. The effective detector width is larger than the detector contact size because of the distribution of the biasing electric field lines between adjacent detector elements in the structure. The structure between the

Table 1. MFPA responsivity

Lot No.	Material	Compensation (total donors), cm^{-3}	Responsivity, amperes/watt	
			Predicted ($E=200$ v/cm)	Measured
2063-20	CZ	10^{14}	0.26	0.185
2096-2	CZ	10^{14}	0.26	0.04 to 0.11
2096-10	FZ	9.9×10^{12}	2.5	2.48

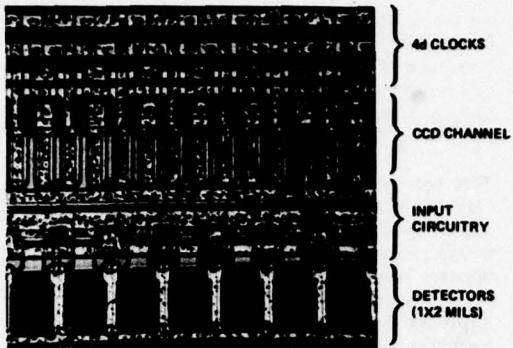


Figure 2. Extrinsic silicon MFPA test chip

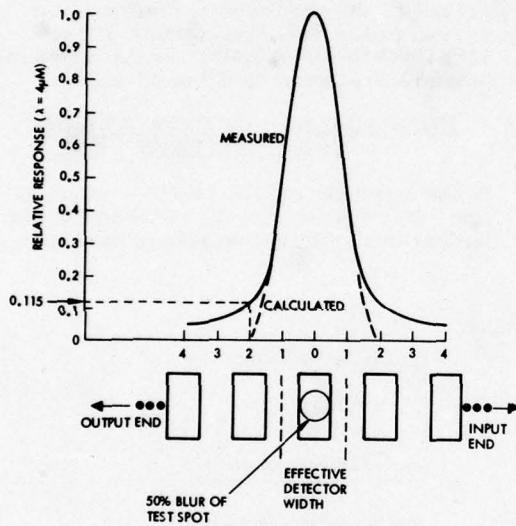


Figure 3. Spot scan of 1×2 mil detector on CCD 2063

contacts is transparent to infrared radiation. The measured spot scan shows 11.5-percent crosstalk at the center of the adjacent detector element when an f/1.5 optical system is used to generate the test spot. The MFPA was 0.020-inch thick with a Si:Ga substrate. As shown in Figure 4, the response is linear with detector bias.

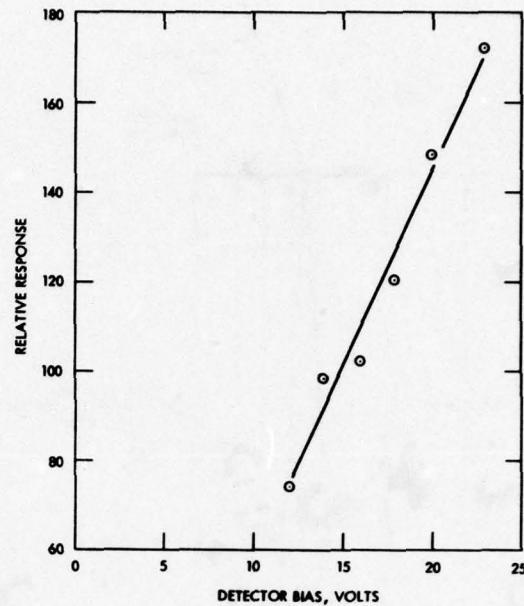


Figure 4. 2063 MFPA output as a function of chip bias

Crosstalk in the MFPA structure is due to bulk optical effects, including reflection from the back surface (see Figure 5). The electrical crosstalk is negligible because the lateral diffusion of the carriers is on the order of $1 \mu\text{m}$. In addition, shunting surface conductance paths between adjacent detector contacts due to dopant impurity pile-up at the processed surface do not occur in this structure.

As shown in Figure 5, the incoming optical cone converges in the silicon substrate because of the change in the index of refraction. Crosstalk is therefore a function of f-number, quantum efficiency η , and backside reflectivity ρ . The measured crosstalk indicated in Figure 3 is shown as a point on the calculated curves in Figure 6. In the calculated curves, the detector geometry shown in Figure 3 was assumed. The second curve in Figure 6 shows the projected crosstalk with greater quantum efficiency (dopant concentration) and the elimination of backside reflectivity. If this reflectivity is small, crosstalk can be further reduced.

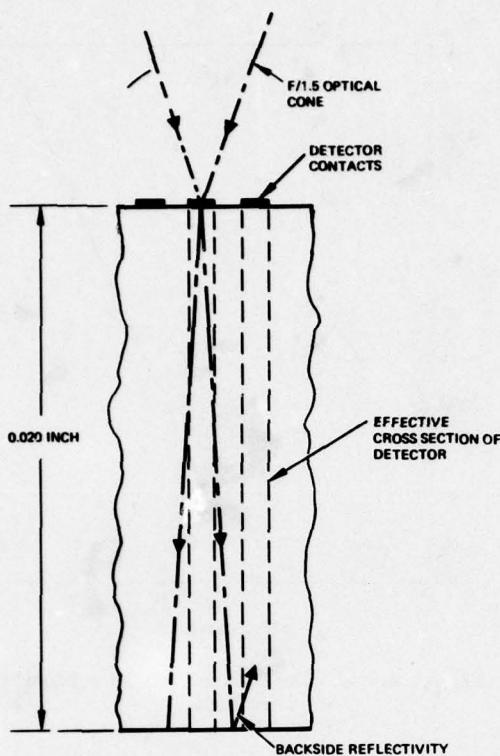


Figure 5. Cross section of extrinsic silicon MFPA

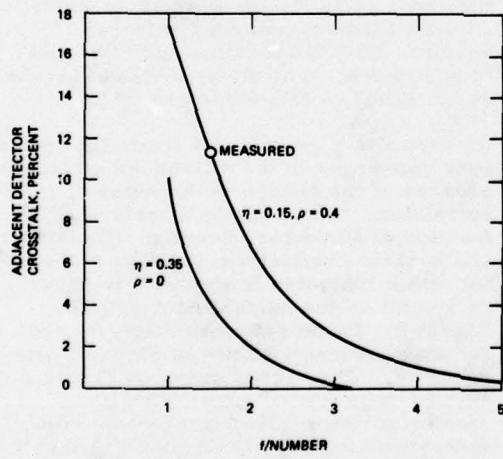


Figure 6. Si:X MFPA crosstalk as a function of optical f/number

by reducing the MFPA thickness. At higher f/numbers, crosstalk approaches zero because the rays entering the silicon are refracted to an angle that is almost perpendicular to the front surface of the MFPA.

The temperature at which an extrinsic silicon MFPA (or any extrinsic detector) must operate in order to achieve BLIP performance depends on the focal plane photon background and on the energy level (spectral cutoff) of the dopant used. Figures 7 and 8, which show $D^* \lambda_{pk}$ as a function of temperature, define the operating temperatures required for two popular extrinsic detector materials (Si:In and Si:Ga), respectively. In Figure 7, the theoretical BLIP operating temperatures for Si:In range from 5° to 10° lower. In a similar fashion, in Figure 8, the predicted operating temperatures for Si:Ga range from 21° to 32°K. For present materials the operating temperatures must be 3° to 5° lower.

PERFORMANCE OF CCDs AT LOW TEMPERATURES

In the extrinsic silicon MFPA configuration, CCDs must operate at the same low temperature that the detectors need for

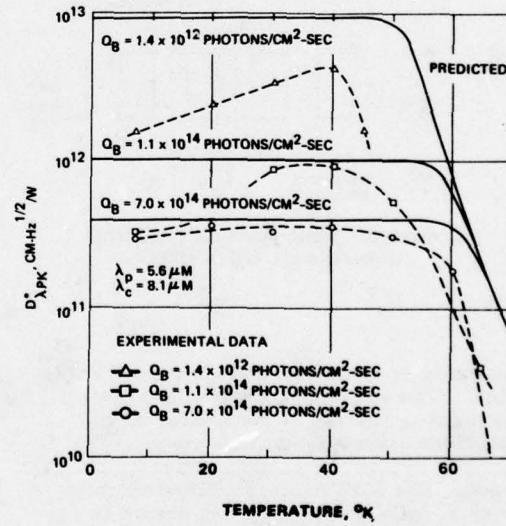


Figure 7. $D^* \lambda_{pk}$ of Si:In as a function of temperature

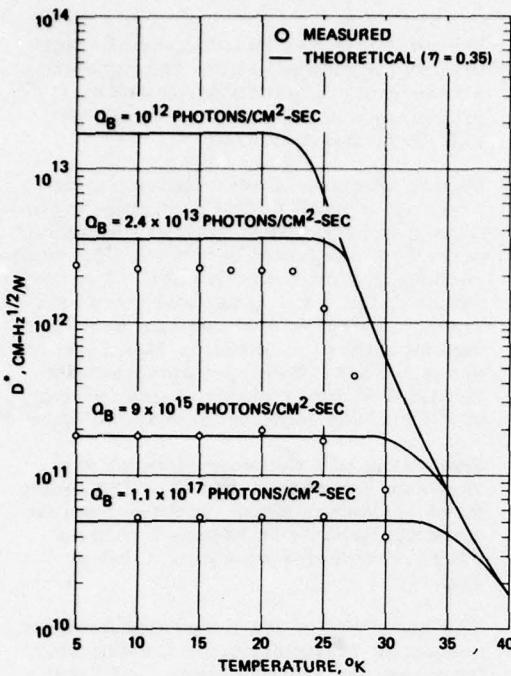


Figure 8. $D^* \lambda_{pk}$ of Si:Ga as a function of temperature

BLIP operation. These operating temperatures can be lower than the temperature at which the onset of thermal carrier freeze-out begins for the CCD. Current understanding of the low-temperature operation of MOS devices suggests that greater noise and poor transfer efficiency may result in this case. Since it is important to the success of an extrinsic silicon MFPA, it is appropriate to review some low-temperature CCD test results.

Figure 9 shows measured CCD transfer efficiency as a function of clock frequency at four different operating temperatures. The CCD tested was a 150-bit shift register (Hughes CCD 2070) processed as a p-surface channel device. Devices from several different lots were evaluated. Dewar test leads limited the test setup to clock frequencies of less than 200 kHz. This figure shows that transfer efficiency increases below room temperature and that at temperatures from 80° to 13°K, the transfer loss $\epsilon = 1 - \alpha$, has an average value of less than 4×10^{-5} (corresponding to a transfer efficiency α of 0.99996).

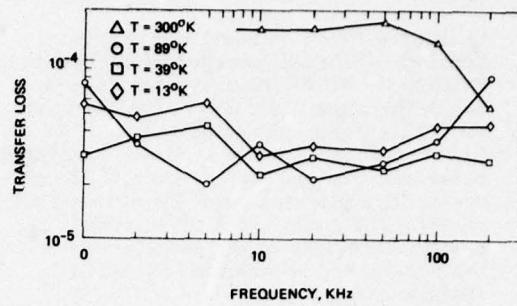


Figure 9. CCD transfer of a function of clock frequency

To help establish a criterion for acceptable values of transfer efficiency for MFPA's, the CCD output pulse height as a function of number of transfers was plotted (See Figure 10). The relative amplitudes of the first, second, and third output pulse are shown for an input pulse having an amplitude of unity. The value of transfer efficiency α is assumed to be 0.9999 ($\epsilon = 10^{-4}$).

For most applications, maintaining a pulse fidelity within 1 percent is adequate. Figure 10 shows that if all bits of the CCD convey a signal, the number of transfers

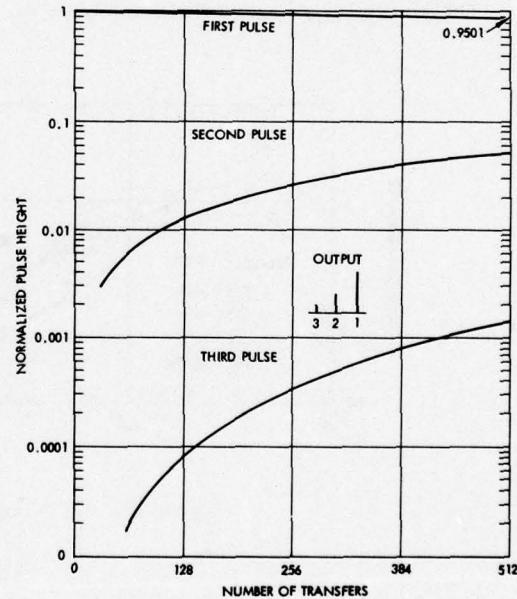


Figure 10. CCD pulse height as a function of number of transfers for $\alpha = 0.9999$

is limited (for 1-percent fidelity) to approximately 100 because of second-pulse spillover. In the more typical case in which the signal is conveyed in alternate bits, this figure shows that even after 512 transfers, fidelity as limited by third-pulse spillover is greater than 0.12 percent. It is therefore concluded that a CCD transfer efficiency of 0.9999, which is easily achievable at the detector operating temperatures, is adequate for most applications.

Figure 11 shows the noise spectral density measured with the same CCD as that used in the transfer efficiency tests (see Figure 9). Measurements were also made at the same four operating temperatures. In Figure 11, the average midband noise is approximately 2.5 noise carriers/ $\sqrt{\text{Hz}}$, which is equivalent to a total integrated noise of 30 noise carriers/bit normalized to an 0.001-inch channel width. For a surface channel CCD, this level of noise is normally considered to be lower than average.

In summary, it appears that the low-temperature transfer efficiency and noise characteristics of surface channel CCDs display no anomalous behavior at

low temperatures and that they in fact improve somewhat at low temperatures. Measurements show that transfer efficiency and noise level are acceptable for most applications.

Figure 12 shows a second-generation extrinsic silicon MFPA test chip; it contains a family of test devices, including three new basic concepts for CCD detector readout in monolithic format. Two test devices, the 4×4 array and the 32×2 array, are being evaluated as part of the development of a complete 32×32 staring array. These devices employ almost identical detector elements measuring 0.004×0.004 inch, as shown in Figure 13.

Spot scans of a detector element are shown in Figures 14 and 15. The calculated responses shown in these figures were obtained as in Figure 3 with an assumed detector aperture 4 mils square.

The geometry of the integrated detector contact is responsible for the departure from the calculated curves, but these scans do indicate that an effective detector area that is 80 percent of the detector element area can be achieved.

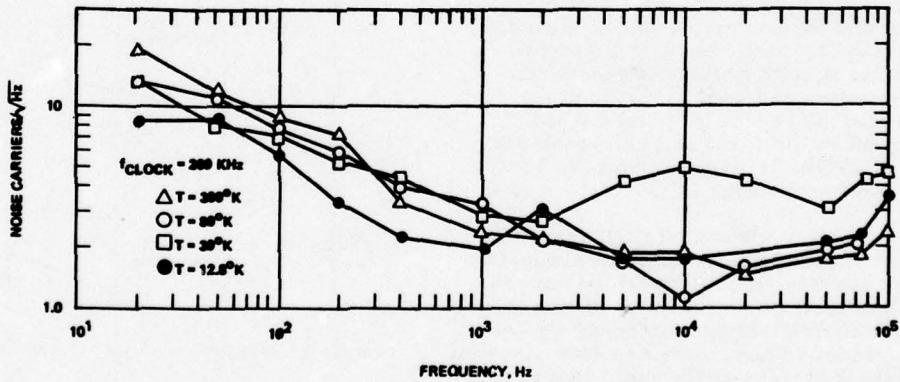


Figure 11. CCD noise as a function of frequency

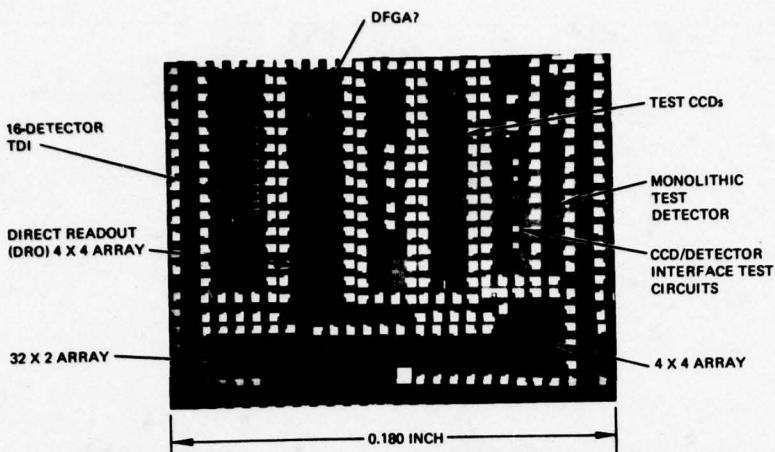


Figure 12. Extrinsic silicon test chip CCD 2096

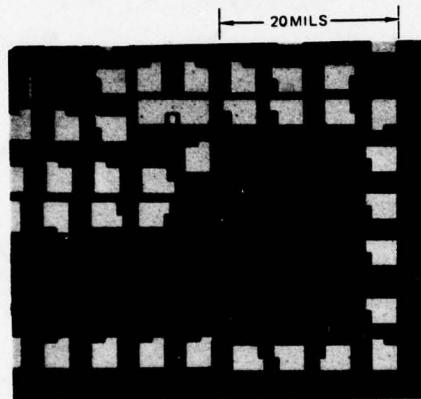


Figure 13. MFPA 4 x 4 array

Figure 16 shows the two output pulse trains from the 2 x 32 array. The integrated detector signals are transferred to the readout CCDs by pulsing the transfer electrode (the transfer pulse shown in this figure) and then read out serially. The uniformity of response is approximately ± 15 percent. At present, it is limited by the variation in the concentration of gallium in the detector volume.

This amount of variation is acceptable for certain staring sensors used for "change

detection". More sophisticated differential encoding techniques can be used when variations in array response must be compensated for, as in imaging applications.

32 x 32 MFPA

A layout of a 32 x 32 detector MFPA is illustrated in Figure 17. The overall chip dimensions are 184 x 187 mils. The total active area is 128 x 128 mils. Each detector element (4 x 4 mils) contains input circuitry, a storage bucket, an overload protection device, a transfer gate, and four bits of CCD readout. Each row of the array consists of 32 detector elements and 128 CCD bits. A 128-bit multiplexing CCD (at the left in this figure) reads the charge out columnwise from the array.

POWER DISSIPATION ON FOCAL PLANE

In systems which will utilize a large number of MFPA chips, power dissipation on the focal plane becomes an important design factor. The sources of electrical power dissipation are briefly discussed below.

Electrical power dissipation on the focal plane chip originates from (1) the

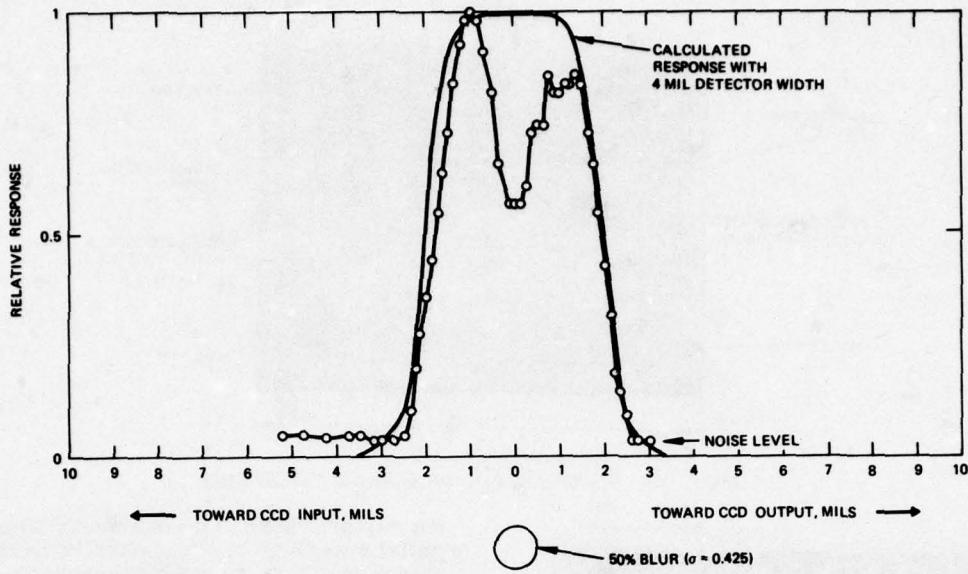


Figure 14. Parallel scan (along array) by a detector element of the Hughes 2096 2 x 32 MFPA

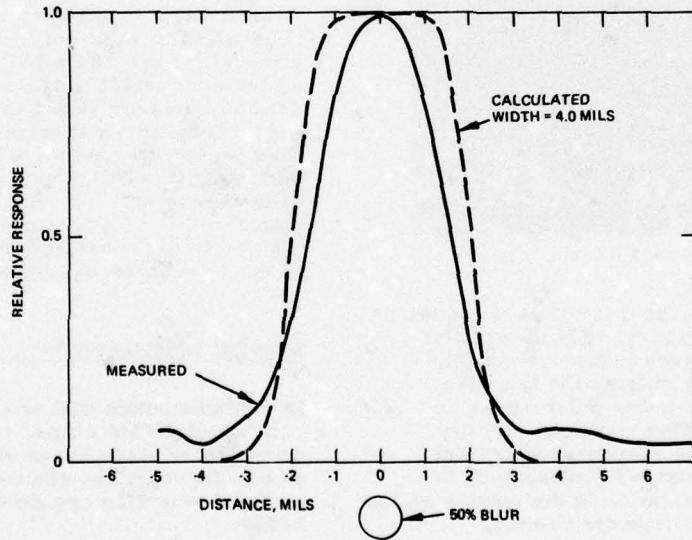


Figure 15. Perpendicular scan by a detector element of the Hughes 2096 2 x 32 MFPA

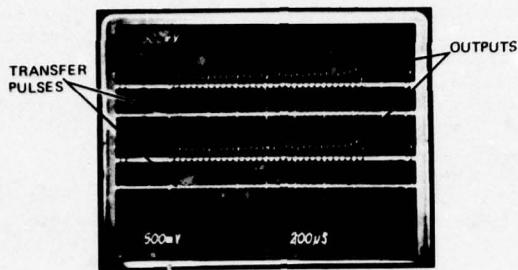


Figure 16. Outputs from 2 x 32 array

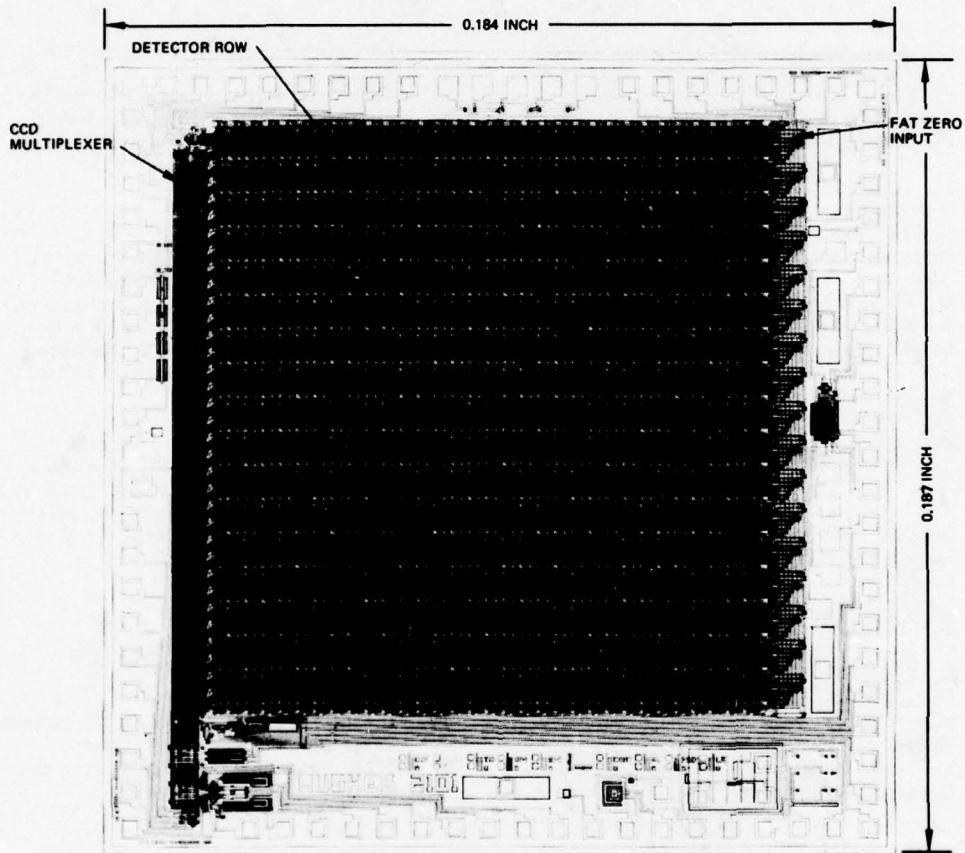


Figure 17. Layout of 32 x 32 MFPA (Hughes CCD 2101)

detectors, (2) the CCD readout registers, and (3) the output circuitry. The power dissipated by this circuitry is expected to dominate and depends primarily on the bandwidth. At clock rates of 200 kHz, bias currents of at least 0.1 ma and a drain voltage of about 6 volts, output MOS devices dissipate about 0.6 mw. This amount of power combined with that dissipated by the detectors brings the total power dissipated to less than 1 mw/chip.

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InSb CCDs AND OTHER MIS DEVICES
FOR INFRARED APPLICATIONS*

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ABSTRACT. Indium antimonide (InSb) CCDs and other MIS devices have been fabricated and successfully operated. The CCDs are four-phase, overlapping gate, surface channel devices fabricated on n-type, single-crystal InSb. The demonstration of charge coupling in this material offers the potential of a future generation of 1- to 5- μm charge-coupled infrared imaging devices (CCIRIDs). Fabrication of the MIS structures is discussed. Several properties of the insulator-InSb interface were evaluated from MOSFET and MIS capacitor data. Measurement of interface state density has indicated midband values of $6 \times 10^{11}/\text{cm}^2\text{-eV}$. Storage times of up to 0.5 sec have been measured at 77°K; the dark current at this temperature is shown to be due to bulk, rather than surface, generation. Effective inversion layer mobility of 250 to 500 $\text{cm}^2/\text{volt}\cdot\text{sec}$ has been determined from the MOSFETs. Results are given for a four-bit InSb CCD with 200- μm bit length. An efficiency per transfer of 0.90 was measured for this device, limited by the gate length of the CCD and the interface state density. Efficiencies of 0.99 or better are projected for InSb CCDs with shorter gate lengths. Other devices for infrared applications utilizing InSb MIS structures have also been fabricated; results are given for single- and multi-element MIS detectors utilizing substrate injection readout.

I. INTRODUCTION

Since the advent of charge-coupled devices, several new concepts for the fabrication of high-density infrared detector arrays have been developed or proposed. The application of CCD readout and signal processing techniques to infrared arrays promises a new generation of infrared focal plane assemblies with significantly improved performance and reduced power and weight requirements. Several approaches for the integration of CCDs and infrared detectors are currently under development, including: 1) hybrid assemblies of conventional silicon CCDs and infrared detectors; 2) sandwich structure configurations, where silicon CCDs and infrared detectors are bonded together in a planar "sandwich" configuration and interconnected using advanced lead fabrication techniques; 3) monolithic silicon devices where CCDs are fabricated on appropriately doped silicon substrates, and extrinsic photoconductivity is employed for the detection mechanism; and 4) monolithic devices fabricated on a narrow-band semiconductor material, such as InSb, where both detectors and CCDs or related devices for readout are integrated in the same material and intrinsic photo-detection is utilized. This fourth concept is the objective of the development reported in this paper.

lithic silicon devices where CCDs are fabricated on appropriately doped silicon substrates, and extrinsic photoconductivity is employed for the detection mechanism; and 4) monolithic devices fabricated on a narrow-band semiconductor material, such as InSb, where both detectors and CCDs or related devices for readout are integrated in the same material and intrinsic photo-detection is utilized. This fourth concept is the objective of the development reported in this paper.

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A monolithic infrared imaging device fabricated in the appropriate narrow-band semiconductor represents in many ways the ultimate solution for realizing an infrared imaging device. The absorption coefficient of the intrinsic material is high; therefore, high quantum efficiencies can be realized. Further, the high absorption coefficient eliminates crosstalk effects that can occur in extrinsic silicon structures. Higher permissible operating temperatures are also an advantage of the intrinsic material approach, which can be critically important in many space and tactical applications where cooling to lower temperatures is impractical.

InSb was selected for development based on the relative maturity of InSb technology compared with that of other infrared detector materials, favorable material parameters, and a spectral response suitable for a wide range of potential applications below 5.4 μm . Two such applications are infrared imaging for earth resources and planetary missions. A configuration particularly suited to these applications is the charge-coupled infrared imaging device (CCIRID), which would combine InSb metal-insulator-semiconductor (MIS) detectors and CCD readout registers in a two-dimensional array. One method of achieving significant performance improvements is to use time delay and integration (TDI) of the infrared signals on the focal plane,¹ utilizing InSb CCDs for the delay-and-add function. The possibility of achieving TDI in real time, within the imaging device itself, is an important feature of this InSb technology development and could lower future spacecraft signal processing complexity. In TDI, the signal-to-noise ratio is increased by the factor \sqrt{N} , with no increase in bandwidth, over that of an individual detector element, where N is the number of detector elements in the TDI subarray. Since the performance improvement is proportional to the square root of subarray length, relatively small gains are achieved by using numbers of detectors greater than about 30. Therefore, the requirements for an InSb CCD to perform TDI on the focal

plane are not severe, in that the number of required bits is small; consequently, transfer efficiency need not be exceptionally high.

To successfully produce a monolithic InSb infrared imaging device, development of a high yield MIS technology in this material is required. Current status of InSb MIS development is discussed in this paper. A process technology for producing multi-layer metal-insulator structures on InSb is described in Section II. Section III describes several relevant interface properties that have been determined from the fabrication of InSb MOSFETs and MIS capacitors. An InSb CCD has been designed and fabricated, with results reported in Section IV. Other devices for infrared applications utilizing MIS structures in InSb are described in Section V.

II. DEVICE FABRICATION

A process technology has been demonstrated for fabricating multilayer metal-insulator structures on InSb. This technology has enabled InSb CCDs, multi-element MIS detector arrays, MOSFETs, and other MIS devices to be fabricated on this infrared semiconductor material. Starting material for device fabrication is single-crystal, tellurium-doped InSb² with donor concentration of $4 \times 10^{14}/\text{cm}^3$ to $1 \times 10^{15}/\text{cm}^3$. All the devices reported in this paper are wafer-processed using standard photolithographic techniques. The wafers are 2.5 to 3.8 cm in diameter, yielding approximately 80 to 120 chips per wafer for a typical die size.

Figure 1 shows an overall view of one of the InSb test chips processed in this work. This chip, which is 2.4 mm square, contains a number of exploratory devices including: MIS capacitors; MOSFETs of various geometries; test devices utilizing substrate injection readout, including a linear and an area array; and a four-phase (4Φ), overlapping-gate CCD.

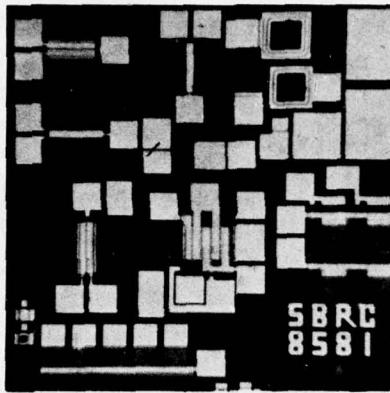


Figure 1. InSb MIS Device Chip

The fabrication sequences for a MOSFET and a four-phase CCD are useful to illustrate the materials that have been used. A photomicrograph of an InSb MOSFET on another test chip is shown in Figure 2. This MOSFET is a closed-geometry device with a channel length $L = 20 \mu\text{m}$ and $W/L = 50$. W/L on other devices fabricated has ranged from 0.3 to 100. The MOSFET source and drain regions are formed by cadmium diffusion, followed by deposition of a gate insulator approximately 1500 \AA thick. Both alumina (Al_2O_3) and silicon monoxide (SiO) have been used successfully as gate insulators in the InSb MIS devices processed in this laboratory. The higher dielectric constant ($K = 8$) of the former is advantageous for charge storage devices such as CCDs, since storage capacity for a given oxide thickness is increased. The Al_2O_3 is deposited by electron-beam evaporation, while the SiO is thermally-evaporated. Evaporation and delineation of the gate metal and subsequent formation of contacts to the source and drain regions complete the structure. Aluminum is used for the metal layers on Al_2O_3 devices. Titanium or titanium-gold metallizations are used on the SiO devices.

A photomicrograph of a four-bit, four-phase InSb CCD is shown in Figure 3. Test results for this device are given in Section IV. The InSb CCD makes use of an

overlapping-gate, stepped-oxide structure. SiO was used for all the dielectric layers in the structure. Titanium was used for the channel stop and buried gate metallizations, and titanium-gold for the surface metal layer. Three insulator levels and three metallizations are used in this InSb CCD design. A four-phase clock layout was used to provide maximum flexibility in clocking the device. Due to the present unavailability of a proven process to either implant or diffuse n^+ layers into n-type InSb, a "channel stop" metallization was used on this device to confine the charge to the channel region. This channel stop metallization consists of a buried gate which bounds the CCD channel, deposited on top of the gate insulator (thin oxide). This metallization is in turn insulated with a thick oxide, which supports the bonding pads for the CCD gates. By appropriately dc-biasing the channel stop metallization with respect to substrate, the surface potential in the region surrounding the channel may be independently controlled.

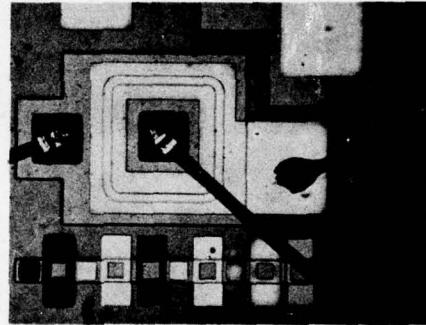


Figure 2. InSb MOSFET ($W/L = 50$)

The CCD of Figure 3 has a channel 0.94 mm long by 0.20 mm wide, with an input and output diffusion at either end of the channel. The device has an overlapping pair of input gates to provide flexibility for various electrical input schemes. The CCD bit length is $200 \mu\text{m}$. The gate lengths and other dimensions on this device are consequently larger than those found in typical

silicon CCDs. The combination of dimensions, tolerances, and multilayer requirements of the CCD was, however, heretofore unproven on InSb, thereby motivating this conservative first mask design. A new mask set currently being processed incorporates 25- μm gate lengths; future designs will incorporate 13- μm or less gate lengths. Fabrication of a nine-bit linear imager with lateral transfer from MIS detectors into a CCD readout register is also underway at the present time.

Figure 4 shows a scanning electron micrograph of one section of the four-bit InSb CCD. This photograph clearly illustrates the delineation capability that has been achieved on these devices.

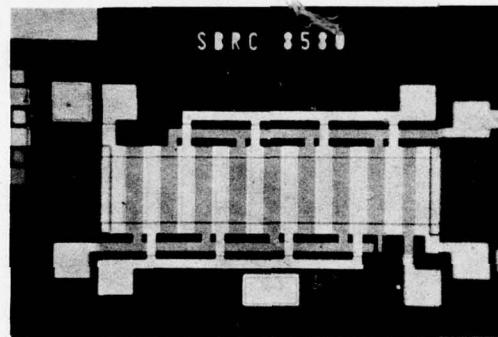


Figure 3. Four-Bit, Four-Phase InSb CCD

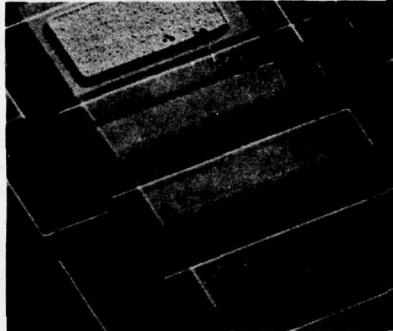


Figure 4. Detail of Four-Phase InSb CCD
(200 \times SEM, Backscatter Mode)

III. InSb MOSFETs AND MIS CAPACITOR MEASUREMENTS

The principal test structures that have been used for process evaluation and measurement of MIS characteristics are InSb MOSFETs and MIS capacitor structures. These devices have been included on each CCD chip design that has been produced.

The MOSFETs generally follow ideal FET behavior, with square-law and linear characteristics in the saturation and low-drain-voltage regions, respectively. An output characteristic for an InSb MOSFET with Al_2O_3 insulator is shown in Figure 5. These characteristics and all other data presented in this paper were obtained at 77°K. The Al_2O_3 -InSb FETs operate as p-channel, enhancement-mode devices with a threshold voltage of about -5 volts. Threshold voltages of the SiO devices are similar.

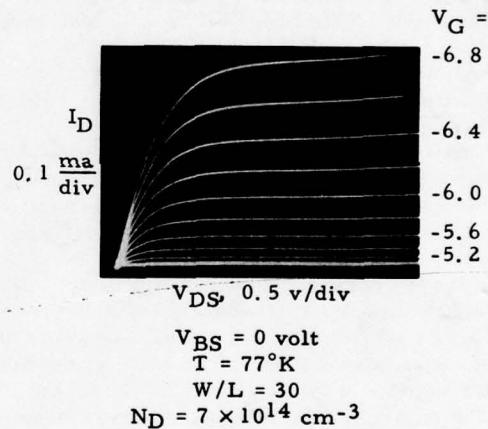


Figure 5. InSb MOSFET Output Characteristics

The effective inversion layer mobility of holes may be determined from a measurement of the channel conductance $g_D = \delta I_D / \delta V_D$ in the linear region. A plot of g_D versus $(V_G - V_T)$ should be linear in the ideal case with slope $\beta = (W/L) C_0 \mu_p^*$, where C_0 is the insulator capacitance per unit area and μ_p^* is the effective hole mobility.

Curve A in Figure 6 shows a plot of this type for the device of Figure 5. An effective mobility of about $500 \text{ cm}^2/\text{volt}\cdot\text{sec}$ is obtained. Curve B in Figure 6 shows a similar plot for an SiO-insulator InSb MOSFET, with a typical value of mobility observed with this dielectric material. The observed effective mobilities are comparable to silicon MOS devices; consequently, these InSb transistors display the same transconductances as silicon MOSFETs of the same geometry. As a result, charge transfer in an InSb CCD will be comparable to that of a silicon CCD, of similar geometry, if other factors such as interface state density are also comparable.

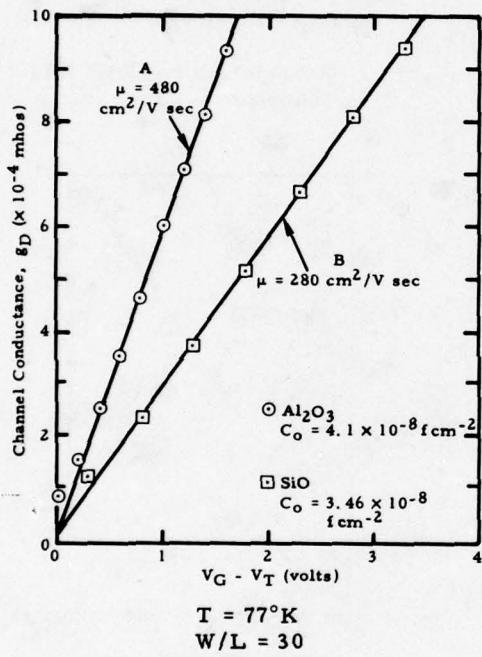


Figure 6. InSb MOSFET Channel Conductance in Linear Region Versus Gate Voltage

Pulsed MIS capacitor (C-t) measurements have been used to investigate the non-equilibrium characteristics of the InSb MIS samples. The storage time is a particularly important parameter for charge

transfer devices. Since the pulsed MIS capacitor measurement is sensitive to minority carrier generation from all sources, a 0° FOV (dark) storage time test is an effective measure of overall device quality. The dark current is given approximately by³

$$J_G = qn_i \left(\frac{n_i L_p}{N_D \tau_p} + \frac{W_d}{2 \tau_p} + \frac{s}{2} \right)$$

where the first term is the leakage current due to minority carriers generated in the neutral bulk which diffuse to the surface depletion region, the second due to carriers generated in the depletion region of width W_d , and the third due to generation at the surface with surface generation velocity s . n_i is the intrinsic carrier concentration, N_D the impurity concentration, L_p the diffusion length, and τ_p the minority carrier lifetime. The storage time T_s is proportional to the charge capacity and inversely related to the average dark current; i.e., $T_s \approx C_0 \Delta \phi_s / J_G$ where $\Delta \phi_s$ is the difference in full and empty well surface potentials. Using the representative 77°K values:

$$\begin{aligned} N_D &= 10^{15}/\text{cm}^3 \\ n_i &= 2.7 \times 10^9/\text{cm}^3 \\ \tau_p &= 0.1 \mu\text{sec} \\ \mu_p &= 9 \times 10^3 \text{ cm}^2/\text{volt}\cdot\text{sec} \\ L_p &= 25 \mu\text{m} \\ \epsilon_s &= 1.5 \text{ pf/cm} \\ C_0 &= 3 \times 10^{-8} \text{ f/cm}^2 \\ \Delta \phi_s &= 2.5 \text{ volts} \end{aligned}$$

the estimated dark current components at 77°K are:

$$\begin{aligned} J \text{ (diffusion)} &= 0.03 \text{ na/cm}^2 \\ J \text{ (depletion region)} &= 300 \text{ na/cm}^2, \text{ average} \\ J \text{ (surface)} &= (0.2)(s) \text{ na/cm}^2 \end{aligned}$$

where s is in units of cm/sec . The generation in the depletion region clearly dominates the diffusion component at this temperature, similar to the InSb p⁺-n photodiode case. For sufficiently low s , the expected bulk-limited storage time is on the order of 0.25 sec.

Experimentally, InSb MIS storage times of up to 0.5 sec have been measured at 77°K. Figure 7 shows the measured small-signal capacitance of an InSb MIS sample in response to a -5V step on the gate. The observed storage time for this sample is about 0.4 to 0.5 sec. By the above calculation, this magnitude of storage time indicates that the dark current is dominated by bulk rather than surface generation centers. To investigate this further, a modified Zerbst model^{4, 5} was used to analyze the C-t data for several samples. A Zerbst plot tests the relationship between the inversion layer formation rate and the depletion region width. A linear region on the plot corresponds to bulk generation, where the time rate of change of the inversion layer density is given by $\frac{dp_g}{dt} = n_i (W_d - W_{df})/\tau_g$. In this expression, W_d is the depletion region width at a given time, W_{df} its final value, and τ_g , the effective generation lifetime. τ_g is obtained from the slope of the linear region and τ_g , the bulk generation lifetime, is extracted from the result. When the C-t response is primarily surface-dominated, the Zerbst plot is markedly nonlinear over its entirety. Figure 8 shows such plots for two InSb MIS samples. Curve A is for the C-t trace of Figure 7; Curve B is a plot for another sample with twice the substrate impurity concentration. The linearity of the plots corroborates the conclusion drawn from the storage time magnitude that the C-t response is bulk dominated. From the slopes of the curves, a bulk generation lifetime of about 0.2 μ sec is obtained for both samples. Relating this result to hole lifetime requires more detailed knowledge of the generation centers; for the case of equal electron and hole lifetimes and generation centers at midgap, $\tau_p \approx \tau_g/2 \approx 0.1 \mu$ sec. From the intercept of the Zerbst plot, the surface generation velocity s may also be calculated; the result is typically 20 cm/sec or lower.

The bulk limited dark current observed in InSb at 77°K contrasts to the room temperature silicon case, where surface generation normally dominates. This is due to the longer lifetimes in the latter material. The measured InSb storage times

are, however, more than adequate for moderate clock frequencies and the CCD applications considered for these devices.

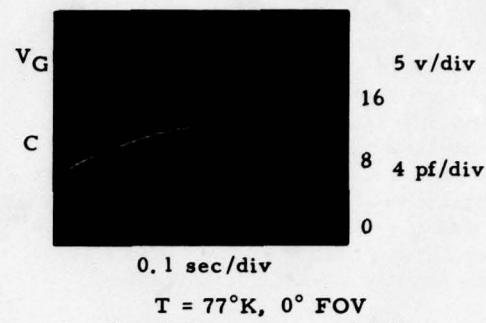


Figure 7. Storage Time of InSb MIS Sample

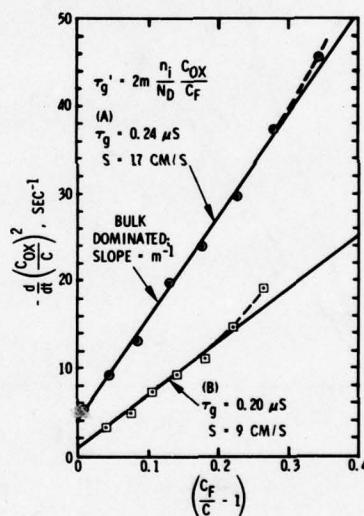


Figure 8. Thermal Generation Parameters from Pulsed InSb MIS Device Transients

The MIS conductance technique⁶ has been used to determine interface state density using InSb MIS capacitors. Representative curves of equivalent parallel conductance G_p/ω versus frequency obtained by this technique are shown in Figure 9, for two values of gate bias. For both curves (A) and (B), the sample is biased such that the surface is depleted. The data were fitted reasonably well by the equivalent parallel conductance for an interface state continuum (broken curves in Figure 9). A deviation from the theoretical curve is observed at low frequencies due to the influence of minority carrier transitions, in addition to the majority carrier transitions on which this model is based. The minority carrier response, usually negligible in silicon devices, appears at low frequencies in InSb due to higher generation-recombination rates. Using $N_{ss} = 2.5$ (G_p/ω)_{M/q}, the interface state density was calculated from the peak value (G_p/ω)_M of the equivalent parallel conductance curve. From curve (A), an $N_{ss} = 1.4 \times 10^{12}/\text{cm}^2\text{-eV}$ is obtained, while curve (B) yields, for N_{ss} near midband, a value $6.2 \times 10^{11}/\text{cm}^2\text{-eV}$. The results of conductance measurements agree with densities as determined by a high-frequency capacitance-voltage technique.

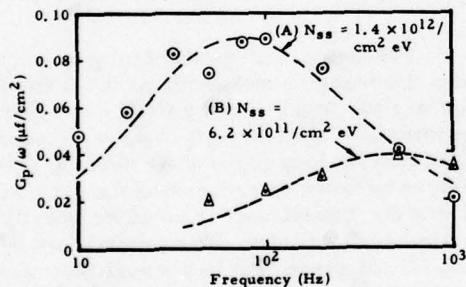


Figure 9. Equivalent Parallel Conductance Versus Frequency for InSb MIS Sample

IV. InSb CCDs

The 4ϕ overlapping-gate InSb CCD (Figure 3) has been successfully operated with three different clocking modes. These modes are: (a) conventional 4ϕ clocking; (b) 4ϕ clocking with storage only under the buried gates; and (c) simulated 2ϕ clocking. Mode (a) results in four transfers per bit while both modes (b) and (c) produce two transfers per bit. Electrical input was achieved by several techniques: the signal was applied to one of the input gates or input diffusion, with the other two input terminals appropriately biased. The device output was obtained through use of the conventional precharge (or reset) circuit, except that the output circuit elements, with exception of the output diode, were not integrated on-chip as is the case in most silicon CCD structures. The circuit was built up in discrete form using silicon FETs and interconnected to the InSb output diode by means of wire bonding. This resulted in a functioning circuit sufficient to observe device operation, but the large output circuit capacitances resulted in a low output responsivity (15 mv/pC) and increased reset clock feedthrough.

Figure 10 shows input and output waveforms for the four-bit CCD clocked at 5 kHz, with a sine wave input signal. The simulated 2ϕ clock mode (c) was used in this case, and the signal was applied to the buried input gate. Input and output waveforms using clock mode (a) and a square-wave input are shown in Figure 11. (Note that the output waveform is inverted with respect to the input waveform on all oscilloscope photographs.)

Measurement of the transfer efficiency for the device was carried out in all three clocking modes. The results for the efficiency per transfer η , at a clock frequency of 5 kHz, ranged from $\eta = 0.82$ to 0.92 depending on the clock mode, fat zero level, and measurement technique used. The best measured efficiencies were obtained for those devices operated in mode (a), but the results for the other modes were not significantly different. For simplicity, only

the 4 ϕ clock results are discussed here. Two principal methods were used in computing the transfer efficiency from the output data. In method (1), the magnitudes (B) of the first output pulse and the maximum value (A) of the signal output were measured. η was then computed from $\eta = (B/A)^{1/N}$, where N is the number of transfers. For mode (a), four transfers per bit result in N = 16. Method (2) utilized the sum of the charge deficits in the leading signal outputs (S_L) or the sum of the trailing signals (S_T) to estimate the efficiency. In this approach, the sums are related to the inefficiency ϵ by:

$$S_L = S_T \approx \frac{N\epsilon}{1 - \epsilon}$$

By measuring either S_L or S_T and inverting, the inefficiency ϵ ($\eta = 1 - \epsilon$) may be readily computed.

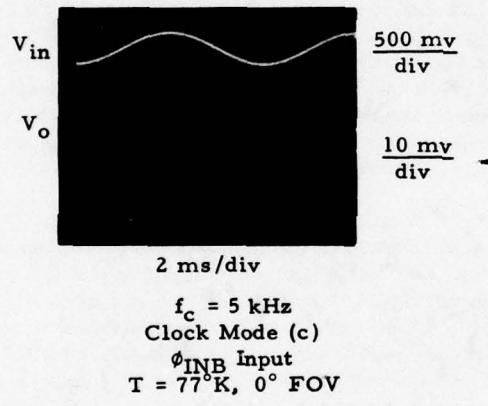


Figure 10. InSb CCD Output Waveform

In Figure 11(a), the device was operated without a fat zero while in Figure 11(b) a fat zero of approximately 50% of saturation was used. From the output signal of Figure 11(a), the efficiency per transfer is computed as $\eta \approx 0.886 \pm 0.006$ using method (1), while application of method (2) yields $\eta \approx 0.854 \pm 0.01$. Similarly, the results with fat zero [Figure 11(b)] are $\eta \approx 0.919 \pm 0.009$ as determined by method (1) and $\eta \approx 0.880 \pm 0.01$ using the leading and trailing sum approach. Although the alternate

methods yield slightly different results, an average of several measurements showed that $\eta \approx 0.90$ was typical of the device when operating in the conventional 4 ϕ clock mode.

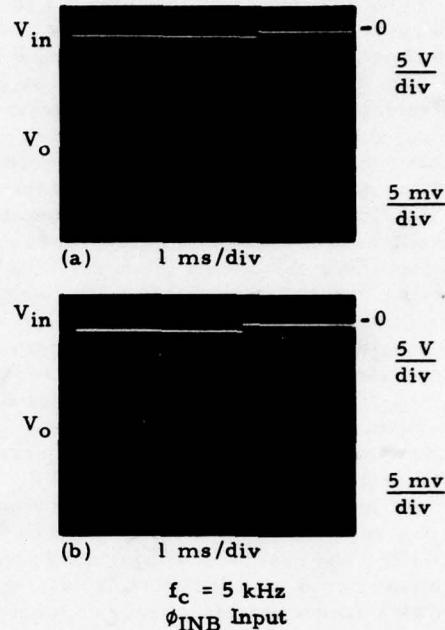


Figure 11. Output Waveform, Clock Mode (a)

The two principal mechanisms which limit the transfer efficiency of the InSb device are the lengths of the CCD gates and the interface state density. As mentioned in Section II, long gates were used on these devices because of processing uncertainties on this first mask set. Computer calculations, based on a two-dimensional model with 50- μm gates, predict a negligible tangential field in the gate centers and a field of approximately 1000 v/cm at the gate edges. For this gate length, therefore, the fringe field coupling between the gates is small. As a result of these small fields, the transfer through the device relies principally on diffusion.

The gate length also increases the impact of interface states on the device efficiency. To examine this dependence, the effects of interface states were treated using the model proposed by Lee and Heller.⁷ The basic assumptions of this model are instantaneous charge redistribution during the transfer period and the use of an effective time constant (τ_s) to describe the effects of interface states. Using the Lee and Heller model, the constant τ_s was determined by fitting the model predictions of transfer efficiency to $\eta \approx 0.90$, the measured value for the present InSb structure at 5 kHz. Assuming the same clock rate and conventional 4 ϕ operation, the efficiencies predicted for future devices with various gate lengths were calculated. The results are shown in Table 1. The well depth used in the calculation is also shown in Table 1. It represents the ratio of the charge stored to the capacitance of the storage well. The well depth observed in operating the present device was ≈ 0.5 volt, so this value was used in fitting the measured efficiency. For the remaining cases of 25- μm , 13- μm and 7.5- μm gate lengths, a well depth of 2 volts was assumed, since this value has been observed on InSb discrete devices and is expected to be realized on future CCD structures. A significant decrease in interface state loss with decreasing gate length is evident in the Table.

Table 1. Calculated Transfer Efficiency Versus Gate Length for InSb CCD

GATE LENGTH (μm)	WELL DEPTH (volts)	INTERFACE STATE LOSS	EFFICIENCY (η)
50	0.5	9.36×10^{-2}	0.90
25	2.0	9.64×10^{-3}	0.990
13	2.0	2.51×10^{-3}	0.997
7.5	2.0	9.11×10^{-4}	0.999

$f_c = 5 \text{ kHz}; \tau_s = 5 \times 10^{-6} \text{ sec};$
NO FRINGE FIELD; 4 ϕ CLOCK MODE (a)

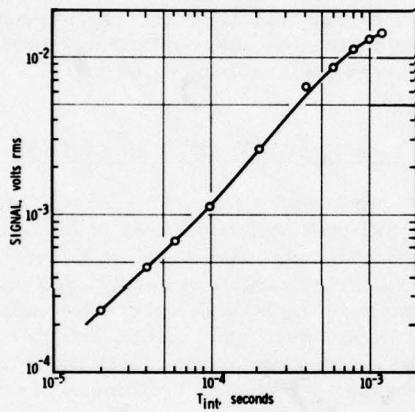
In summary, CCD operation has been achieved on an InSb substrate. Analysis of the device structure indicates that the transfer efficiency is limited by the gate length as well as by interface state trapping. From Table 1, an efficiency of $\eta = 0.99$ or better is predicted, even with the present interface state density, for InSb CCDs with gate lengths of 25 μm or less. Although these predictions are necessarily qualitative, they represent reasonable extrapolations from the performance of the first devices reported here. Further, fringe field coupling will also enhance transfer in future devices with decreased gate lengths, an effect which has not been included in the calculations leading to Table 1. The efficiency values projected in the Table will be more than adequate for a number of system applications of these InSb CCDs. Investigation of processing variations to reduce interface state densities is also continuing, and future improvements are anticipated.

V. InSb MIS DETECTOR ARRAYS

Other devices for infrared applications utilizing MIS structures in InSb have been fabricated. The interface properties and multilevel structure capabilities demonstrated in the InSb CCDs are also applicable to the fabrication of MIS detector arrays using approaches other than CCDs for readout. Two such techniques are the detection of signal charge by sensing voltage change on an element or line capacitance, or the injection of signal charge into the substrate and detection of the displacement current by various circuit approaches.

Single-element InSb MIS detectors utilizing substrate injection readout were fabricated and tested prior to processing of multielement arrays. The single-element device has a 125- μm square active area defined by a semitransparent titanium gate approximately 50 \AA thick. Infrared testing was accomplished using chopped blackbody radiation input and a cold FOV restriction to reduce background photon flux to 2×10^{14} photons/sec- cm^2 , a typical level for a 3- to 5- μm infrared system. Figure 12 shows

the dependence of output signal on integration time for a representative device, for a constant incident blackbody irradiance. The output signal is approximately linear with integration time as expected for an integrating detector, until a saturation point is reached which is dependent on the total incident photon flux and the storage capacity of the device. For the example shown in Figure 12, saturation occurs at about 1 msec, consistent with the background flux and clock level used. The MIS detector shows the typical InSb spectral response, identical to that of a photovoltaic InSb detector. Relative response per photon is nearly flat over the spectral band characteristic of an ideal quantum detector, with the intrinsic InSb cutoff at 5.4 μ m.



$$T_{BB} = 500^\circ K$$

$$H_{BB} (\text{rms}) = 7.1 \times 10^{-6} \text{ watts/cm}^2$$

$$T = 77^\circ K$$

$$Q_B = 2 \times 10^{14} \text{ phot/sec cm}^2$$

$$A_D = 1.6 \times 10^{-4} \text{ cm}^2$$

Figure 12. Output Signal Versus Integration Time for InSb MIS Detector

Five-element MIS detector arrays also have been designed and fabricated; one such array is shown in Figure 13. Device processing techniques are similar to those used in the InSb CCDs: insulator layers are SiO; all metal levels, including the transparent gates, are titanium. Each element

(or unit cell) of the array consists of a pair of overlapping transparent gates: an X gate on the buried metal level, and a Y gate of equal area on the surface metal level. Each gate is $125 \times 125 \mu\text{m}$. The X gates are interconnected with a buried metal clock line, terminating in a bonding pad which is positioned over a channel stop or ground plane metallization and its associated thick oxide. This latter metallization level ensures that no infrared sensitivity or other spurious effects are obtained in the bonding pad region. In a full two-dimensional array of these devices, the Y gates would be similarly interconnected by a pattern of clock lines (on the surface metal level) at right angles to the X clock lines. On this linear array, the Y lines were eliminated and contact was made directly to the Y gates by wire bonding.



Figure 13. 5-Element InSb MIS Detector Array

The correct mode of operation of the unit cells in the linear arrays has been observed; i.e., the transfer of stored charge from the X gates to the Y gates and subsequent charge injection readout has been obtained. A clear demonstration of unit cell operation was obtained by infrared spot scanning of the device. Figure 14 shows a contour plot of one unit cell of a five-element array. In Figure 14, both X and Y clocks are running, and the full $125 \times 125 \mu\text{m}$ area is photosensitive as shown. In Figure 14(B), the X gate is grounded, disabling this half of the cell, as confirmed by

the resulting spot scan. Spectral response and other characteristics of the arrays are similar to those of the single-element devices.

focal plane assembly complexity, reduced sensor power and weight requirements, and improved performance.

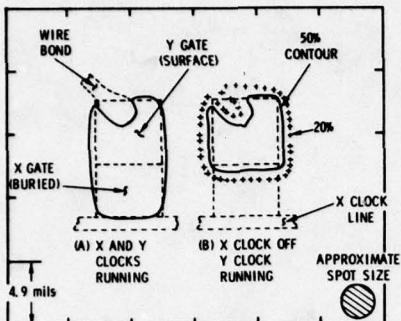


Figure 14. Spot Scan of InSb MIS Array Unit Cell

VI. CONCLUSIONS

An InSb MIS technology for the fabrication of monolithic InSb infrared imaging devices is under development. The insulator-InSb interface properties as determined from MOSFET and MIS capacitor structures have been found to be favorable for the fabrication of CCDs and other charge storage devices in this material. A process technology for producing the required multi-layer metal-insulator structures on InSb also has been demonstrated, a second requirement for realization of the monolithic infrared imaging device. Third, the principal component of a CCIRID, an InSb charge-coupled device, has been fabricated and successfully operated. Finally, InSb MIS detectors have been produced which are suitable for fabrication of two-dimensional arrays using other approaches for readout. The demonstration of charge coupling in InSb offers the potential of a future generation of 1- to 5-μm monolithic infrared imaging devices with significant reduction in

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*A CCD MULTIPLEXER WITH FORTY AC COUPLED INPUTS

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ABSTRACT The performance of a buried channel CCD multiplexer with forty floating diffusion inputs 1, 2 is described. Features include: (1) Single-stage, low noise preamplifiers fabricated on the CCD chip and interfaced with each input at a nominal power of 25 μ W per channel; (2) ac coupling between preamps and CCD on the monolith with low frequency response adequate for slow scan FLIR applications; (3) CCD input bias maintained by periodic reset (dc restore) with measured sag rate of 166 μ V in 8.3 msec.; (4) anti-aliasing characteristics of the combined preamp-CCD input measured to be excellent and adequate for FLIR applications.

Overall ac dynamic range of 50 dB was measured. Ac coupling suppressed by 20 dB dc input variations such as would result in a direct coupled system from average background temperature changes, detector bias non-uniformities, and cold finger temperature fluctuations. Frequency response data on ac coupling circuitry is presented. Channel-to-channel crosstalk due to CCD CTE was measured to be less than -40dB at the 4 MHz output data rate.

I. INTRODUCTION

Charge coupled devices (CCD's) have been recognized as a potential means of performing signal processing functions in HgCdTe FLIR systems, for example: multiplexing, delay-and-add, data storage, and scan conversion. In recent months, increasing interest has been directed toward integration onto the same monolith of, not only the CCD's and their driver electronics, but also the interface circuitry between the HgCdTe detectors and the inputs to the CCDs. Total integration of the interface circuitry would make placement of the signal processing electronics on the focal plane an option available to the system designer.

A number of requirements on the CCD and its interface circuitry in an 0.1 eV HgCdTe system result from characteristics common to many IR detector-array systems.

(1) The detector noise bandwidth exceeds the required video bandwidth, a condition that can produce undesirable aliasing of high frequency noise in a sample-data system.

(2) The dynamic range requirements at the detectors (focal plane) is severe in 8 to 14 μ m systems because of ambient background variations, detector non-uniformities, and "cold-finger" temperature fluctuations, in addition to the variations in irradiance associated with the viewed scene. Non-uniform response to the background also represents coherent or "fixed pattern" noise at the detector array which is large relative to "signal" because of the low contrast in real scenes.

(3) The charge transfer inefficiency (CTI) of a CCD is a potential source of image MTF degradation, an effect which in a multiplexer system is referred to as channel-to-channel crosstalk.

Techniques to circumvent the first two problems outside the detector/dewar are relatively straightforward; for example: RC filtering and ac coupling. However, the large coupling capacitors, necessary for low frequency response as well as for band-limiting of detector noise, are not

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compatible with either monolithic integration or physical placement within the dewar. The device described in this paper is a 40 input buried channel multiplexer designed specifically for compatibility with slow scan FLIR applications. It incorporates input circuitry which, together with its low CTI, represents viable solutions to the three problems listed above.

II. MULTIPLEXER DESIGN

A. Buried Channel CCD for Basic Shift Register

The basic functional design of the 40 input multiplexer is illustrated in block diagram form in Figure 1. The nucleus of the multiplexer is a 40-stage four-phase poly-Si/Al shift register fabricated by conventional ion-implant buried-channel processing. Simultaneous parallel inputs are made to each stage via 40 floating diffusion inputs 1, 2 each of which is preceded by a single stage MOSFET preamp which is ac coupled to the control gate of the floating diffusion input. A more detailed schematic is shown in Figure 2. The floating diffusion inputs and preamplifiers were masked from the ion implant to maintain surface channel characteristics.

The interchannel crosstalk due to charge transfer inefficiency, ICR, is defined as the ratio of the amount of charge that is lost into the primary packet by other charge packets to that of the primary charge packet when measured at the output. Since inputs are made to every stage, the interchannel crosstalk can be written as

$$ICR = k\epsilon + \frac{[k\epsilon]^2}{2!}$$

where the first term is due to the charge packet initially at position $k - 1$ and the second term is due to the charge packet initially at position $k - 2$. Epsilon, ϵ , here denotes the fractional loss per stage and is equal to the loss per transfer, CTI, times the number of phases.

B. The Floating Diffusion Input as an Anti-Aliasing Filter

The structure of the floating diffusion (FD) input is shown in Figure 3. In simple terms, the technique involves first setting the intermediate node to a voltage dependent on the signal voltage applied to the first

transfer electrode, then setting it to a second level dependent on a reference pulse applied to the second transfer electrode. The second process is accomplished through transfer of charge into the receiving CCD well; as such, the charge introduced is derived from the difference in the two preset levels multiplied by the capacitance of the floating node and is insensitive to threshold voltage (V_T) to the extent that V_T is the same under the closely spaced electrodes.⁴ The noise characteristics of this input are known to be approximately described by kTC_2 ,⁵

The first process in the two step sampling operation of the floating diffusion input is essentially the "fill-and-spill" or "potential equilibration" 1, 6, 7, 8 procedure applied to a diffusion instead of a CCD or MIS node. This process is initiated by pulsing the input diode negatively (for an N channel CCD) to introduce excess charge onto the diffused node and then returning it to a high positive value to extract charge from the node while the channel current is controlled by the signal voltage applied to the input gate (V_{g1}). The process is terminated by the pulsing of the second gate, which, for a multiplexer, is the serial-parallel transfer electrode. It can be shown that for noise, the time interval associated with the first process constitutes an effective integration time, τ , and the input acts to band limit the noise.^{9, 10} Details of this analysis are contained in another paper at this conference listed here as reference 10. The band-limiting effect approaches the $\sin X/X$ of an ideal integrator where $X = \pi T_c/\tau$ and T_c is the reciprocal of the input data rate.

C. Monolithic AC Coupled Preamplifier for Background Suppression

Because of the impracticality of introducing large discrete coupling capacitors into the dewar, focal plane processing of HgCdTe photoconductor signal is usually associated with a direct-coupled system. The severe dynamic range requirements on the CCD and any interface circuitry due to background radiation, together with the "fixed pattern" noise, were identified in Section I. Because of the very high impedance associated with the gate of a monolithic MOSFET, however, it becomes feasible to achieve acceptable low-frequency

time constants allowing ac coupling on-chip. A proposed structure, shown in Figure 4, relies on periodic reset techniques to maintain bias stability. System considerations for the reset are similar to those associated with dc restore techniques in FLIR systems. One might set the dc bias level prior to each sweep of the IR scan mirror and then allow ac variations about this dc level; therefore, it is desirable for this level to change less than, say, several gray shades; for the 30 frame-per-second 2:1 interlace FLIR with nominal gain between detector and this point of 1500, the required sag is 300 μ V in 8.3 msec assuming 50% scan efficiency. From a design standpoint, a capacitor value of 2 pF is required based on a diode leakage current of 10 nA/cm² and a typical source drain diffusion area of 4×10^{-6} cm². This value is the total capacitance to ground of the input node; that is, C is C_{couple} (Fig 4) in parallel with the FD input gate capacity, the MOS reset drain capacity and the stray capacity. We selected $C_{couple} = 2$ pF and had planned to hold other capacities ≤ 0.2 pF to avoid attenuation in a capacitive voltage divider.

In the final design, a preamplifier with a design gain of six preceded the coupling capacitor. An overall gain of at least four between preamp input and FD input gate was desired after the divider attenuation mentioned in the preceding paragraph. The preamplifiers were of a single stage MOSFET design, as shown in Figure 2, where the W/L ratio of the drain load MOSFET was planned to be 1/6 that of the active input MOSFET.

III. EXPERIMENTAL RESULTS

Provisions were made by metal mask variation to separate the multiplexer with its 40 FD inputs from the ac coupled preamps for independent evaluation of the multiplexer. Characteristics of the preamplifiers and ac coupling were inferred by comparing the combined operation with that of the multiplexer by itself.

Table I
Buried-Channel Multiplexer
With Floating Diffusion Inputs

CTE (@ 4 MHz)	0.99996
Crosstalk (Worst-case)	-44 dB
Output Capacitance	0.24 pF
Source Follower Gain	0.5
Overall Gain	1
Noise (100 kHz input rate)	
Output Spot Noise	1.85 μ V/ $\sqrt{\text{Hz}}$
Output Wideband Noise (50 kHz)	0.41 mV
Maximum Output Swing (P-P)	0.15 V
Dynamic Range	51 dB
Low Frequency Noise Corner	500 Hz
Equivalent Input Spot Noise	1.85 μ V/ $\sqrt{\text{Hz}}$
Wideband Input Noise (50 kHz)	410 μ V

A. Buried Channel Multiplexer With Forty Floating Diffusion Inputs Only

Data presented in Table I summarizes the results obtained on the device of Figure 2 without the ac coupled preamplifiers; inputs were directly to the first gates of the FD inputs.

The CTE was measured to be at least 0.99996 at 4 MHz output data rate (which corresponds to an input data rate of 100 kHz) with a corresponding -44 dB crosstalk measured for the input farthest from the output end. The design goal of 40 dB isolation was achieved.

The output capacitance was measured to be 0.24 pF. The source follower output associated with the serial output (see Fig 2) showed a gain of 0.5. This loss value was attributed to the small value of load resistor (10K) necessary to achieve 4 MHz operation. The overall small signal voltage gain of unity, obtained by comparing the demultiplexer output rms voltage of a given channel with the rms value applied to the corresponding FD input, combined with the measured source follower gain and output capacitance, allowed calculation of an equivalent input capacitance of 0.48 pF.

Noise data were taken. An output spot noise (spectral intensity) of 1.85 μ V/ $\sqrt{\text{Hz}}$ was obtained for a typical demultiplexed channel (demux sample rate equal to 100kHz) in the "white" region of the spectrum from which an rms wideband value (over the

Nyquist bandwidth) was calculated to be 0.41 mV.

A saw tooth waveform was applied to a typical channel and compared to its demultiplex output as depicted in Figure 5. The maximum peak to peak undistorted output voltage was determined to be approximately 0.15 volts from which a dynamic range of 51 dB was calculated. The system requirement was 40 dB.

By observation of the output spot noise, the low frequency ($1/f$) noise corner was determined to be approximately 500 Hz.

Table II
Buried-Channel Multiplexer With Preamps AC Coupled Using DC Bias Reset

Overall Gain	2.0
Noise (100 kHz Input Rate)	
Output Spot Noise	$2.0 \mu\text{V}/\sqrt{\text{Hz}}$
Output Wideband Noise (50 kHz)	0.46 mV
Maximum Output Swing (P-P)	0.15 V
Dynamic Range	50 dB
Low Frequency Noise Corner	1000 Hz
Equivalent Input Spot Noise	$1.0 \mu\text{V}/\sqrt{\text{Hz}}$
Wideband Input Noise (50 kHz)	220 μV
Input dc Dynamic Range	76 dB

B. Buried Channel Multiplexer With Preamps and Periodic Reset

The data of Table II characterize the buried channel device of Table I with the addition of ac coupled preamps. The preamps, coupling capacitors, and bias reset circuitry were also protected from the ion implant and therefore have surface channel characteristics.

Comparison of Tables I and II suggests that the nominal gain of the preamps, as attenuated by a possible capacitive voltage divider effect at the ac coupled node, was two.

Since output "white" noise and maximum undistorted output swing were essentially unchanged, it can be concluded that the combination of ac coupled preamplifier and bias reset circuitry made negligible contribution to the noise in the "white" spectral region. Data taken on MOSFETs of similar geometry or similar bias conditions are consistent with this conclusion and

further suggest that the slightly higher low frequency corner listed in Table II was not due to the preamp.

An extra term, Input DC Dynamic Range, has been added to Table II. It is defined as the ratio of the maximum change in DC voltage applied to the input to the preamplifier (while maintaining undistorted small-signal ac response) divided by the equivalent input wideband noise voltage.

The value of 76 dB was determined by superimposing a small sawtooth signal on a variable input dc level and recording the range over which the output waveform was essentially undistorted and the gain was substantially constant. A very important result is that the input dc dynamic range is approximately 20 dB larger than the output ac dynamic range. Another stage of preamplification with bias reset should increase input dc dynamic range even further. This "dc dynamic range" is a measure of the suppression of background effects due to the ac coupling. It is limited only by the maximum dc response of the preamplifier.

The total current drain on the preamp supply V_{DD} was measured to be 100 μA , or 2.5 μA per channel, indicating a power dissipation of 25 μW per channel.

C. Low Frequency Characteristics of AC Coupling With Bias Reset

The ac coupling with its bias reset MOSFET circuit is illustrated schematically in Figure 4 and in Figure 2 in relationship to the 40 input multiplexer. While the data for Tables I and II were being taken, the test circuitry was adjusted so as to apply a pulse (ϕ_R) to the gate of the bias reset transistors every 8.3 msec. As pointed out in Section II.C, 8.3 msec corresponds to the nominal read-in time for an entire horizontal line of parallel-scan FLIR video. During this bias reset interval, the ac components of the input signals were grounded using the set up of Figure 6 to simulate the condition of the detectors viewing a uniform background.

Using this technique one would predict that the low frequency gain suppression effects of a periodic series clamp would not be evident. Without input clamping as in Fig 6 the output signal became chopped up near the

reset rate and quickly went to zero for frequencies below the reset rate.

Using the 8.3 msec restore rate the frequency response curve of Figure 7 was obtained. The rolloff at 0.2 Hz was only -1.6 dB. The high frequency data was a smooth rolloff in $\sin X/X$ fashion to zero at 100 kHz and was limited by the sample and hold. A more detailed study is contained in reference 10 presented at this conference.

An experiment was devised to measure the sag rate directly. With the 8.3 msec reset interval the sag on the envelope of the output waveform and on the demultiplexed output was impreceivable. By increasing the interval between the bias resets to values much larger than normally required the sag rate became discernable. A typical demultiplexed waveform is shown in Figure 8. The sag rate was consistent and appeared linear in several repetitions of the experiment. An output sag rate as low as 0.02 V/sec was measured on one device. Since the slope of the sag was linear, denoting a leakage current or an RC decay with a time constant much longer than 1.3 seconds it is appropriate to interpolate the sag in an 8.3 msec interval as only 166 μ V. Even at these low restore rates a 2 Hz signal could be processed riding on the linear sag.

D. Anti-Aliasing Characteristics of the Combined Floating Diffusion-Preamplifier Circuitry

Preliminary experiments were conducted to evaluate the bandlimiting nature of the floating diffusion input in combination with the ac coupled preamplifiers. Data indicated effective bandlimiting of otherwise unbandlimited input noise with negligible resulting aliasing.¹⁰

IV. CONCLUSIONS

The performance of the 40 input multiplexer was adequate for many slow scan FLIR applications. The use of monolithic ac coupling with dc bias reset maintains good low frequency response below 2Hz. This reset, when synchronized to detector signals from a uniform background, will allow system dc restoration on a frame basis. This effectively increases dynamic range by 20 dB

by eliminating dc input variations from average background temperature changes, detector bias non-uniformities, and cold finger temperature fluctuations.

Channel to channel crosstalk was maintained less than -40 dB at 4 MHz data rate by the high CTE of buried channel design without the use of isolation inputs.

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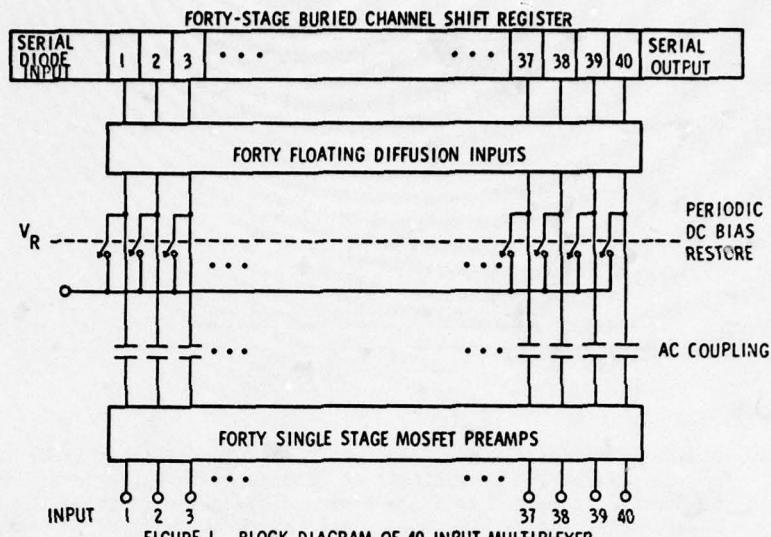


FIGURE 1. BLOCK DIAGRAM OF 40 INPUT MULTIPLEXER WITH PREAMPLIFIERS

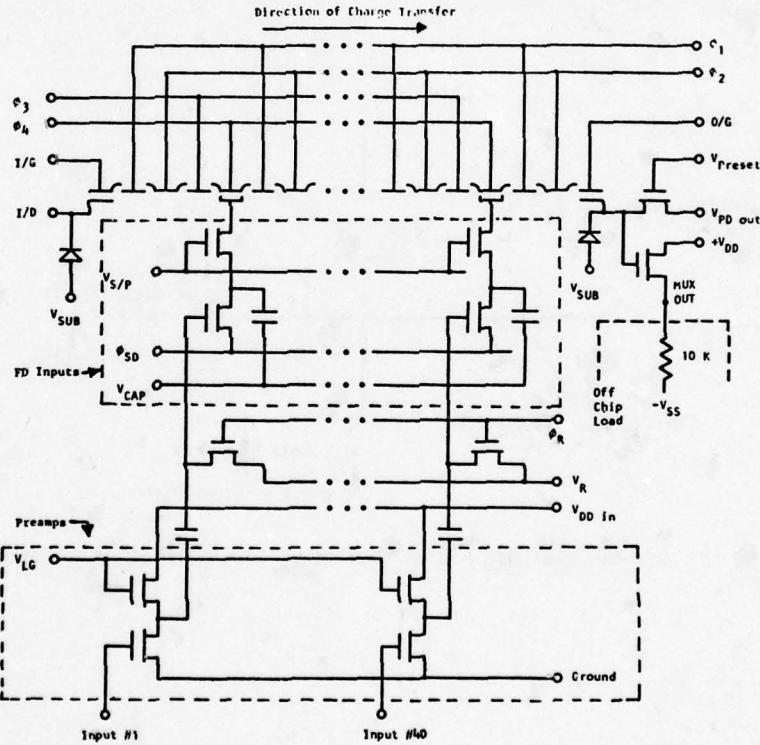


Figure 2 Schematic of Chip With Preamps, Bias Reset, and FD Input

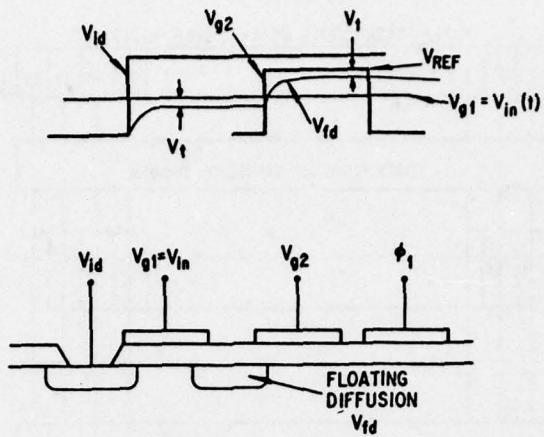


Figure 3 Floating Diffusion Input Structure Consisting of Input Diode (Connected to V_{id}), First Transfer Electrode (Connected to V_{g1}), Second Transfer electrode (Connected to V_{g2}), Floating Diffusion (Between the Two Transfer Electrodes), and ϕ_1 Electrode. The waveforms required to operate the floating diffusion are shown.

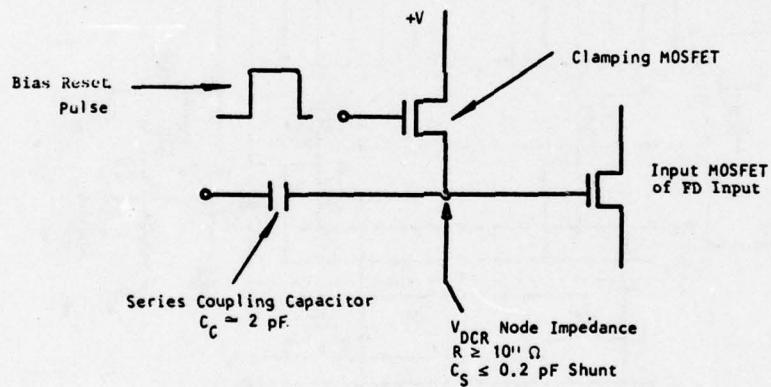


Figure 4 Schematic of AC Coupled Monolithic Node With DC Bias Reset

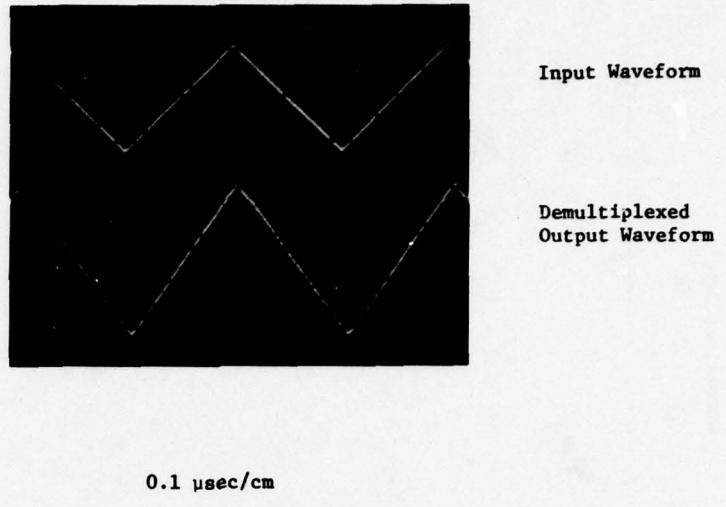


Figure 5 Typical Waveforms Used To Determine Maximum Undistorted Output Swing of Multiplexer

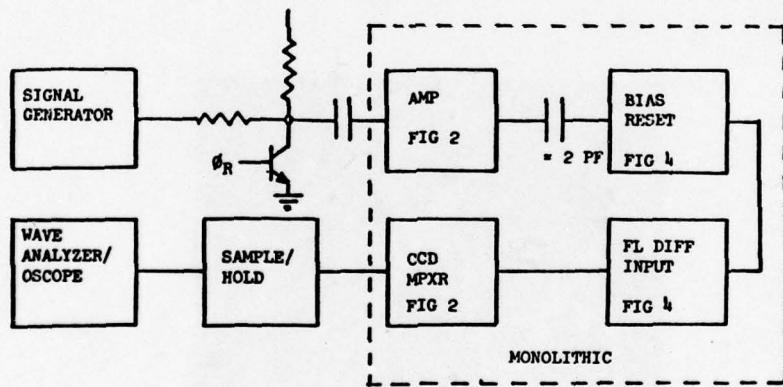


Figure 6 Block Diagram of Test Setup Showing Input Signal Clamping

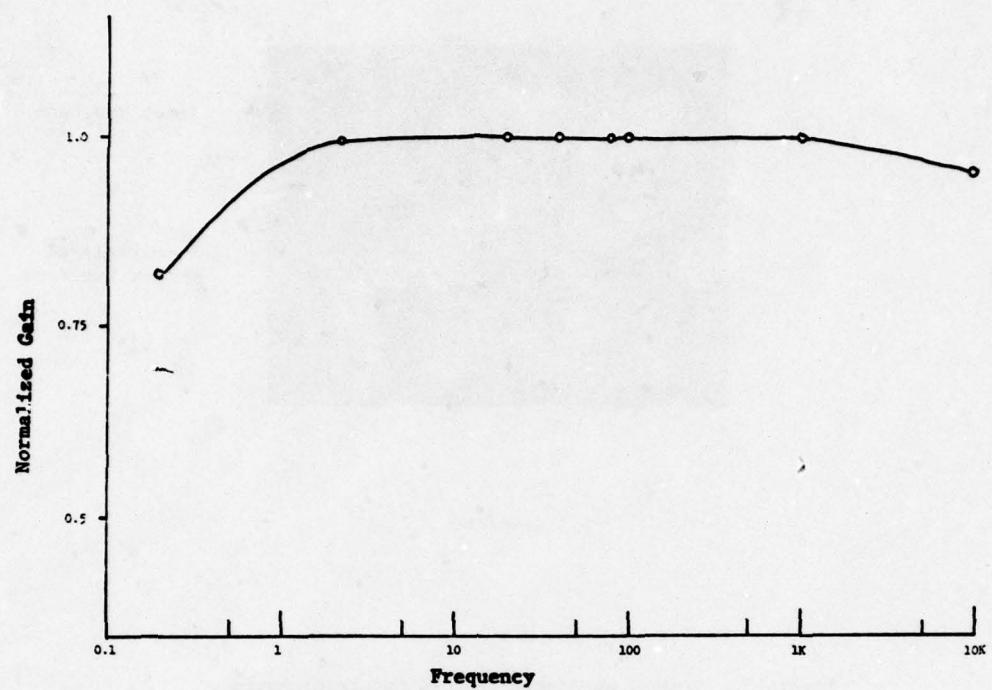


Figure 7 Frequency Response of AC Coupled Multiplexer With Bias Reset Every 8.3 msec



Figure 8 Demultiplexed Output Showing Sag Between Bias Resets

INTEGRATED CCD-BIPOLAR STRUCTURE FOR FOCAL PLANE PROCESSING OF
IR SIGNALS

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ABSTRACT The trend in thermal imaging sensor design is toward the use of high performance, low cost, integrated focal plane arrays. The hybrid marriage on the focal plane of detector mosaic with charge coupled device processor is one concept to economically achieve greater detector densities. The IR system requirements do impose severe constraints on the design of the preamplifier/CCD processor.

A monolithic CCD processor with bipolar preamplifier array was developed for use with photoconductive HgCdTe detectors.* The designs and operation of both PNP and NPN preamplifiers with P and N type surface channel charge coupled devices are described. Preliminary test results show the preamplifier gain for a PNP device at 77°K to be above 30 with greater than 1.8 megahertz bandwidth and approximately two (2) nanovolts per root Hz noise referenced to the input. Non-uniformities among preamplifiers (base-emitter voltages and bias resistors) are responsible for variation in dc bias voltages at the CCD input gates. Large differences in dc bias among input gates may compromise the CCD gain when operating in a time delay integration mode. The measured linear dynamic range using gate modulation input is 67db.

I. INTRODUCTION

The evolution of charge coupled device technology has provided momentum to the concept of focal plane signal processing in advanced FLIR systems.⁽¹⁾ Speculative systems designs with CCD's predict much greater number of detectors than contemporary technology would permit. The ability to integrate detector with signal processor on the focal plane in a single hybrid or monolithic structure permits detector densities commensurate with high performance in thermal imaging. Ultimately, the detector-processor marriage will lower system cost and improve system reliability.

This paper addresses the development of a CCD Time Delay Integration (TDI) circuit monolithic with a bipolar preamplifier array.⁽²⁾ The device is designed to operate at 77°K for direct coupling to 0.1 ev HgCdTe in a serial scan application. The basic system characteristics which impose constraints on the preamplifier-CCD design are listed in Table I.

TABLE I
Requirements Imposed On CCD/Preamp

System Spec	CCD/Preamp Requirement
Multi-row, Serial Scan, TV Compatible	Signal B.W.> 1.5MHz Out. Data Rate > 5MHz Taps per TDI > 8
8-12 μ wavelength NETD < 0.2°K	Dynamic Range > 60db
HgCdTe at 77°K	Operate at 77°K NEI < 2nV/Hz ^{1/2} Gain > 30
Dewar Heat Load <.75 watts (cold shield, radiation, bias, preamp, CCD)	3mW max per channel Min Silicon Area
Cost/Reliability	Bipolar compatible with CCD fabrication process

*Devices fabricated by Hughes Aircraft and supplied to NVL under contract DAAK02-74-C-0229.

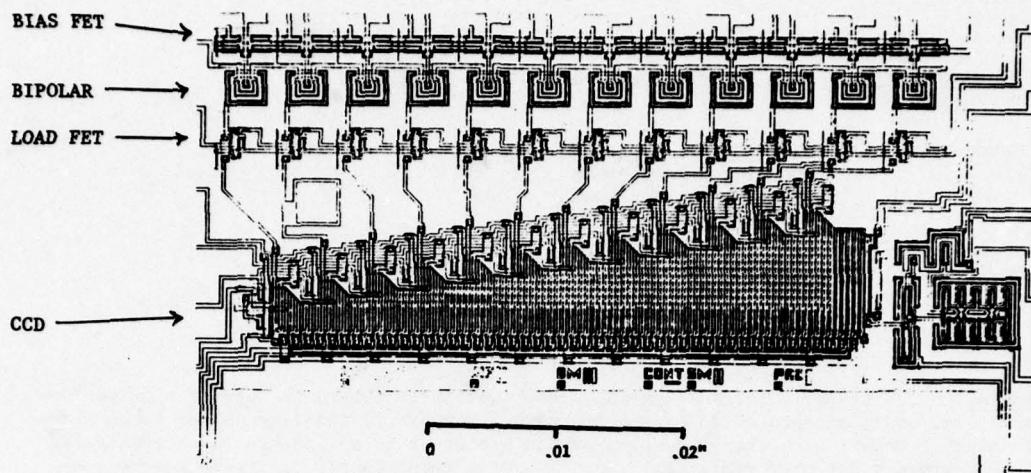


FIGURE 1
PREAMP ARRAY WITH CCD-TDI

The CCD/Preamp must interface with a mercury-cadmium-telluride detector array. Photoconductive HgCdTe, operated at background limited performance (BLIP), has a noise voltage which ranges from 4 to 8 nanovolts per root hertz. The detector bandwidth is greater than one megahertz. The impedance is normally 50 ohms but may vary from 50 ohms up to 100 ohms. A constant current detector bias is used to partially compensate for detector resistor variance.

The CCD must not limit system sensitivity, linearity, MTF, or dynamic range and must maintain detector BLIP conditions.

II. CIRCUIT DESCRIPTION

The preamplifier and CCD processor array (PAPA) is shown in Figure 1. The circuit consists of (1) a 12 input tapered CCD shift register for time-delay-integration action; (2) a MOSFET bias resistor for each detector and a MOSFET for each preamp load at the input to the CCD gates; and (3) bipolar amplifiers operating in a grounded base configuration. Devices were made using P-channel CCDs with PNP bipolars and N-channel CCDs with NPN bipolars. All CCDs were surface channel devices.

A. Charge Coupled Device: Each output of the twelve preamplifiers is directly coupled to one of the twelve input gates on the

charge coupled device. Figure 2 schematically illustrates the basic building block (1 of 12) for the focal plane processor.

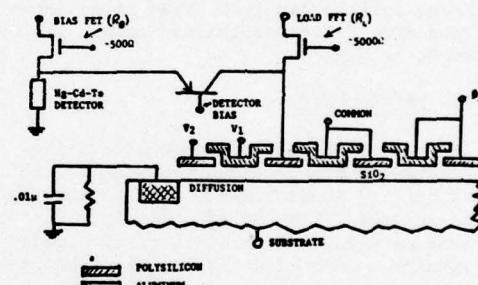


FIGURE 2
PREAMPLIFIER/CCD BUILDING BLOCK

The amplified signal voltage modulates the channel beneath a buried polysilicon electrode. The CCD register is operated with complementary two phase clocks. A "diffusion" current, entered through an RC integrating network, is introduced at the p+ diffusions adjacent to each input gate. It is this current, when modulated by gate signal voltage, which supplies charge to the CCD wells for transfer and integration. The width of the CCD registers are tapered, becoming progressively wider from the beginning to the end of the device. The

tapering effectively maintains a near constant percentage of fill level since well capacity becomes greater as charge is successively integrated along the line. Several gate modulated input schemes were evaluated. The integrating input, where charge is integrated on common over a clock period then shifted out at θ_1 rates, proved to have a lower noise equivalent input than that of the pulsed diffusion mode. (2) The voltage at the CCD output should be less than a volt in order to maintain reasonable linearity in the output charge amplifier. The on-chip output charge amplifier uses a floating diffusion with a single reset MOS transistor and a double source follower as shown in Figure 3.

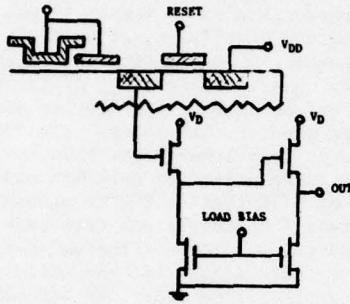


FIGURE 3
CCD OUTPUT

B. MOSFET Resistors: The MOSFET resistor used to bias the HgCdTe detector was designed to be 500 ohms at 2mA of current. This separate MOSFET supplies the detector bias current in order that only minimum current need flow through the bipolar transistor and associated load resistor. The preamplifier load FET is designed for 5K ohms when operating near 200 μ A quiescent current.

C. Bipolar Preamplifier: Several preamp designs were incorporated on each chip in order to determine the optimum gain-bandwidth and low noise configuration. The current gain (β) decreases substantially at lower temperatures. However, the α remains reasonable and a significant transconductance (g_m) can be obtained at 77°K. Figure 4 shows the noise model for the common base preamplifier. The preamplifier voltage gain is given by:

$$1) \text{ gain} = \frac{\alpha R_L}{R_D + r_e + (1-\alpha)r_b}$$

where

R_L = MOSFET Load Resistance

$$\alpha = \text{current transport factor} = \frac{\beta}{\beta+1}$$

$$r_e = \text{emitter resistance} = \frac{kT}{qI_e}$$

$$r_b = \text{base spreading resistance}$$

$$R_d = \text{detector resistance}$$

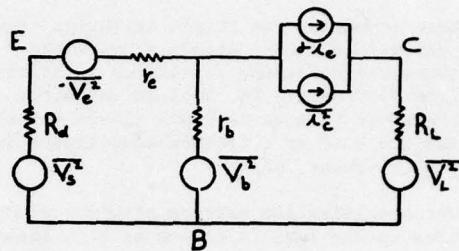


FIGURE 4
COMMON BASE AMPLIFIER NOISE MODEL

The noise equivalent input (NEI) of the preamp was designed for less than 2 nanovolts per root hertz. At midband the mean square equivalent input noise is given by:

$$\overline{V_{in}^2} = \overline{V_L^2}/G^2 + \overline{V_s^2} + \overline{V_b^2} + \overline{V_e^2} + \overline{i_c^2} (R_L/G + r_b)^2$$

where

G = amplifier gain

$\overline{V_s^2}$ = thermal noise of the source

$\overline{V_b^2}$ = thermal noise of the base spreading resistance

$\overline{V_e^2}$ = Voltage equivalent of emitter current noise (3)

$\overline{i_c^2}$ = Collector current noise

III. CIRCUIT FABRICATION

In order that the bipolar device fabrication be compatible with surface channel CCD processing, lateral bipolar transistors were built using a "triple diffusion" process. The basic processing steps for a triple

diffusion PNP-transistor E-channel CCD are:

- (1) P-type collector well diffusion (or implant) and drive in
- (2) N-base contact diffusion (required only for PNP devices)
- (3) N-type base diffusion and drive-in (simultaneous with input diffusions in CCD)
- (4) Contact holes and metallization (can be merged with CCD processing)

When comparing the triple diffusion transistor to the more standard types the parasitic collector resistance is higher (500-1500 ohms), the base to collector breakdown voltage is lower (15-30 volts), and the base to collector capacitance is higher (about 3pf).

The metallization pattern provided common ties to the same functions on each input and the fat zero (Fig 1 & Fig 2). The bias FETs (R_B) drains are common. The bipolar bases are common. The load FETs (R_L) gates and drains are each common. The integrating gates "common" for the 12 inputs and fat zero are also tied together. Fat zero level may be controlled separately by its own gate. One test pad was made available on the CCD input at the output of the amplifier on channel two. The combination of tied electrodes made separate evaluation of the effects of each component (R_B , bipolar, R_L , CCD gate) difficult without using special operating modes.

IV. EXPERIMENTAL RESULTS

A. Preamplifiers: Both NPN and PNP transistors were evaluated. The current gain betas (β) for both are tabulated in Table II for the various emitter configurations. Beta does decrease dramatically with temperature, however, at 77°K the $\frac{\beta}{\beta+1}$ appearing in the gain equation for a common base amplifier, is still reasonable. The magnitude of the base spreading resistance (r_b) is inversely proportional to temperature. At reduced temperatures the current crowding, even at 200 μ A, can affect beta. The multi-emitter structure minimizes r_b , reduces current crowding, and thus enhances beta at 77°K. Figure 5 shows the gain and

TABLE II
Transistor Beta
Collector Current = 200 μ A

Emitters	NPN		PNP	
	300°K	77°K	300°K	77°K
1	180	12.5	135	5.4
2	460	16.	110	5.6
4	500	19.5	110	5.6
8	440	23.0	130	6.2

noise over frequency for PNP amplifiers at 300°K and 77°K. Figure 6 is a similar graph for NPN amplifiers. With the reduced emitter resistance($\frac{kT}{qI_e}$) at 77°K, there is an increase in gain. With a 5K ohm load resistor the high frequency roll-off in gain is dominated by instrumentation input capacitance. Operating into a CCD gate the frequency response of the bipolar amplifier would be greater than shown. The PNP devices do have lower noise than the NPN devices. The noise for both NPN and PNP is higher at 77°K than at 300°K, probably due to increased contributions from base spreading resistance. Because the multi-emitter structure does reduce r_b , the noise associated with multi-emitter PNP and NPN devices is less than for a single emitter transistor at 77°K.

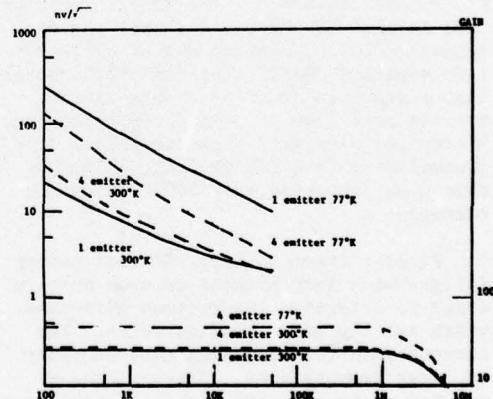


FIGURE 5
PNP GAIN/NOISE CHARACTERISTICS
(With discrete load resistor)

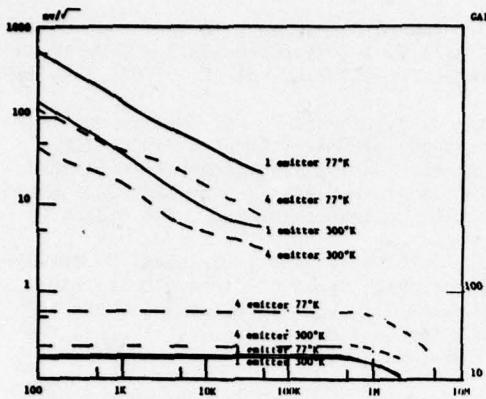


FIGURE 6
NPN GAIN/NOISE CHARACTERISTICS
(With discrete load resistor)

C. CCD & Preamp: The gain of this CCD is related to the g_m associated with the gate modulated input and the integration time. The g_m may be increased by increasing the dc current beneath the gate (channel current in the common source MOSFET analogy). With signal and bias applied to only one input the dc current can be adjusted to achieve a gain of about 1.5 in the CCD-2085 when clocked at one megahertz. In the TDI mode all inputs are on and the signals and dc bias levels add constructively. Therefore, the dc channel current must be reduced to prevent complete filling of any wells as each input adds to the main channel. The maximum signal gain achievable in the TDI mode was 0.2 at 1MHz data rate.

In order to study the effect of variations from the preamplifiers and input structures the CCD was run in both the TDI and multiplexer modes. In the TDI mode a long period (greater than 48 clock periods) pulse was entered into all inputs simultaneously to assure that TDI action would occur. The resulting output is a staircase with 12 steps. Variations in step height were noted. However, the relative amount due to gain variances, and dc variances could not easily be separated as the gain was low (0.2 as described above). In the second experiment the CCD was run as multiplexer in the higher gain mode with 200kHz clock. The "common" electrodes, which are between each input and the main channel, are normally biased to a dc level. In this case, they were held off and gated on for a short period and then the inserted signals

clocked out before inserting additional inputs. This short sampling period prevented the TDI action and permitted separate observation of the samples from each input. Operating the CCD register with the bipolar amplifiers off (emitter grounded) provides a reference output level for each input. Then, applying a stable dc voltage to each emitter, the resulting output can be compared to the reference. If there were no variations among amplifiers (bipolars and FET loads) then the differences in "off" and "on" outputs should be identical for all inputs. The measured differences using this technique on one P-channel device ranged from 9 millivolts to 111 millivolts. These variations can be attributed to:

Transistor base-emitter offsets leading to different dc currents through each load FET.

Resistance tolerance of the load FET.

The metallization pattern on the CCD-2085 did not permit experimental separation of the offsets from these two sources.

The dynamic range was characterized by applying a sinusoidal signal to a single input and determining when distortion becomes excessive. The signal was capacitively coupled to the CCD gate, which was dc biased through a large resistor. The clock frequency was 1MHz and the signal frequency was 10kHz. At the CCD output the signal is filtered to suppress the main clock frequency, and the harmonic components are measured using a spectrum analyzer (HP5556). The percentage 2nd harmonic component of the fundamental is used to express the signal transfer linearity and define the upper extreme for dynamic range. The setting of quiescent current (at zero + diffusion currents from 12 inputs) will determine where a large signal will start to distort. For a given quiescent current, the output spot noise of the CCD can be measured and the ratio of maximum signal to output noise established. At one megahertz clock and under particular bias conditions, the maximum signal for 3% second harmonic was 0.6 volts and the spot noise at 200kHz was $350\text{mV}/\sqrt{\text{Hz}}^{1/2}$. Dynamic range is defined as the ratio of the maximum undistorted peak-to-peak signal to the RMS value of the output wideband noise voltage. The dynamic range, assuming a 500kHz flat noise bandwidth, is 67db.

V. SUMMARY

A CCD delay and integration processor with integrated preamplifiers was developed for focal plane processing of signals from HgCdTe detectors. The CCD-compatible bipolar devices operating at 77°K exhibited gains greater than 30, bandwidths above 1.8MHz, and noise commensurate with good background limited HgCdTe detectors. The success of this bipolar/CCD monolith is in itself an important contribution to charge coupled device technology.

The IR system imposes many requirements on the design of the CCD focal plane processor. Noise, gain, bandwidth, dynamic range, uniformity, and power must trade-off against one another in a manner not to degrade system performance after the detector. Of particular interest in direct coupling from detector to preamp to CCD is dynamic range and uniformity. The measured linear dynamic range of 67db should be adequate under all but the most unusual scenario. For delay-and-integration operations, because the signals from individual channels are summed together, small variations between channels are unimportant. Large variations in dc level at the CCD input gate, however, may turn-off or saturate some channels. Interchannel non-uniformity can be caused by variations in the CCD gate threshold, transistor load resistance, or the transistor emitter-base threshold voltage. The process used to fabricate the CCD-bipolar combination must provide enough uniformity to minimize the occurrence of such effects. The non-uniformities measured on the CCD-2085 were great enough to impair efficiency on certain channels. Improved bias uniformity among CCD input gates may be obtainable through optimized device processing to minimize bipolar threshold variations or through ac coupling between amplifiers and CCD.

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INFRARED IMAGING WITH MONOLITHIC, CCD-ADDRESSED SCHOTTKY-BARRIER
DETECTOR ARRAYS: THEORETICAL AND EXPERIMENTAL RESULTS*

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ABSTRACT. The theoretical basis for infrared imaging in the 3 to 5 μm spectral band with CCD addressed silicon, Schottky-barrier mosaics is presented. A unique approach is used which allows readout of majority carrier signals with depletion mode CCD's. Photo-response, contrast, and noise relationships for this type of all solid-state sensor are derived. It is seen that the use of the Schottky-barrier, internal-photoemission process, which is independent of lifetime and doping variations in the silicon wafer, leads to at least a factor of 100 improvement in infrared photoresponse uniformity. This advance permits for the first time the development of infrared cameras that are not limited by fixed pattern noise. Systems considerations such as cooling requirements, noise mechanisms, and cutoff wavelengths, are related to signal contrast and noise-equivalent-temperature (N.E. ΔT .). A charge-coupled imager sensitive to infrared light as far out as 3.5 μm has been fabricated and operated. It consists of a linear array of 64 Pd:p-Si Schottky-barrier detectors adjacent to a three-phase charge-coupled shift register. A single transmission gate, when pulsed on, coupled each detector to its associated shift register gate, thus reverse-biasing the detectors. The charges transferred to the shift register are then read out sequentially to produce the video signal. It is demonstrated that in this mode of operation, the IR-CCD is particularly immune to non-uniformities in substrate doping and in MOSFET pinch-off voltage. Visible images were sensed directly by illumination of the shift register through the gaps as well as through the unthinned substrate. Infrared images ($1.1 \mu\text{m} < \lambda < 3.5 \mu\text{m}$) were sensed by the Schottky-barrier detectors illuminated through the (transparent) substrate. The two imaging modes could be easily distinguished by their spectral sensitivities as well as by their responses to changes in their separate integration times. All IR measurements were made at 77°K. Uniformity was within a few percent, and objects at 110°C could be detected. A scheme for observing low-contrast, thermal scenes without requiring the charge-coupled shift register to carry the entire background signal has been implemented in the design of this chip. Operation in this mode was also demonstrated.

INTRODUCTION

The realization of a viable infrared television camera with electronic scanning would represent a major advance in thermal imaging technology. Applications would range from military reconnaissance and weapons delivery systems to high resolution, real-time thermography systems for earth resource management and medical diagnostics. We will describe recent results of a device effort directed towards the development of silicon monolithic focal planes that are suitable for an IRTV.

The design of an IRTV camera for thermal imaging is complicated by signal conditions which include the presence of high photon flux densities from the thermal background and low scene contrast. Cameras use frame integration to achieve high sensitivity; therefore, an IRTV must have very wide dynamic range to accommodate background flux integration without signal saturation. Further, in the presence of high background flux densities, point to point variations of photoresponse, give rise to fixed pattern noise which obscures low contrast detail. We are attempting to develop a diode array

* This work was funded by the Defense Advanced Research Projects Agency.

focal plane that has sufficient dynamic range to accommodate the infrared background in the 3 to 5 μm spectral range and sufficient spatial uniformity to give good thermal imagery. The focal plane consists of ordered arrays of Schottky internal photoemission diodes operated in staring-mode which are multiplexed by an integral surface channel CCD. The focal plane is fabricated using standard silicon micro-circuit technology.

SCHOTTKY INTERNAL PHOTOEMISSION

It has been suggested that the Schottky internal photoemission process is inherently more uniform than conventional photodetection processes and that this process could be exploited in the development of IR thermal imaging retinas.² The internal photoemission process is shown in Fig. 1. The metal photocathode of a Schottky barrier is illuminated through the silicon semiconductor substrate resulting in photoemission of charge into the semiconductor from the metal. Photoemission occurs in a spectral band determined by the silicon transmission edge at 1.1 μm and the internal photoemission threshold wavelength, λ_c , given by

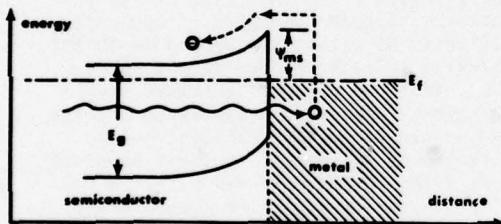


Fig. 1. Band diagram of Schottky-barrier detector.

$$\lambda_c (\mu\text{m}) = \frac{1.24}{\psi_{\text{ms}} (\text{eV})} \quad (1)$$

where ψ_{ms} is the Schottky barrier potential. Within the above spectral range, the photoemission quantum efficiency, η , is given by

$$\eta(v) = C_1 \frac{(hv - \psi_{\text{ms}})^2}{hv} \quad (2)$$

provided that the metallic photo-absorption process is energy independent. In Eq. 2, hv is the photon energy and C_1 an efficiency

coefficient that is dominated by properties of the metal.^{3,4} Archer and Yep⁵ have shown that the value of ψ_{ms} is independent of the substrate doping density over large ranges of impurity concentration. The only significant variation of ψ_{ms} with semiconductor properties is that due to the conductivity type where

$$\psi_{\text{msn}} + \psi_{\text{msp}} = E_g \quad (3)$$

Thus, the quantum efficiency of an internal emission photodiode is expected to be insensitive to normal variations in semiconductor properties. Further, it should be noted that this process emits majority carriers into a substrate that is operating at high enough temperatures to have full extrinsic ionization; two factors which combine to eliminate most of the causes of spatial non-uniformities in the photoresponse of other detectors. Variations of minority carrier lifetime, diffusion length and impurity compensation can be neglected. The key remaining causes of spatial non-uniformity will be variations of sensor cell geometry, Schottky barrier formation metallurgy, multiplex losses and dark current. Dark current variations can be minimized by cooling to the point where dark signals are negligible. We note that the dark current density is given by

$$J_d = A_r T_d^2 \exp \left(\frac{-\psi}{kT_d} \right) \quad (4)$$

where k is Boltzmann's constant and A_r is Richardson's constant ($20 \text{A cm}^{-2} \text{K}^{-2}$ for p-Si) and T_d is the detector temperature. Dark currents become negligible at 80°K for $\lambda_c \leq 5 \mu\text{m}$.

Shepherd, et al⁶ have shown experimentally that both continuous and reticulated Schottky surfaces have the expected improvements in spatial uniformity, but their work does not include the effects of spatial variation of multiplex losses.

THERMAL IMAGING

Since quantum efficiencies of internal photoemission diodes are low, staring-mode operation is used to achieve good sensitivity. In staring-mode an infrared scene is projected onto the Schottky array and the resulting signal is accumulated for a frame time, t_s . At the end of the frame, the array is multiplexed cell by cell and

the resulting charge pulse train provides a video signal of the IR image. We will now calculate the magnitude of these charge pulses and the resulting sensitivity of the Schottky arrays.

Consider a Schottky focal plane mounted in a cold chamber that is exposed to a uniform thermal background at temperature, T_b , through an aperture of f-number, F. In the short wavelength limit, where $hv \gg kT_b$ the photon flux incident on the focal plane in the frequency interval, dv , is given by

$$N(T_b, v) dv = \frac{\pi v^2}{2c F^2} \exp\left(\frac{-hv}{kT_b}\right) dv \quad (5)$$

where c is the velocity of light and h is Planck's constant. The number of electrons collected per frame by a cell of area A is given by

$$N_b = At_s \int_{\psi_{ms}}^{\infty} n(v) N(T_b, v) dv \quad (6)$$

$$N_b = \frac{\pi A t_s C_1 k^4 T_b^4}{c F^2 h^3} \left(\frac{\psi_{ms}}{kT_b} + 3 \right) \exp\left(\frac{-\psi_{ms}}{kT_b}\right) \quad (7)$$

The resulting signal contrast, γ , is given by

$$\gamma = \frac{dN_b}{dT_b} N_b^{-1} \quad (8)$$

For a Schottky retina that has a barrier height ψ_{ms} the contrast is given by

$$\gamma = \frac{1}{T_b} \frac{\left(\frac{\psi_{ms}}{kT_b} + 3\right)^2 + 3}{\left(\frac{\psi_{ms}}{kT_b} + 3\right)} \quad (9)$$

For a 15°C background, γ varies from 6.9%/°K for threshold at 3 μm to 4.3%/°K for threshold at 5.5 μm. Thus, a system uniformity better than 0.4% would not prevent the resolution of 0.1°K details.

In order to calculate the response of a Schottky retina to a thermal signal we note that most metals have values of $C_1 \approx 0.1$ (eV)⁻¹. Later we will consider a CCD addressed retina that has Pd₂Si Schottky contacts of area 2.8×10^{-5} cm². The Pd₂Si retina has a photoemissive threshold at

$\lambda_c = 3.54 \mu m$. Other retinas under design cut-off at 4.5 μm and 5.5 μm. The cell response of these retinas to a 15°C background is given in Table 1.

Table 1. Thermal Background Photoresponse of Schottky Diodes

$\lambda_c (\mu m)$	$N_b(T_b)$	$\gamma N_b(T_b)$	$N_b(T_b+10^\circ)$	$N_b(T_b+100^\circ)$
3.54	2.0×10^4	1.2×10^3	3.6×10^4	2.0×10^6
4.5	3.4×10^5	1.7×10^4	5.5×10^5	1.6×10^7
5.5	2.2×10^6	9.5×10^4	3.3×10^6	saturated

$T_b = 15^\circ C$, $A = 2.8 \times 10^{-5}$ cm², $t_s = 30$ ms, $F = 1$, and $C_1 = 0.1$ eV⁻¹.

A detail in an infrared scene will be detected as a low contrast signal superposed on the background signal, N_b . Consider an object which is at a temperature ΔT above T_b , and which has an image that subtends a sensor cell. The cell which views the object will have an accumulated charge N_j where

$$N_j = N_b + \frac{dN_b}{dT} \Delta T \quad (10)$$

The signal of interest is

$$N_s = N_j - N_b = \frac{dN_b}{dT} \Delta T = \gamma N_b \Delta T \quad (11)$$

Note that γN_b given in Table 1 represents the number of additional charges counted per cell from an object 1°C above background temperature. The signal-to-noise ratio of our measurement will be

$$\frac{N_s}{N_t} = \frac{\gamma N_b \Delta T}{N_t} \quad (12)$$

Where \bar{N}_t is the total rms noise of the detector, its multiplexer and its associated amplifiers. The noise equivalent temperature is then given by setting Eq. 12 to unity.

$$\bar{N}_t / (\text{NEAT}) = \frac{\bar{N}_t}{\gamma N_b} \quad (13)$$

To find \bar{N}_t we follow Carnes and Kosonocky⁷ with the following differences:

1. On focal-plane thermal noise corresponds to 80°K rather than 300°K.
2. Operation is at high infrared backgrounds where photo-electron shot noise can be significant, and where, for low contrast targets, $N_j \approx N_b$.

TABLE 2. IR SCHOTTKY CCD NOISE SOURCES AND NOISE EQUIVALENT TEMPERATURES^a

SOURCE	\bar{N}	$\lambda_c = 3.54 \mu\text{m}$	$\lambda_c = 4.5 \mu\text{m}$	$\lambda_c = 5.5 \mu\text{m}$
Photo-electron Shot Noise	$\sqrt{\bar{N}_b}$	1.4×10^2	5.8×10^2	1.5×10^3
Background Charge, Incomplete Transfer Noise ^b	$\sqrt{2\epsilon N_g N_1}$	1.6×10^3	1.7×10^3	2.1×10^3
Fast Interstate Trapping Noise ^c	$\sqrt{1.4 N_g (kT/q) N_{ss} A_g}$	1.6×10^3	1.6×10^3	1.6×10^3
Floating Diffusion Reset Noise	$200 \sqrt{C_{pf}}$	200	200	200
Combination of Above Noise Sources	\bar{N}_t	2.3×10^3	2.4×10^3	3.0×10^3
NEAT From Above Sources	$\bar{N}_t / \gamma N_b$	1.9°K	0.15°K	0.04°K
NEAT Including Above Sources and 1% Nonuniformity		1.9°K	0.20°K	0.23°K

a) Terms defined in Ref. 7.
b) ϵN_g (transfer loss per gate times number of gates) was taken from Ref. 8.
c) N_{ss} was taken as $4 \times 10^{10} \text{ cm}^{-2} \text{ eV}^{-1}$.

Because of the large background signal, an electrical bias charge (fat-zero) is not needed. Assuming that the first well has 0.25 pf capacitance and the floating diffusion and MOSFET gate have 1 pf capacitance, we find the results given in Table 2. These results indicate that a Schottky focal plane with a floating diffusion and MOSFET output can have very good sensitivity.

IR-CCD DESIGN

There are several approaches to the design of infrared, charge-coupled imagers. One is the fabrication of charge-coupled shift registers on materials having the desired intrinsic response.⁹ Such materials include InAs, InSb, and HgCdTe. Infrared radiation would be absorbed in the wafer, generating minority carriers which would then be transported just as in silicon devices. A second approach is the fabrication of charge-coupled shift registers on silicon wafers with separate infrared detectors prepared on the wafer. Schottky barriers are a natural choice though photoconductive films and heterojunction detectors are other possibilities.⁸ A third approach is the use of extrinsic silicon.¹⁰

Our approach to the design of infrared-sensitive, charge-coupled imagers has been to use well-known technologies, namely charge-coupled shift registers and Schottky-barrier detectors fabricated on silicon wafers. This requires that the majority-carrier signals from the detector be converted to minority-carrier packets for transport by the shift registers. Methods for accomplishing this were reported by Shepherd and Yang,² and by Williams and Kosonocky.¹¹ The latter method, which we adopted for this work, is simpler, and has the advantage that the large background signal from a thermal scene need not be transferred to the shift registers. While this technique does not, by itself, compensate for nonuniformities in the detector array, it does make better use of the shift register's dynamic range and thereby makes possible the use of frame comparison techniques. To test these ideas, we fabricated 64 x 1 linear arrays of Schottky-barrier detectors coupled with three-phase, charge-coupled shift registers. The structure used for coupling the Schottky barrier detectors to the charge-coupled shift register is shown in Fig. 2. A row of Schottky-barrier metallizations is seen in the center of the chip. The center area

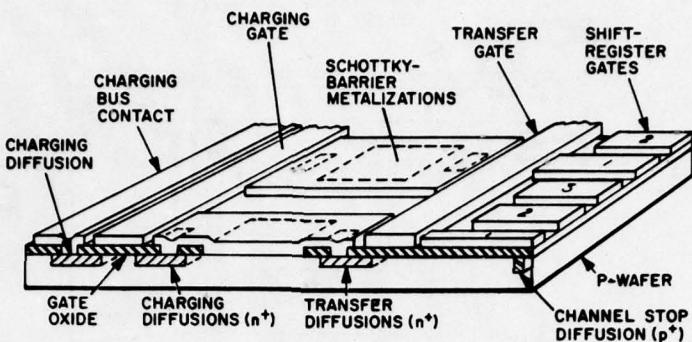


Fig. 2. Layout of IR-CCD.

of each metallization contacts the p-wafer forming the infrared-sensitive area. Each metallization also contacts individual charging and transfer diffusions. The transfer gate overlaps the transfer diffusions, and can couple them individually to the phase-1 gates of the shift register. The phase-1 gates are wider than the other shift register gates for just this reason. The charging gate on the left of the detectors overlaps the individual charging diffusions and can couple them all at once to the charging bus diffusion. A channel stop diffusion at the right terminates the shift-register channel as shown in the illustration. The shift-register gates are connected to three phase buses to the right of the channel (not shown in Fig. 2). Strips of channel stop, also not shown in the illustrations, are included between the detectors to prevent coupling.

The structure shown can be operated in two different modes: the high contrast mode or *vidicon mode*, and the *thermal imaging mode* or *skimming mode*. A device designed for use in the high contrast mode does not require the charging gate or the charging diffusions. If these structures were included in the device, the charging gate can simply be biased negatively and ignored. The three-phase clock voltages are applied to the shift-register gates. At some time in the cycle, when the phase-1 shift register gates are on and the other two phases are off, a positive pulse is applied to the transfer gate making the potential under that gate V_A as in Fig. 3b. The floating transfer diffusion will settle at a potential equal to V_A . All excess charge flows across the transfer gate chan-

nel into the deeper CCD potential well. After the transfer pulse ends, the shift register clocks out the charge packets. The next time, and each subsequent time, the transfer pulse is applied, the detectors are reset to the same potential, V_A , and the charges removed are stored in the phase-1 wells. These charges represent the photocurrent and dark current that accumulated at the detectors during the integration time, and make up the video signal when read out. This mode of operation is somewhat different from that used in interline devices with photogates where all minority carriers are removed from the detectors during the transfer time. It is more closely related to the mode of operation of a vidicon, since the detectors are reset to the same potential each frame, with the charge removed to do this making up the video signal. Hence, the designation: *vidicon mode*. An imager designed for use in this mode should have detectors whose charge storage capacity is about the same as a shift-register well since the entire detector signal plus dark current must be carried out by the shift register. For thermal images with only a few percent contrast, however, the dynamic range of the shift register would be better utilized if only the small fraction of charge containing the signal modulation were transferred out by the CCD and the large constant background charge containing no information were removed by an auxiliary drain. This can be accomplished with the help of the charging bus and the charging gate shown in Figs. 2 and 3. A large potential V_B is applied to the charging bus (Fig. 3b) which acts as an auxiliary drain for the constant background charge. A clock pulse is applied to the

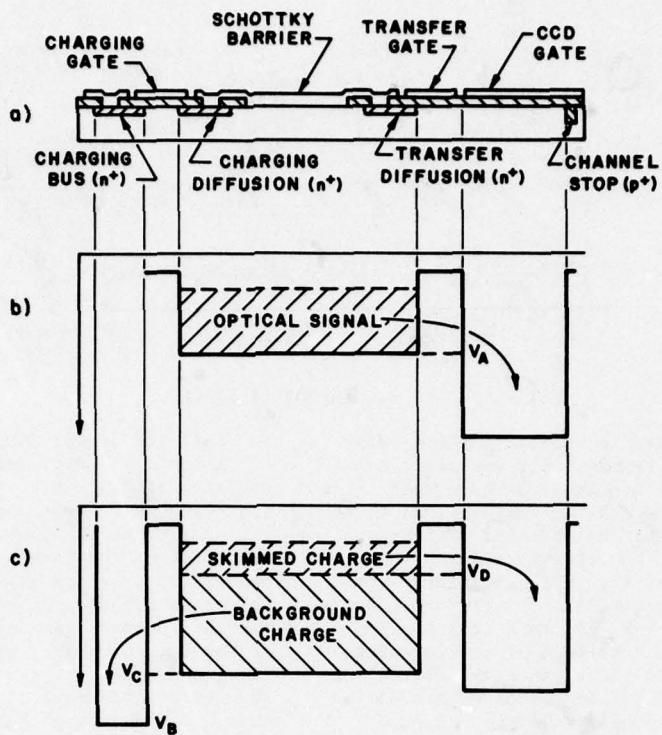


Fig. 3. Electron potential energy profile of IR-CCD during operation. (a) Cross-section of device. (b) Potential profile during operation in the vidicon mode. (c) Potential profile during operation in the thermal imaging mode. Certain details were omitted for clarity.

charging gate once per frame, setting the surface potential under it to V_C . This in turn sets the charging diffusions, Schottky-barrier gates and transfer diffusions to V_C , since all excess electrons stored on these conductors will spill over the charging gate channel into the charging bus and be returned to the substrate. Thus the initial level of the Schottky barrier is set by the charging gate pulse amplitude, not by the transfer gate pulse amplitude as in the vidicon mode described earlier. At the end of the integration period a small pulse is applied to the transfer gate which causes its surface potential to go to V_p (see Fig. 3c). Now only the charge above V_D will drain into the CCD potential well and be read out. Remaining behind is the constant background charge. This background charge is removed shortly thereafter when the charging pulse comes on and sets the Schottky barrier to V_C . It

is assumed that the light falling on the detectors is sufficient to discharge each of them below V_D . In actual operation, V_C would be adjusted to ensure this condition.

DESIGN AND FABRICATION

The shift register was a 64 bit, 3-phase, linear CCD having a single level of metallization with $2.5 \mu\text{m}$ gaps. The gates are $12.5 \mu\text{m}$ long in the directions of charge transfer, making the bit spacing 45μ . The channel is $125 \mu\text{m}$ wide, and is confined by a channel stop diffusion. The Schottky-barrier contact holes are rectangles $125 \mu\text{m}$ by $22.5 \mu\text{m}$ and are spaced on $45 \mu\text{m}$ centers along the CCD register so that each detector can load into a phase-1 CCD gate when the transfer gate is clocked. There is a source diffusion with loading gates at one end of the shift register and a resettable floating diffusion connected to an

on-chip MOS transistor at the other end. The fabrication procedure is as follows. A $10^{15}/\text{cm}^3$ doped (100) silicon wafer is subjected to a p-type diffusion and an n-type diffusion, each defined by a thermal oxide left after a photolithographic step. The gate oxide is grown, and contact holes are opened. Palladium is then evaporated onto the wafer in a vacuum system that received special care to avoid sodium contamination. While the palladium is being evaporated, the wafer is heated, causing palladium silicide to be formed in a chemical reaction. The wafer is then removed from the evaporator, and the remaining metallic palladium is etched off. It is returned to a vacuum system, where it receives a film of aluminum to be defined photolithographically. Thinning was not necessary because silicon is transparent to infrared light beyond $1.1 \mu\text{m}$. Fig. 4 shows photomicrographs of the two ends of a completed device on a wafer containing about 50 chips. The vertical white rectangles in a row along the top (1) are the Schottky barrier metallizations, each overlapping the contact holes to the substrate and to the setting and transfer diffusions. The setting gate (2) and the transfer gate (3) control the channels to the setting diffusion (contacted by 4) and the phase-1 gates (5), respectively. The bonding pad for the phase-1 bus-bar (5) cannot be seen because it is near the center of the CCD. Phases 2 (6 and 7) and 3 (8 and 9) are double-end

connected because they require a diffused crossunder which is more resistive than a metallization. Two separate gates are provided at the beginning (10 and 11) of the shift register and at the end (12 and 13). A source diffusion (contacted by 14) is provided to permit electrical input to the shift register while a floating diffusion with a reset gate (15) and drain (16) is provided at the output. The floating diffusion is connected to an on-chip MOS transistor whose source and drain diffusions are brought out to pads 17 and 18. Contact to the substrate is made at pads 19 and 20, each of which contacts a channel-stop diffusion.

A circuit diagram of the IR-CCD chip is shown in Fig. 5. The extra gates G_2 and G_3 , which were included to make possible other input and output schemes, are connected in sequence with the three phases, while G_4 receives a small positive bias, and the reset gate is pulsed. For operation with electrical input, the transfer gate receives a negative bias, isolating the shift register from the detectors while the three-phase, overlapping clock waveforms run continuously, and a burst of electrical pulses is applied to G_1 . At the clock rate of 250 KHz used in this work, the minimum transfer loss of 5×10^{-4} per transfer was achieved with a bias current (at zero) of $0.3 \mu\text{A}$.

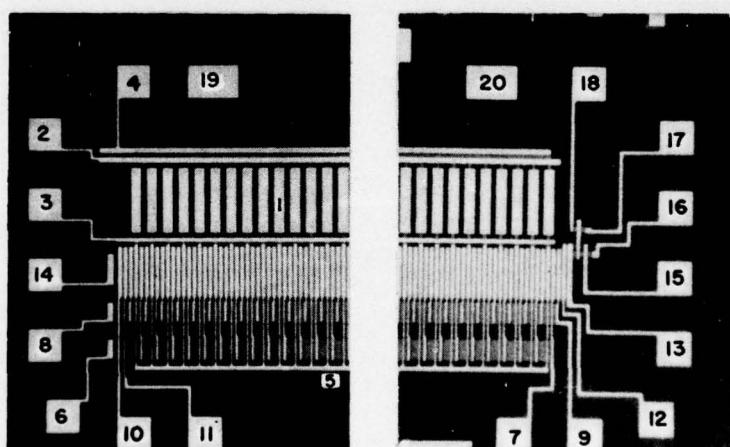


Fig. 4. Photomicrographs of the two ends of the CCD chip.

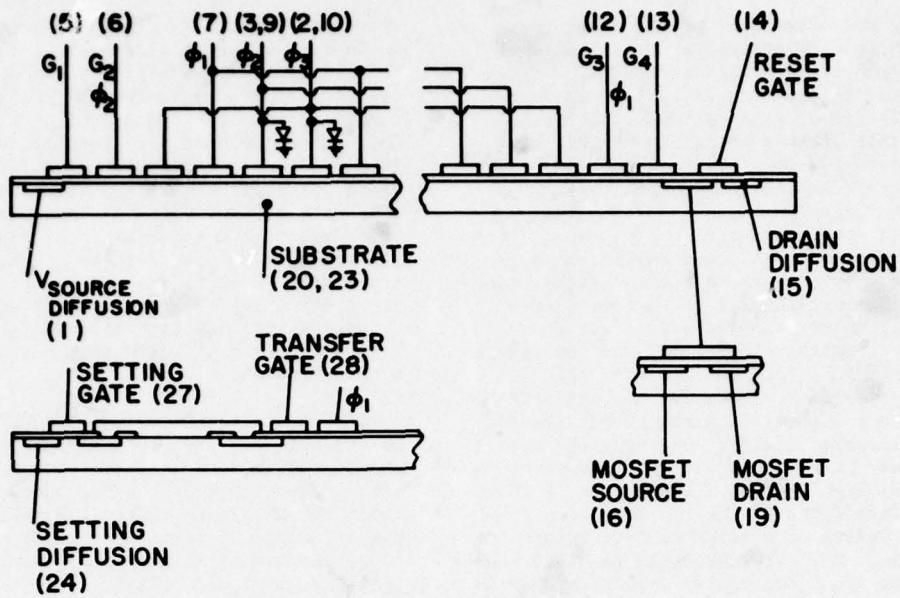


Fig. 5. Circuit diagram of the IR-CCD chip. The diodes indicate diffused busses.

DETECTION OF INFRARED IMAGES (VIDICON MODE)

For infrared imaging, the IR-CCD chip was operated in a quartz optical dewar containing liquid nitrogen. A weak tungsten lamp illuminated an adjustable slit that was imaged on the IR-CCD chip with a germanium lens. The lens also served to block light of wavelength less than 1.7 μm . The charging gate was biased negatively to pinch off that channel. The integration time for infrared detection is the time between transfer pulses. The shift register runs continuously during the integration, with the first 64 bits after the transfer pulse ends comprising the video signal; only during the transfer pulse does the shift register not run. Hence, the transfer pulse width is the integration time for light detection by the shift register. Any doubt whether the video signal was caused by absorption at the shift register or absorption at the Schottky barriers can be resolved by varying the two integration times independently. Fig. 6 shows the video signal for imaging with a narrow slit and a wide slit in different locations. The signal with the narrow slit was 2 bits. Making the slit still smaller did not improve the resolution beyond this.

The limitation was probably in the focusing as the shift register had sufficiently good transfer efficiency to deliver a single recognizable bit. For this chip, a transfer pulse as high as 15 V could be used without significant dark current. The optical system was focused using the video signal of a narrow slit as a guide. The slit could then be moved laterally to scan the signal across the oscilloscope screen. A photograph of the video signals with the narrow slit in four positions is shown in Fig. 7. A soldering iron tip, invisible to the human eye, easily saturated the video signal. A hotplate at 110°C could be detected with a 30-ms integration time.

It should be noted that, unlike some visible charge-coupled imagers, this IR-CCD is immune to smear and blooming. Smear occurs when imaging is performed by the shift register, and an unusually bright spot creates a significant number of carriers in a shift-register well during the short time between two consecutive clock pulses. Since our chip will not be allowed to image at the shift register, this mechanism does not apply. This is true of all CCD's of the "interline" type. Blooming

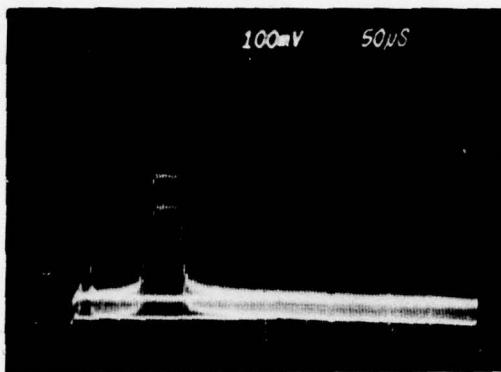


Fig. 6. Video signal for infrared imaging with a narrow slit and a wide slit. The first trace was taken with the slit smaller than 0.1 mm; the second trace was taken with the slit repositioned and set to 1.0 mm.

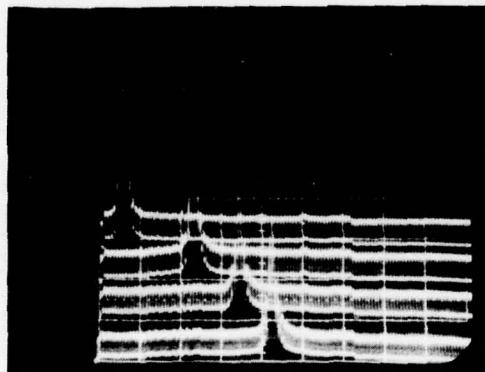


Fig. 7. Video signal corresponding to a narrow slit in four positions.

occurs when a bright spot causes a well to become overfilled with minority carriers which then transfer to adjacent wells. Again this is not possible at our shift register because we do not permit imaging there. A charge-coupled imager with separate p-n junction detectors or photogate detectors could conceivably bloom but Schottky barriers are majority-carrier devices. No minority carriers are even generated, so there is no blooming mechanism.

DEVICE UNIFORMITY

Although Schottky-barrier detectors offer the advantage of uniformity good enough for thermal imaging, this advantage would be lost if nonuniformities were introduced by the transfer process. We must, therefore, consider the consequences of the charge-coupled imager. Possible nonuniformities include those associated with substrate doping, oxide thickness, oxide charge, and accuracy of definition in the photolithographic process. A variation in doping across the array will not have any significant effect on Schottky barrier detector responsivity but will result in a variation of detector capacitance. If the device is operated in the vidicon mode, (with the detectors recharged by the shift-register wells) small differences in detector capacitances should not show up in the video signal. Of course, if dark current were a factor, doping variation would result in dark-current variation. Variations in oxide thickness or oxide charge would cause variation of the surface potential under the transfer gate, and thus would result in a variation of the level to which the detectors are set. Still, in the vidicon mode of operation, each detector is reset to its same potential at the end of each frame. The charge removed is independent of the capacitance and of the transfer level so long as the detectors are not discharged to zero. Thus, in the vidicon mode, the transfer process should not introduce any additional nonuniformities. The uniformity with which the contact holes can be defined and etched will clearly affect the uniformity of response. However, uniformity measurements on similar arrays at Air Force Cambridge Research Laboratories suggest that this will not be a problem.⁶

The uniformity obtained experimentally in the vidicon mode is shown in Fig. 8. The video signal, measured downward, is shown for seven levels of approximately uniform, germanium-filtered, tungsten illumination. Local nonuniformities of a few percent can be seen on the signals with small illumination. Slow variations across the signal are most likely due to grading of illumination. Much larger variations can be seen at high levels of illumination as some of the detectors are discharged to zero.

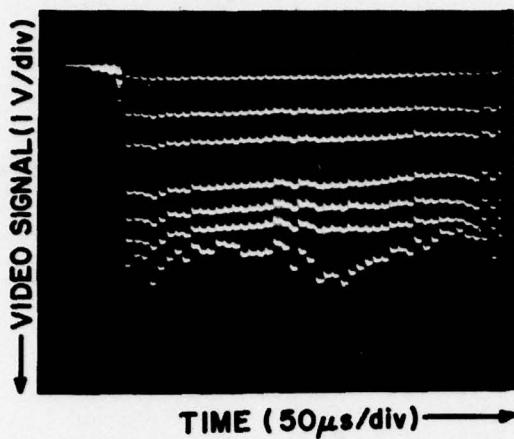


Fig. 8. Response of a typical IR-CCD in the vidicon mode to several levels of approximately uniform infrared illumination.

OPERATION OF THE BACKGROUND-SUPPRESSION (SKIMMING) MODE

In the background-suppression (skimming) mode of operation the initial Schottky barrier potential is set at the beginning of the integration period by the surface potential under the charging gate. The charge which is transferred into the CCD is determined by the surface potential under the transfer gate which is turned on at the end of the integration period when phase-1 is high, as in Fig. 3c. The voltage on the transfer gate is set so that just the "top" of the optical signal containing the signal modulation is skimmed off. The uniform background charge remains behind and is drained into the charging bus when the charging gate is turned on at the start the next integration period. In order for the skimming technique to be beneficial, the charge storage capacity of each detector must be several times that of a shift register gate. If the shift register can hold the entire detector signal, there is no reason to have it do otherwise. Indeed the skimming mode might be expected to introduce non-uniformities in the video signal because of variations in the threshold voltages of the transfer gate and the charging gate. In the vidicon mode these differences are not observed because the same gate (the transfer gate) is used to initially set the

Schottky barrier potential and to remove the charge. Variations in detector capacitance can be expected to show up in the skinned video signal as well, even in the absence of threshold variations. The devices were operated in the background suppression mode with scenes consisting of bright slits and a uniform background. For fixed optical input, increasing the potential applied to the charging gate did reduce the video signal, eventually removing the slit peaks as expected. However, since the storage capacity of the detectors in our device was smaller than the shift register well capacity, the true value of this technique could not be demonstrated. The operation in this mode was displayed more clearly with the charging circuit used to load charge in the dark. In these measurements, the charging bus was used to set the charging level with the charging gate used as a transmission gate. The relative magnitudes of the charging and transfer levels were reversed compared to Fig. 3. Here, with no illumination, that circuit is being used to create a signal. The lower the charging bus potential the more charge is loaded. Fig. 9 shows three different output signals using this mode of operation for three different charging bus potentials. The non-uniformities displayed here result from differences in the threshold voltages and detector capacitances, and contrast vividly with the uniformity displayed in Fig. 8 for the same device. Thus, while the skimming mode has been demonstrated, much better control of device uniformity will be required for practical use in this mode.

CONCLUSION

Schottky-barrier detector arrays were shown to have the uniformity required for thermal imaging with sufficient sensitivity for use in the staring mode. Calculations indicate that thermal imaging is possible in the 3 to 5 μm region with noise-equivalent-temperature of a fraction of a degree K. A charge-coupled imaging array using palladium-silicide Schottky-barrier detectors has been designed, fabricated, and tested. Thermal scenes as low in temperature as 110°C were imaged. It was shown theoretically that in the vidicon mode of operation, non-uniformities in the transfer process and in detector capacitance do not degrade the video signal, and good uniformity was indeed obtained in this mode. A scheme for removing

the background signal from the detectors before loading into the CCD was incorporated into the design of the chip, and operation in this mode was also demonstrated. This imager, though made with a single level of metallization with gaps, had reasonably good transfer efficiency and is immune to smearing and blooming.

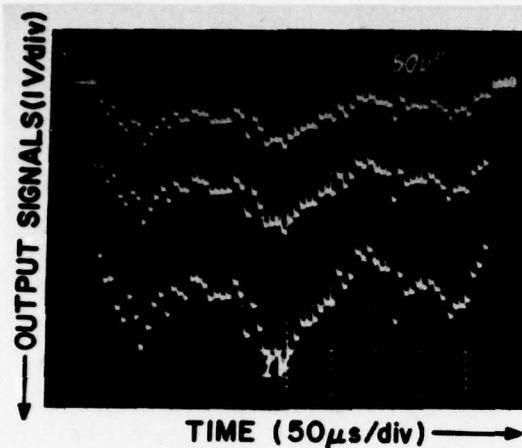


Fig. 9. Output signals from shift register with charge loaded into the unilluminated detectors from the setting diffusion. The largest output signal corresponds to the lowest setting potential. The transfer level was the same for all three cases. The device was the same one used for Fig. 8.

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SERIES-PARALLEL SCAN IR CID FOCAL PLANE ARRAY CONCEPT

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ABSTRACT

A series-parallel scan IR focal plane array concept which uses small InSb CID modules is introduced. The CID is used to premultiplex photocurrent through a preamplifier before the photosignal is introduced into a Si CCD TDI signal processor. An analysis of the expected performance of this configuration suggests that if correlated double sampling is used in the CID readout, a larger f^* can be obtained (in the 3-5 μm region) than with most other focal plane array configurations (which use direct injection).

INTRODUCTION

The development of silicon CCD and CID area imaging arrays for $\lambda < 1 \mu\text{m}$ has encouraged the infrared community to examine the application of these technologies to infrared focal planes. For terrestrial applications the interest is primarily in the development of new kinds of thermal imagers for the 3-5 μm and the 8-12 μm atmospheric windows. We expect that the use of CCD's at or near focal plane will permit the use of thousands of IR detectors in a focal plane at reasonable cost. If these future focal plane arrays (F.P.A.'s) succeed in being limited by statistical fluctuation in background flux (background limited) a signal-to-noise ratio improvement proportional to the square root of the number of detectors can be expected compared to present systems assuming other design parameters remain constant. This paper will concentrate on the problems associated with obtaining background limited performance with F.P.A.'s operating in the 3-5 μm region.

CCD and CID structures can be fabricated in materials sensitive to infrared radiation however CCD and CID structures which are appropriate for the visible and very near infrared are not necessarily appropriate for thermal imaging systems. Because of the low contrast of thermal imagery a DC coupled staring sensor would have difficulty distinguishing between

variations in detector responsivity and variations in image irradiance. For example net detector to detector responsivity uniformity in an unscanned array would need to be better than 0.35% in the 3.4-5.1 μm band in order not to compete with apparent target temperature differences of 0.1°C.

The use of area arrays in a mechanically scanned series-parallel configuration using time delay and integration (TDI) and an effective AC coupling of the detector with the image avoids these stringent uniformity requirements. Also TDI provides built in redundancy in that a few dead detectors can be tolerated without significantly degrading the imagery.

The technical approach to a high packing density array for series-parallel scan which to date has received the most investigation mates conventional InSb photodiodes with a Si CCD chip to form a InSb photodiode Si CCD sandwich focal plane module. (See Fig. 1).^{1,2} Several modules would be used to form a focal plane of thousands of detectors. With this approach each detector is individually connected to a direct injection input circuit which inputs photocurrent into a silicon TDI CCD register. This method of inputting photocurrent into a Si CCD requires a connection for each detector and has certain signal-to-noise limitations which will be discussed

later. Preamplifiers between the detector and the CCD have not been used to date due to packing density considerations.

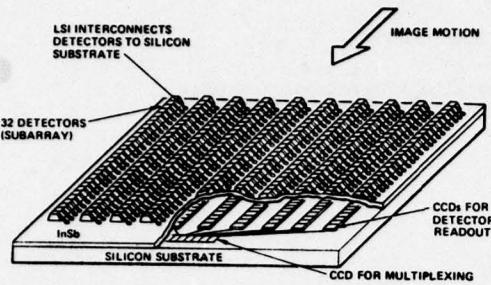


FIGURE 1 - Sandwich/direct injection IR focal plane array using IR photodiodes and Si CCD TDI registers.

As an alternative to the sandwich/direct injection F.P.A. structure discussed above we propose the approach series-parallel scan with InSb shown in Fig. 2 which is based on the CID in InSb developed by Kim.³ The CID in effect premultiplexes the photocurrent through a preamplifier before it is demultiplexed and inserted into Si CCD TDI registers. High transfer efficiency in the InSb is not required since an x-y readout can be implemented. Connections must be made to the x-y readout lines on the CID module, but for the 400 detector module size suggested in Fig. 2 this is only 0.1 interconnect per detector. The CID modules must be read out more than once per dwell time leading to high clock frequencies, but the premultiplexing feature allows the use of a small number of high quality preamplifiers before introduction of the signal current into the CCD TDI signal processor. This can lead to improved signal to noise performance over direct injection as will be explained later. "Background rejection" equivalent to A.C. coupling would be provided at the TDI output as with the sandwich/direct injection structure.

OPERATION OF SERIES PARALLEL SCAN CID

Operation of the focal plane shown in Fig. 2 can be understood by reference to Fig. 3. With the arrangement shown in Fig.

3, each CID detector which integrates photo-generated charge is read out sequentially at a rate such that the entire CID module is read out in the time the image moves a distance $y/2$ on the focal plane where y is the detector center to center spacing.

When detector 5A is read out gate A° is closed and the amplified signal charge is fed into CCD well 1A'. When detector 5B is read out gate B° is closed and the amplified charge is fed into CCD well 1B'. Before detector 4A is read out the charge in 1A' is transferred to 2A' to make room for the charge from 4A. This process continues until the entire CID module is read out and an amplified replica of the signal from detector 1A, 2A, 1B, 2B, etc., is stored in CCD wells 1A', 2A', 1B', 2B'. At that point, the transfer gates are opened and the charge

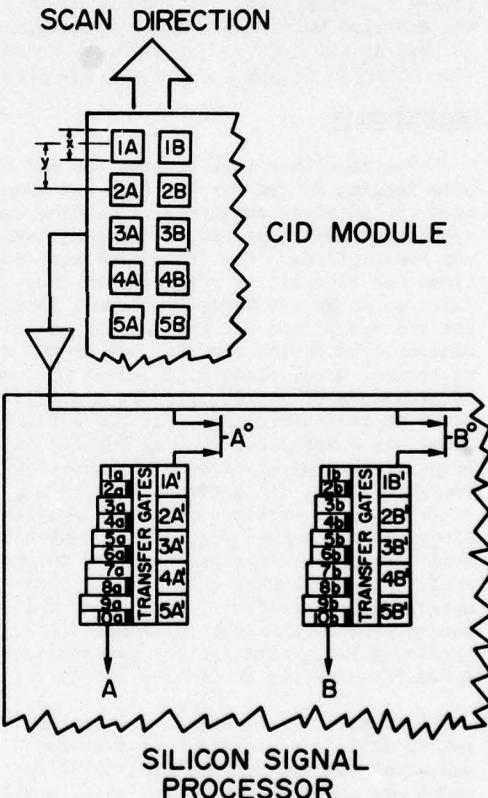


FIGURE 3 - Schematic of the CID module and the Si TDI signal processor used for series parallel scan.

SERIES PARALLEL SCAN InSb CID FOCAL PLANE ARRAY (IR IMAGER OR SEARCH SET)

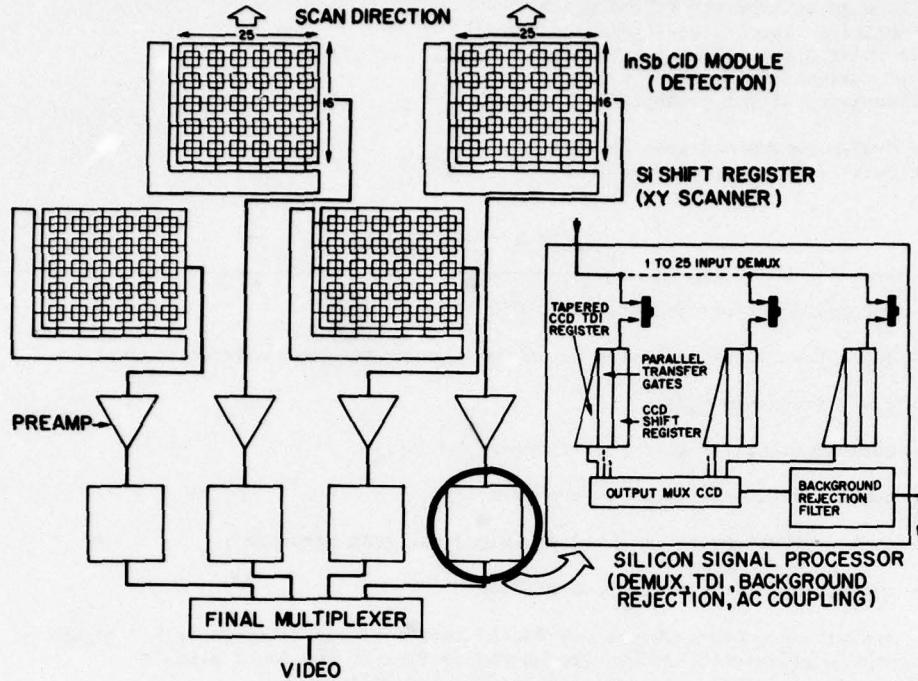


FIGURE 2 - Series-Parallel Scan CID focal plane array concept.

in 1A' is transferred to 1a at the same time that charge in 2A' is transferred to 3a, etc. After this parallel transfer, charge in 1a is moved to 2a, the charge in 3a to 4a, the charge in 1b to 2b, etc., and the readout process is repeated. With the design shown in Fig. 3 integration occurs after the third read out when the charge in 2A' is added to the charge in 2a which originated two read out sequences ago from detector 1A. A smaller ratio of sampling time to dwell time can be obtained by interleaving more CCD bits. The register 1a, 2a, etc. is tapered in width to be able to accomodate the integrated charge.

Since the scan rate and the clock frequency are synchronized the signals from all the detectors in a column will add coherently. The noise adds incoherently so that TDI provides a \sqrt{n} improvement in signal-

to-noise where n is the number of detectors in a column (16 as shown in Fig. 2). The Si signal processor chip used with the CID premultiplexer would be similar in design to that used with the sandwich approach except that since it is removed from the focal plane it can be much larger than the detector area relieving packing density and CCD well saturation limitations inherent in the sandwich approach.

EXPECTED PERFORMANCE OF SERIES PARALLEL SCAN CID

To be competitive, any IR focal plane must be able to operate background limited for IR backgrounds and scan frequencies of interest. Thus we must estimate the magnitudes of the competing noise sources for the configuration shown in Fig. 2. Sampling effects complicate the analysis. We will

consider three sources of noise: background noise arising from the statistical fluctuation of arriving photons, "kTC" noise arising from an uncertainty in charge on the preamplifier input capacitance and preamplifier noise arising from fluctuations in channel current of the input field effect transistor of the preamplifier.

The design parameters associated with any particular system are defined in Table 1.

TABLE I - DEFINITIONS

τ_s	- integration time any particular CID detector cell
τ_d	- dwell time, the time taken by an image point to cross a detector cell
f_c	- clock frequency τ_s/N_m
f_{\max}	- maximum signal frequency of interest = $0.8/\tau_d$
N_m	- number of CID detectors in a module
n	- number of detectors in a column (along the scan direction)
B	- output bandwidth of the preamplifier
N_B^*	- background photoelectrons per second into a single detector cell = $nA_d Q_B^*$ where Q_B represents the background photon flux at the focal plane A_d is the detector area and n is the quantum efficiency

Performance of the CID IR focal plane will be analyzed with reference to Fig. 4. Signal and background photons are converted into charge in the CID. The CID detectors all integrate this charge for a time τ_s after which the integrated charge is sampled by the readout process, converted into a voltage, and amplified by the preamplifier which has an output bandwidth B . The amplified voltage is resampled before being reconverted into charge for input into the CCD signal processor. The signal processor performs TDI and outputs a number of pulse trains corresponding to the photosignal seen by each column of the CID as the image is scanned over the module.

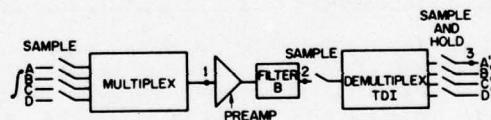


FIGURE 4 - Block diagram of the signal flow through a series-parallel scan CID focal plane array.

The input signal is reconstructed by a sample and hold process on these pulse trains. At point 3 after the sample and hold the signal will have the appearance of a staircase function, as shown in Fig. 5 for the case of uniform focal plane irradiance. The variation of signal height N shown in Fig. 5 represents noise.

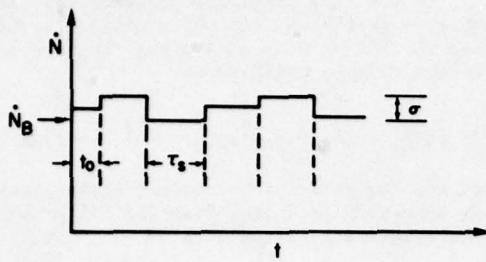


FIGURE 5 - Representative signal as a function of time after the sample and hold function shown in Fig. 4, for uniform focal plane irradiance.

As a matter of convenience, the output at point 3 will be referred back to the electrons/sec coming from an individual detector cell. σ is the standard deviation of the individual sample values at point 3 due to noise. We will assume that, after subtraction of the average value, there will be no correlation between these individual sample values as long as the input illumination is uniform. This is equivalent to assuming that before sampling the auto-correlation function of the input due to noise was zero for times larger than τ_s . This will be true for background and kTC noise and represents a reasonable approximation for preamplifier noise as long as the sampled values which are close together at point 3 did not come through the preamplifier in adjacent time slots. If the sampled values are not correlated the auto-correlation function of the signal at point 3 ignoring the DC component will be

$$\langle \dot{N}(t) \dot{N}(t-\tau) \rangle = \sigma^2 \text{ rect} \left[\frac{\tau - (t-t_0 - (m + \frac{1}{2}) \tau_s)}{\tau_s} \right] \quad (1)$$

where m is the largest integer such that $m \tau_s < (t-t_0)$ and rect represents the rectangular function which is unity between $\pm 1/2$ and zero elsewhere. The nonstationarity of the sampling process makes this auto-correlation function a function of both t and τ , however to calculate a power spectral density we can average this auto-correlation function over time to obtain:

$$\frac{1}{T} \int_0^T \langle \dot{N}(t) \dot{N}(t-\tau) \rangle dt = \sigma^2 \Lambda(\tau/\tau_s) \quad (2)$$

where Λ is the triangular function (zero at $\tau/\tau_s = \pm 1$). Ignoring the DC component the power spectral density (PSD) of the output staircase waveform will thus be

$$\text{PSD} = \int_{-\infty}^{\infty} \sigma^2 \Lambda(\tau/\tau_s) e^{i\omega\tau} d\tau = \sigma^2 \tau_s$$

$$\text{sinc}^2 \pi f \tau_s \quad (3)$$

The problem is one of estimating the value of σ^2 for background noise, kTC noise and preamplifier noise. If we wish to compare the variance at point 3 to the component variances associated with a single detector cell we can write:

$$\sigma^2 = \frac{\sigma_B^2}{n} + \frac{\sigma_{\text{kTC}}^2}{n} + \frac{\sigma_{\text{pa}}^2}{n} \quad (4)$$

where all the variances are normalized to the mean. The factor of n is due to the time delay and integration process. The uncertainty in the amount of collected background photons in an integration period τ_s from a single detector cell is just $\sqrt{\frac{n}{N_B} \tau_s}$ so that the variance in the rate of collection is just

$$\sigma_B^2 = \frac{\dot{N}_B}{\tau_s} \quad (5)$$

kTC noise is caused by an uncertainty in the charge on the capacitor C at the input to the preamp (point 1) before the detector cell charge is shifted under this capacitor for readout. This uncertainty in electronic charge is just $\sqrt{(2/3)kTC}$ which converted to a rate and referred back to the detector as electrons per second, gives a variance of

$$\sigma_{\text{kTC}}^2 = \frac{(2/3)kTC}{e^2 \tau_s^2} \quad (6)$$

where e is the electronic charge and k is Boltzman's constant.⁴

The preamplifier introduces noise which can be described by an equivalent input voltage noise with RMS value V_{rms} such that

$$V_{\text{rms}} = V_n B^{1/2} \quad (7)$$

where B is the bandwidth of the preamplifier circuit. Because the preamplifier is followed by a sampling process this value of B must be minimized regardless of the final value of f_{max} . The rms noise must be

made small at the sampling point. B must not be made too small since we must pass signal pulses through the preamplifier relatively unattenuated and since crosstalk between adjacent samples should be avoided. Thus there is a genuine tradeoff in selecting a value of B . For our calculation we will use:

$$B = 1.6 f_c = 1.6 \frac{N_m}{\tau_s} \quad (8)$$

With this choice, we can calculate an equivalent charge uncertainty at the input to the preamplifier and relate this to an uncertainty in the rate of electrons at the detector. This leads to a variance of:

$$\sigma_{pa}^2 = \frac{C^2 V_n^2 B}{e^2 \tau_s^2} = \frac{1.6 N_m C^2 V_n^2}{e^2 \tau_s^3} \quad (9)$$

For comparison with a signal in electrons/sec from a single detector cell we thus have:

$$PSD = \left[\frac{2N_B}{n} + \frac{4kTC}{3ne^2 \tau_s} + \frac{3.2N_m C^2 V_n^2}{e^2 \tau_s^2 \eta} \right]$$

$$\text{sinc}^2 \pi f \tau_s \quad (10)$$

To understand the tradeoff in the choice of τ_s relative to f_{max} we must consider the effect of the sampling process on signal as well as noise. The scanning process converts the spatial variations in the image into an AC signal which is added to the noise. Any single frequency AC signal, $N_s \sin^2 \pi f t$, coming from a single detector cell, will be attenuated by both the input integration function and the output sample and hold function so that its peak to peak value at the output (excluding aliased terms) on the average will be

$$\text{signal} = 2N_s \text{sinc}^2 \pi f \tau_s \quad (11)$$

From a noise point of view, a long τ_s is desirable because it makes background limited operation more likely. As $\tau_s \rightarrow 1/f$, however, the magnitude of the signal at the output will be reduced. A τ_s which is longer than optimum can thus reduce the background limited signal to noise ratio at f_{max} . For our example we will choose:

$$\tau_s = \frac{1}{3f_{max}} \quad (12)$$

such that a signal at f_{max} would be attenuated by a factor of 0.68 if no frequency boosting were employed.

In practice frequency boosting will be employed to flatten out the signal. In that case the PSD of the noise after the boosting process will be modified to

$$PSD' = \sigma^2 \tau_s / \text{sinc}^2 \pi f \tau_s \quad (13)$$

and the RMS value of the output after passing through a frequency boosting filter and then a bandpass filter will be

$$\begin{aligned} (\text{RMS noise})^2 &= \int_{f_{min}}^{f_{max}} PSD' df \\ &\approx 2\sigma^2 \tau_s f_{max} \left[1 + \frac{f_{max}^2 \pi^2 \tau_s^2}{9} \right] \end{aligned} \quad (14)$$

so that the use of $\tau_s = 1/(3f_{max})$ with a bandpass final filter implies a decrease in the background limited signal-to-noise ratio of 6% over that which would be obtained for $\tau_s \ll 1/f_{max}$. In practice with an imaging system the bandpass of the final filter is influenced by the eye acting as a spatial filter for signals on the display.

If we desire $f_{max} = 0.8/\tau_d$ (representative for an imager design) we can achieve $\tau_s = 1/3f_{max}$ by a 3 to 1 interleave in the TDI register and a center to center spacing to detector size ratio, y/x of 1.25.

With this relationship between τ_s and f_{max} and with frequency boosting we have for the CID

$$\begin{aligned} (\text{RMS noise})^2 &= \left[\frac{2N_B}{n} + \frac{4kTC f_{max}}{e^2 n} \right. \\ &\quad \left. + \frac{28.8C^2 V_n^2 N_m f_{max}^2}{e^2 n} \right] f_{max} \quad (15) \end{aligned}$$

For background limited operation the first term should dominate the remaining two. We will define f^* for the CID to be that value of f_{max} for which the first term equals the sum of the remaining two terms. Without correlated double sampling, C.D.S., kTC noise dominates and

$$f^* = \frac{N_B e^2}{2kTC} \quad (16)$$

whereas if kTC noise is suppressed by correlated double sampling we will have:

$$f^* = \left[\frac{N_B e^2}{(14.4)V_n^2 C^2 N_m} \right]^{\frac{1}{2}} \quad (17)$$

Without excess noise in the preamplifier, channel thermal noise of the input FET will dominate and V_n will be given by $V_n = (8/3 kT/g_m)^{1/2}$ where g_m is the transconductance of the input FET. g_m can be as high as 8000 μhos giving

$$V_n = 5.95 \times 10^{-10} \text{ volts}/\text{Hz}^{1/2} \text{ at } 77^\circ\text{K} \quad (18)$$

In these f^* relationships for the CID, C is the total capacitance between the input to the preamplifier (at point 1) and ground. C includes stray capacitance, the input capacitance to the preamplifier (5 pF), and the capacitance of the column readout line. If nondestructive CID readout techniques are used with two surface electrodes per detector then this latter capacitance will be limited by the capacitance of half the photoactive area associated with a column of the CID module. As the number of detectors in a column is increased to make the module size larger C will thus increase. Assuming the same module aspect ratio as shown in Fig. 2 (16/25), a stray capacitance of 1 pF, InSb photoactive area capacitance of 0.1 pF/mil² and a full detector cell size of 4 mil², we can write

$$C = (6 + .16 \sqrt{N_m}) \text{ pF} \quad (19)$$

which is 9.2 pF for $N_m = 400$.

Using the above relationship for C we have plotted f^* as a function of N_B for several values of N_m in Fig. 6. In all cases we have adjusted the clock frequency such that $\tau_s = 1/3f^*$. With kTC noise there is a minimum number of background photons which must be collected per sample time to make the device background limited. For $C = 9.2$ pF this number is 2.5×10^5 electrons. If the limitation is kTC noise, the dependence of f^* on N_m is not strong.

With a careful implementation of the non-destructive CID readout techniques introduced by Michon and Burke in their parallel injection readout scheme it should be possible to implement correlated double sampling (CDS) as shown in Fig. 7, and remove the effect of kTC noise.^{6,7} The removal of kTC noise by correlated double sampling (CDS) can provide approximately an order of magnitude increase in f^* for devices operating in the 3-5 μm region where considering different applications N_B can vary from $1 \times 10^8/\text{sec}$ to $1 \times 10^{10}/\text{sec}$ depending on the exact choice of spectral filtering and F/no.

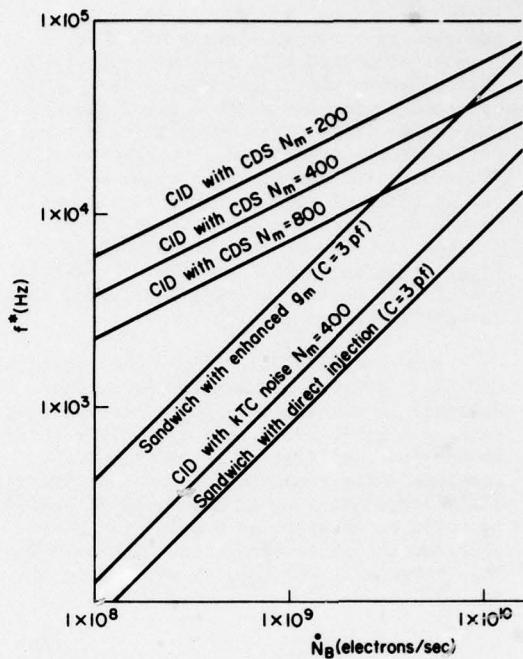


FIGURE 6 - The maximum signal frequency for which various FPA configurations will be background limited as a function of the photoelectron generation rate at a single detector in the array.

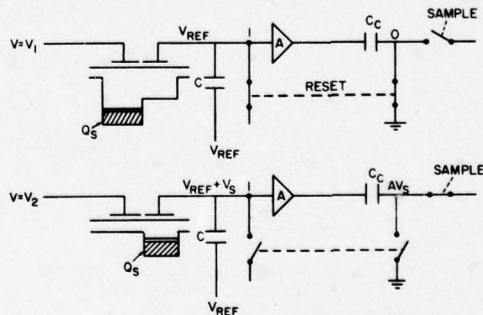


FIGURE 7 - Technique for implementing correlated double sampling with a non-destructive CID readout. The reset switch is opened, V_1 changes to V_2 transferring the signal charge, Q_S , and then the output is sampled.

kTC noise will lead to an uncertainty in the charge on the capacitor C before the read cycle, however if the resistance between the point 1 and ground is high enough after the reset switch is opened, this total charge will not have time to change before the signal charge is "sloshed" under the readout electrode and the change in voltage caused by this transfer of charge is sampled at the output. Since only the change in voltage caused by the transfer of signal charge is measured at the output, kTC noise will not be observed. As long as the capacitance of a single cell is a small portion of the total capacitance between point 1 and ground this change in voltage V_s will be Q_s/C .

Examination of Fig. 6 for the CID with CDS ($N_m = 400$) shows that for background currents of 10^9 electrons/sec corresponding to $A_d = 4 \text{ mil}^2$, $\eta = .7$, and $Q_B = 5.7 \times 10^{13}$ photons/cm², an f_{\max} of 10 kHz should be possible while remaining background limited. Clock frequencies of 12 MHz would be needed; τ_d could be as short as 8×10^{-5} sec for background limited operation. The relationship between f_c and f_{\max} is determined by eq. (12).

$$f_c = 3 N_m f_{\max} \quad (20)$$

This relationship is plotted in Fig. 8 for representative values of N_m . Larger values of N_m would reduce the number of interconnects per detector. However, in general the use of a larger N_m reduces f^* and for a given f_{\max} may increase the required clock frequency to unobtainable values.

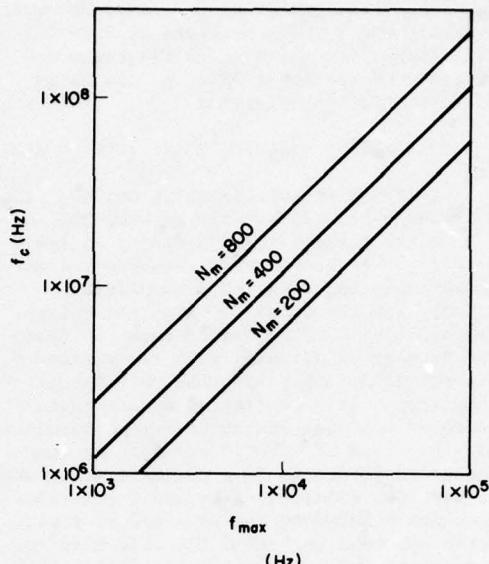


FIGURE 8 - Clock frequency, f_c , as a function of the maximum signal frequency of interest, f_{\max} for various CID module sizes.

NOISE LIMITATIONS WITH DIRECT INJECTION (SANDWICH STRUCTURE)

In the previous section we have developed estimates of f^* for the CID F.P.A. structure which uses premultiplexing. In this section for comparison purposes we will estimate f^* for a sandwich FPA structure which uses direct injection to inject photogenerated charge into CCD TDI registers. A comprehensive treatment of signal-to-noise ratio at the output of a direct injection based FPA has been developed in refs. 1 and 2. It was determined that the direct injection input circuit itself is responsible for the most stringent limitation on f^* . In the simplified treatment provided here, we will concentrate on the competition between noise arising from the input circuit and noise arising from fluctuations in the background flux. As a first approximation, the effects of sampling will be neglected. Minor correction factors due to sampling will be derived in Appendix A.

The input structure is shown in Fig. 9. The detector anode is connected to a p type diffusion. During an integration period τ_s , V_{sc} is held at a fixed bias to deplete the vicinity of the input diffusion while the screen electrode, V_{st} , is biased more negatively to create a potential well. Photocurrent from the detector is injected from the diffusion and stored beneath V_{st} . At the proper time by changing ϕ_T this stored charge is transferred into the CCD TDI register. Charge is then transferred down the register and the cycle is repeated.

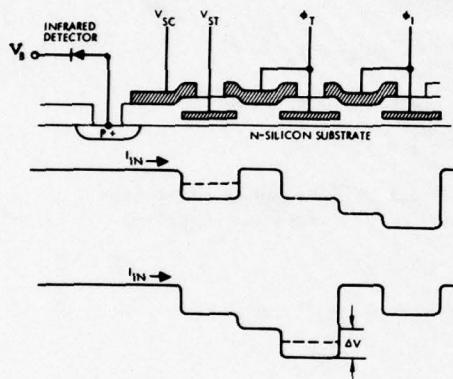


FIGURE 9 - Direct injection input circuit structure.

The AC equivalent circuit of Fig. 10 can be used to analyze the circuit operation. The input structure is treated as a grounded gate MOSFET where the input diffusion, "S", acts as a source, V_{sc} as a gate and the potential well under V_{st} as a virtual drain. At the low photocurrents of interest this MOSFET will usually operate in the sub-threshold or weak inversion regime where

$$g_m = \frac{1}{2} \frac{e}{kT} I \quad (21)$$

where I is the total D.C. current flowing from the source to the drain.^{8,9,10} At higher currents $g_m \propto I^{1/2}$. In Fig. 10, C is the combination of all input shunt capacitances and will be about 3 pF for a 2 mil square InSb photodiode. i_s is the shot noise of the background generated photocurrent, i_1 is the noise current due to shunt resistances and i_2 represents the MOSFET channel thermal noise. V_{gs} is the voltage between the gate and the source. Note that the current generator $g_m V_{gs}$ acts like a resistance in series between the detector and an ideal processor.

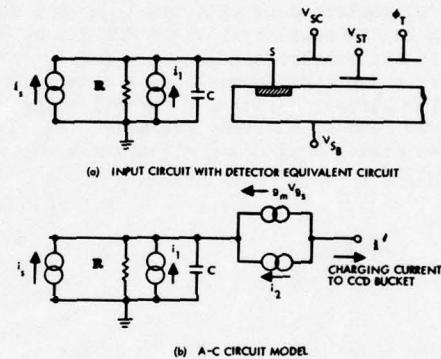


FIGURE 10 - AC equivalent circuit with direct injection.

An analysis of this equivalent circuit gives an expression for the output current power spectral density.

$$\begin{aligned}
 PSD_1 &= \left| \frac{g_m R}{(1+g_m R)(1+j\omega RC(1+g_m R)^{-1})} \right|^2 \\
 &\quad (e^2 N_B + 2kT/R) \\
 &\quad \left| \frac{1+j\omega RC}{(1+g_m R)(1+j\omega RC(1+g_m R)^{-1})} \right|^2 \\
 &\quad ((4/3)kTg_m) \tag{22}
 \end{aligned}$$

where R is the effective resistance between S and ground. To avoid Johnson noise limitations we must assure that R is large enough. If we arrange the circuit such that $R \gg 2kT/e^2 N_B$, f^* will be limited by channel thermal noise. If Johnson noise can be neglected we will have $g_m R \gg 1$ as long as the equivalent input MOSFET would be in the subthreshold regime (for $I = eN_B$). Under these conditions f^* can be defined as the largest value of f for which the second term in the PSD_1 dominates the first term. Neglecting effects due to the sampling process f^* is thus given by:

$$f^* = \frac{\sqrt{2eN_B g_m}}{2\pi C \sqrt{8/3 kT}} \tag{24}$$

If the value from Eq. 21 is used for g_m then:

$$f^* = \frac{\sqrt{3/2} e^2 N_B}{4\pi C k T} \left[\frac{I}{eN_B} \right]^{1/2} \tag{25}$$

As large a value of g_m as possible is desired. Use of the subthreshold expression for g_m as a function of I could be optimistic for $I \geq 1 \times 10^9$ amps.

With the most straightforward implementation of direct injection R is the detector resistance and $I = eN_B$. f^* for this case is plotted in Fig. 6 as direct injection with $C = 3pF$. If I is greater than eN_B , g_m enhancement can occur and f^* will be increased. We estimate that I can be increased by a factor of 30. Assuming the subthreshold expression for g_m vs. I , this leads to a maximum improvement ratio

of 5.5 for f^* which is plotted in Fig. 6.

Another approach to a higher f^* with direct injection is to use a photoconductor to provide D.C. gain to enhance I . The smaller capacitance of a photoconductor would by itself lead to an increase in f^* . As an example we will consider an extrinsic Si photoconductor with the properties listed in Table II.¹¹

TABLE II - EXTRINSIC PHOTOCONDUCTOR PROPERTIES.

$$\begin{aligned}
 E_{\max} &= 2500 \text{ V cm}^{-1} \\
 \mu &= 6 \times 10^3 \text{ cm}^2 \text{V}^{-1} \text{ sec}^{-1} \\
 \tau &= 2 \times 10^{-8} \text{ sec} \\
 L &= 0.1 \text{ cm (thickness and inter-electrode spacing)} \\
 C &= 0.5 \text{ pF} \\
 A_d &= 2.5 \times 10^{-5} \text{ cm}^2
 \end{aligned}$$

With these properties the D.C. gain $G_O = (E\mu\tau/L)$ will be 3 making $I/eN_B = 3$.

Assuming a saturated A.C. gain of 1/2 and $R \gg 8kT/e^2 N_B$ referring to Eq. 16, f^* for the photoconductor will be

$$f^* = \frac{1}{2} \frac{\sqrt{3/2}}{4\pi C k T} e^2 N_B (G_O)^{1/2} \tag{26}$$

which for $G_O = 3$ and $C = .5pF$ represents an improvement in f^* over the 3pF photodiode of a factor of 5.2 (at the same T). Thus f^* for a photoconductor would be similar to our estimate of f^* for a photodiode with g_m enhancement. The use of an A.C. gain of 1/2 in the above expression

will be justified as long as the dielectric relaxation time, τ_p , is such that

$$f_p = \frac{1}{2\pi\tau_p} \ll f^* \quad (27)$$

i.e., as long as

$$\frac{\epsilon\mu\tau N_B}{2\pi A_d L \epsilon} < \frac{1}{2} \frac{\sqrt{3/2} e^{2\epsilon} N_B (\frac{E_m \mu \tau}{L})^{1/2}}{4\pi C k T} \quad (28)$$

For the values in Table II at 60°K

$$f_p/f^* = \frac{(G_o)^{1/2}}{E_m \epsilon} \frac{4CkT}{\sqrt{3/2} e A_d} = 0.23 \quad (29)$$

so that the assumption of a saturated photoconductive gain of 1/2 at $f = f^*$ is justified.¹²

The 3-5 μm extrinsic photoconductor will give superior f^* performance to the photodiode; however there will be a temperature of operation penalty and since absorption lengths tend to be long there will be quantum efficiency vs. crosstalk tradeoffs for a 3-5 μm FPA made with extrinsic photoconductors.

All of the above estimates for f^* with direct injection ignore sampling effects and are therefore only strictly true for sampling rates such that $\tau_s \ll 1/f^*$. In practice since CCD bits cannot be made an order of magnitude smaller than the detector size this is unlikely to be the case if f^* approaches $f_{max} = 0.8/\tau_d$. In the appendix we have considered the effects of sampling for a more realistic case where $\tau_s = 1/3f^*$ and show that the degradation in f^* from the effects of sampling will be about 16%.

CONCLUSIONS

Series parallel scan with small InSb CID modules appears to be a convenient moderate cost approach to IR focal plane arrays for the 3-5 μm region. Our calculations suggests that the use of CID for pre-multiplexing has the potential of providing a higher f^* in the 3-5 μm region than any of the focal plane array approaches that we

have analyzed which use direct injection with the possible exception of direct injection with an extrinsic photoconductor including g_m enhancement. To realize this projected f^* performance high speed (10-20 MHz) CID readout schemes which include correlated double sampling must be developed.

None of the FPA designs we have analyzed appear readily capable of providing f^* high enough for a TV compatible IR imaging system in the 3-5 μm region (which requires an f^* of = 30 kHz). With the higher background fluxes of the 8-12 μm region extrinsic photoconductor FPA's using direct injection should not be seriously limited by f^* problems if the imaging systems use a parallel scan.

APPENDIX A

DEGRADATION IN f^* WITH DIRECT INJECTION DUE TO SAMPLING

Unless $\tau_s \ll 1/f$ the integration and sampling which occurs at the output of a direct injection circuit with a sandwich type FPA structure will have some effect on the signal-to-noise ratio. Due to the complex frequency dependence of the noise power spectral densities before the sampling we will take a different approach to calculating the effect of aliasing than was used with the CID.

If f_s is the sampling frequency the noise current power spectral density after integration and sampling, PSD_I , will be

$$PSD_I(f) = \sum_{-\infty}^{\infty} PSD_I(f+nf_s) \text{sinc}^2 \frac{2\pi f + nf_s}{f_s} \quad (A-1)$$

where $\text{sinc}x \equiv (\sin x)/x$ and where $PSD_I(f)$ is the power spectral density before integration and sampling. In a practical case we could adjust f_s such that

$$f_{max} = f_s/3 \quad (A-2)$$

so that

$$\text{PSD}_1(f_{\max}) = 0.68 \text{ PSD}_1(f_{\max}) \\ \left[1 + 0.25 \frac{\text{PSD}_1(2f_{\max})}{\text{PSD}_1(f_{\max})} + \right. \\ \left. 0.06 \frac{\text{PSD}_1(4f_{\max})}{\text{PSD}_1(f_{\max})} \dots \right] \quad (\text{A-3})$$

With the expression for PSD_1 from Eq. 22 the term in brackets represents an increase of about 55% in channel thermal noise power and 10% in photon noise power. With these sampling effects included, the frequency $f_{\max} = f^*$ at which channel noise power exceeds photon noise power is 16% lower than that predicted by the non-sampling approximation. Further the signal-to-noise ratio at the corrected f^* is approximately 5% lower than that predicted at the uncorrected f^* with the non-sampling approximation. This decrease is due to increased photon noise due to noise folding.

While one would like to avoid the effects of noise folding, the geometry of the array will determine the maximum sample rate relative to the dwell time. If n_d is the maximum number of CCD bits that can be placed in a space equal to the detector width in the scan direction then:

$$\tau_d = n_d \tau_s \quad (\text{A-4})$$

and if

$$f_{\max} = \frac{0.8}{\tau_d} \quad (\text{A-5})$$

we will have

$$f_s = \frac{1}{\tau_s} = \frac{n_d}{0.8} f_{\max} \quad (\text{A-6})$$

so that if n_d is limited to 2.4 for a 2 mil detector

$$f_s \leq 3f_{\max} \quad (\text{A-7})$$

An acceptable yield with smaller CCD bits would allow less aliasing and noise folding. The inter-detector spacing would of course in all cases be adjusted to provide an integer number of CCD bits between inputs.

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INJECTION EFFICIENCY IN HYBRID IRCCD'S

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ABSTRACT. In this paper an equivalent circuit approach is used to model the direct injection hybrid IRCCD. The injection efficiency is calculated as a function of frequency up to 10 MHz for different values of detector and CCD input circuit parameters. The dynamic effect of the total detector current on the injection efficiency is taken into account by a first-order correction. For a typical case, a photodiode with a resistance of $5K\Omega$, a capacitance of $20pF$ and CCD input transconductance of $500\mu mho$ and an input capacitance of $1pF$, an injection efficiency of $\sim 67\%$ is calculated at the minimum read frequency of 1.34 MHz .

I. INTRODUCTION

In the direct injection IRCCD, the photo-generated charge is directly introduced into the CCD shift register [1-5]. Since this is in effect a DC coupled system, only IR detectors which exhibit relatively small DC currents (e.g. photovoltaic, extrinsic detectors) can be coupled to the CCD due to the latter's limited charge handling capacity. A critical parameter of the direct injection IRCCD is the injection efficiency, defined as the ratio of the charge introduced into the CCD to the total charge generated by the detector. In this paper, the frequency dependence of the injection efficiency is examined as a function of the detector and CCD input parameters. Since different IR focal plane scanning organizations (e.g. staring, parallel, serial) operate at different rates (from 30 Hz to 6 MHz) it becomes very important to be able to predict the injection efficiency at the appropriate frequency in order to calculate the overall performance of the IRCCD.

The basic direct injection concept is illustrated for a hybrid IRCCD consisting of a (Pb,Sn) Te photo-diode and an n-channel CCD (see Fig. 1). The (Pb,Sn) Te/PbTe heterostructure [6] is particularly attractive for a hybrid IRCCD array since integration can be achieved in a

relatively simple sandwich structure with full use of the detector active area and requiring no interconnects (see Fig. 2). As shown in Fig. 1, the IR diode is connected in parallel to a silicon diode which serves as an input tap to the CCD. The first MOS gate, V_G , serves to reverse bias both diodes. While the charge accumulates under the storage gate V_S , it is isolated from the CCD channel by the transfer gate V_T . After one read time, t_R , V_T is biased into inversion and the accumulated charge is transferred into the CCD channel.

II. EQUIVALENT CIRCUIT MODEL

To evaluate the direct injection efficiency, the equivalent load presented to the detector by the CCD is first considered. The CCD input stage is effectively a MOSFET with the input diffusion representing the source and the potential, ϕ_s , of the inverted surface under the V_S electrode, representing the drain. Since we want the charge to accumulate under the storage electrode, we need $V_S > V_G$, thus driving the MOSFET into saturation. However, the saturated drain current is not free to take the value it normally would in the grounded source MOSFET configuration since it is driven by the detector current. This results in an increase in the source potential required

to satisfy the appropriate current flow. Under these conditions the gate and drain voltages must be referred to this effective source potential. Since we are in the saturation region, the drain conductance $g_D = \frac{\partial I_D}{\partial V_D} = 0$ and the input conductance seen by the detector is given by the variation of the drain current with changes in the gate-to-source voltage, V_{GS} , or the transconductance g_m . It should be pointed out, however, that as charge accumulates under V_S , the surface potential decreases to the point where the drain-to-source potential is lower than the gate-to-source potential thus forcing the MOSFET out of the saturation regime. As the drain-to-source potential decreases further the drain current will decrease accordingly, resulting in a potentially very useful self-limiting action. The CCD input capacitance is the parallel combination of the source diode capacitance, channel capacitance and gate-to-source capacitance with the latter being the dominating factor [8].

The equivalent circuit for the detector/CCD input circuit can thus be simply shown as in Figure 3, where i_D is the detector current (signal + background + dark current) and G_D and C_D are the detector conductance and capacitance. The current flow in the circuit is then given by

$$i_D = i_1 + i_2 \quad (1)$$

$$i_1 [G_D + SC_D]^{-1} = i_2 [g_m + SC_{GS}]^{-1} \quad (2)$$

where i_2 is the current injected into the CCD. The injection efficiency, η_{INJ} , defined as the ratio of the current flowing into the CCD over the total detector current, can then be obtained from Equations (1) and (2):

(3)

$$\eta_{INJ} = \frac{i_2}{i_D} = \frac{g_m}{g_m + G_D} \cdot \frac{A}{\left[1 + \omega^2 \left(\frac{C_D + C_{GS}}{G_D + g_m} \right)^2 \right]} \quad (3)$$

where A is given by:

$$A = \sqrt{1 + \omega^2} \cdot \frac{2C_{GS}^2 \left(\frac{G_D}{g_m} \right) + \frac{1}{g_m^2} |C_{GS}^2 G_D^2 + g_m^2 C_D^2 + [(C_{GS} + C_D)^2 C_{GS}^2 \omega^2]|}{(G_D + g_m)^2} \quad (4)$$

In the two frequency limits the injection efficiency simplifies to the expected resistance and capacitance divider network:

$$\omega \rightarrow 0 \quad \eta_{INJ} = \frac{g_m}{g_m + G_D} \quad (5)$$

$$\omega \rightarrow \infty \quad \eta_{INJ} = \frac{C_{GS}}{C_D + C_{GS}} \quad (6)$$

In addition, for reasonably good photodiode characteristics, the injection efficiency is well approximated in the submegahertz range by

$$\omega \leq 1 \text{ MHz} \quad \eta_{INJ} = \frac{\eta_{INJ}(0)}{\left[1 + \omega^2 \left(\frac{C_D + C_{GS}}{g_m + G_D} \right)^2 \right]^2} \quad (7)$$

where $\eta_{INJ}(0)$ is defined by Equation (5).

III. HYBRID IRCCD PARAMETERS

For a (Pb,Sn) Te/PbTe diode sensitive over the entire 8-12 μm region, the background photon flux is roughly 1×10^{17} photons/cm⁻² sec which for an optical area of 5×5 mils² results in a background current of $\sim 2 \mu\text{A}$. The mesa structure of the diode results in an electrical area of the detector smaller than the optical area, giving rise to effective optical gain. The electrical properties of the device are, therefore, a function of the electrical area one can obtain through the mesa etching. Under these conditions the detector parameters vary typically from $1\text{K}\Omega$ to $10\text{K}\Omega$ for R_D and 10 to 100 pF for C_D at an effective reverse bias of the order of 100 mV [6]. The total detector current at this bias is taken to vary from $10 \mu\text{A}$ ($R_D = 10\text{K}\Omega$) to $100 \mu\text{A}$ ($R_D = 1\text{K}\Omega$).

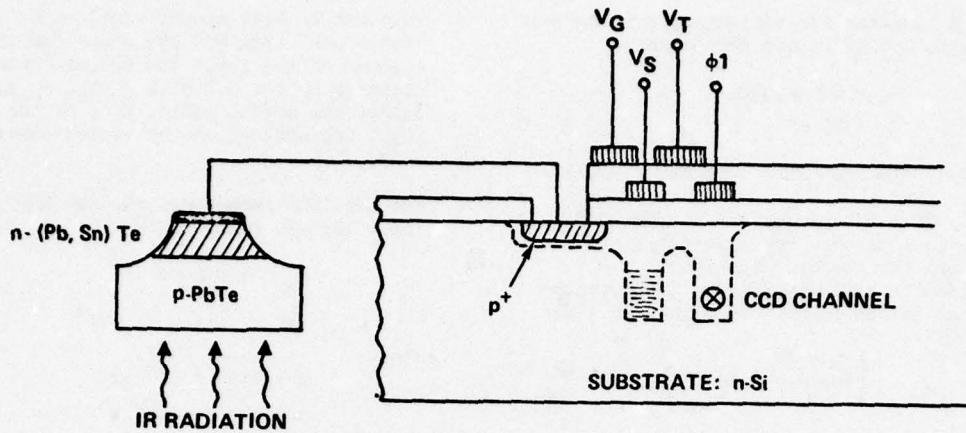


Fig. 1 Hybrid IRCCD: Direct Injection from (Pb, Sn) Te/PbTe Heterodiode.

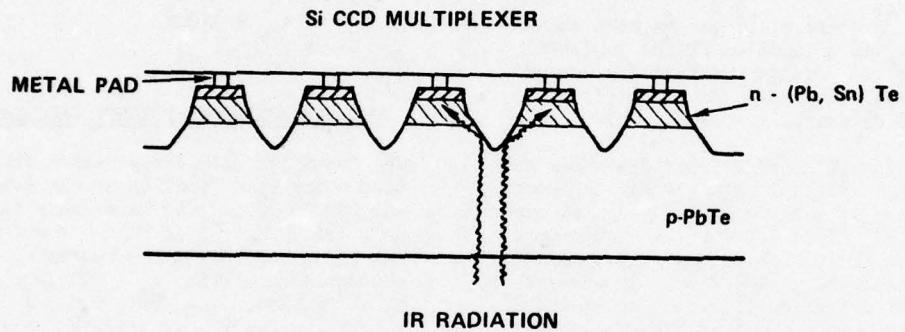


Fig. 2 Hybrid IRCCD Two Chip Device Using Inverted Heterojunction Detector Array.

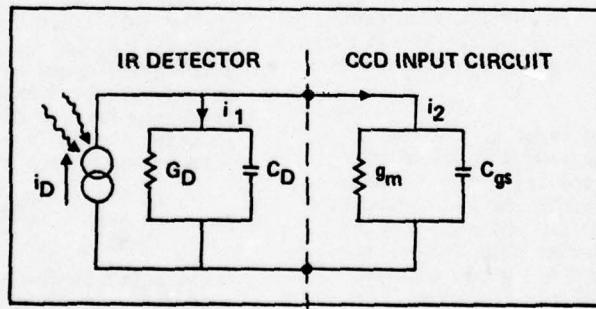


Fig. 3 Direct Injection Equivalent Circuit Model.

As a baseline for the detector parameters the following values were chosen:

$$G_D = 200 \mu\text{mho}$$

$$C_D = 20 \text{ pF}$$

and a total detector current of $20 \mu\text{A}$.

The CCD input parameters can be used within a certain range as design parameters for the optimization of the injection efficiency. The transconductance in the saturation region is given by [7]

$$g_m = \left(\frac{2Z \mu_n C_{ox}}{L} I_{D,SAT} \right)^{\frac{1}{2}} \quad (8)$$

where Z is the width of the channel, L is the length, μ_n is the electron mobility at the temperature of operation, C_i is the insulator capacitance per unit area and $I_{D,SAT}$ is the saturated drain current or i_2 . Therefore, it can be seen that since g_m is a function of the injected current the injection efficiency depends both statically on g_m as in eq (3) as well as dynamically as in eq (8).

As the injection efficiency decreases with frequency, the injected current decreases resulting in a lower effective g_m as given by eq (8). This results in a lower η_{INJ} as by eq (3) which in turn results in a still lower g_m and so on. To account for this iterative effect, a first order correction given by the first iteration was used in the calculation of g_m and then η_{INJ} . In the case of BLIP-limited detectors where the background current is the dominant detector current, the transconductance and thus the injection efficiency would be related to the background photon flux [3].

Both the transconductance g_m and the capacitance C_{gs} are also a function of the dimensions of the input tap circuit. g_m is directly proportional to the aspect ratio of input channel, while C_{gs} is a function of the overlap area between the source diffusion and the input gate as well as of the insulator thickness. Since the photodiode capacitance, C_D , is generally much larger than C_{gs} , the input tap channel width can be increased to improve the transconductance without greatly affecting the total capacitance.

This can be best accomplished in a "razorback" type CCD [9] where the dimensions of the input tap are not entirely dictated by the CCD cell size. In particular, the aspect ratio, Z/L , of the input tap channel can be varied considerably.

The baseline parameters for the CCD input tap are taken to be

$$g_m = 500 \mu\text{mho}$$

$$C_{gs} = 1 \text{ pF}$$

where

$$Z = 2.54 \times 10^{-2} \text{ cm}$$

$$L = 2.54 \times 10^{-3} \text{ cm}$$

$$Z/L = 10$$

$$\mu_n (77^\circ\text{K}) = 4 \times 10^4 \text{ cm}^2/\text{V-sec}$$

(see ref. [10])

$$C_i = 2.3 \times 10^{-8} \text{ F/cm}^2$$

$$t_{ox} = 1500 \text{ \AA}$$

$$i_D = 20 \mu\text{A}$$

IV. INJECTION EFFICIENCY CALCULATIONS

The injection efficiency versus frequency is plotted as a function of the detector and CCD input circuit parameters in Figures 4-6. Curve B of Fig. 4 shows η_{INJ} vs. f for the baseline parameters chosen in Sec. III: $g_m = 500 \mu\text{mho}$, $G_D = 200 \mu\text{mho}$, $C_D = 20 \text{ pF}$, $C_{gs} = 1.0 \text{ pF}$. As pointed out in Sec. III, g_m will vary with the level of the injected current and, therefore, with frequency. The g_m parameter shown in Figures 4-6 represents the DC value, but in the calculations the corrected g_m is used at each frequency point. The arrow on this curve, as well as the others, indicates the minimum read frequency for the given IRCCD parameters at which direct injection can take place without saturating the CCD capacity

$$f^* = \frac{i_2(f)}{Q_{MAX}} = \frac{\eta_{INJ}(f) i_D}{Q_{MAX}} \quad (9)$$

where $i_2(f)$ is the current actually injected at a given frequency and Q_{MAX} is the maximum charge the CCD can store, taken here to be 10 pC . Equation (9) was solved iteratively since η_{INJ} is itself a function of frequency. For the baseline

case, curve B in Figure 4, an $f^* = 1.3$ MHz and $\eta_{INJ}(f^*) = 0.67$ are calculated. The other curves in Fig. 4 are for different values of the CCD input circuit parameters generated by varying the input tap channel width. In this manner both the aspect ratio and the total area of the input channel are varied, thus affecting simultaneously the transconductance and the input capacitance. Curve A was generated for $Z/L = 20$, resulting in $g_m = 1 \mu\text{mho}$ and $C_{gs} = 2\text{pF}$. Since the injection efficiency is now higher resulting in a larger injected current, the minimum read frequency also increases to $f^* = 1.6$ MHz where $\eta_{INJ} = 0.8$. If the IRCCD is part of a serially-scanned focal plane operating at a TV compatible rate, the injection efficiency at say 5 MHz is $\eta_{INJ} \approx 0.55$ for Curve A and $\eta_{INJ} \approx 0.27$ for Curve B. It, therefore, becomes advantageous to have a serial-parallel system where one can lower the frequency by the number of channels and thus approach as much as possible the optimum frequency of operation, f^* . It is also obvious by comparing the curves of Fig. 4 that a large W/L ratio, $\gtrsim 10$, and the resulting high transconductance is required in order to obtain a reasonable level of injection efficiency, $\gtrsim 0.5$.

In Fig. 5 the injection is plotted versus frequency for four different values of detector conductance. The detector leakage current is assumed to be proportional to the detector conductance at these levels. This in turn affects g_m , since it is proportional to the square root of the injected current. Curve B on Fig. 4 is the same as in the preceding figure, namely the baseline case. If the G_D is reduced by a factor of 2, as in Curve A, the optimum frequency of operation improves almost a factor of two to $f^* = 750$ KHz and $\eta_{INJ}(f^*) = 0.74$. It is interesting to note that if one is constrained to operate at frequencies above 4MHz, it becomes advantageous to use a detector with a higher conductance since it will have a higher η_{INJ} in that frequency range.

Finally in Fig. 6, the effect of varying the detector capacitance on η_{INJ} vs. f is shown. The effect of a decrease of a factor of two from the baseline value of C_D can be seen by comparing curves A and B.

The f^* value increases by only 5% to 1.4 MHz where $\eta_{INJ}(f^*) = 0.7$. However, as expected, a much stronger effect is observed at higher frequencies where the role of the capacitance begins to dominate. At 5 MHz, there is about a factor of two difference in injection efficiency between the two top curves. Curves C and D show that for increases in C_D to respectively 50pF and 100pF the performance is progressively degraded. Even though the f^* decreases with C_D , η_{INJ} at f^* also decreases considerably and in the high frequency regime, $f > 2$ MHz, the η_{INJ} becomes quite small, < 0.25 .

V. CONCLUSIONS

An equivalent circuit model of the direct injection hybrid IRCCD has been presented and analyzed. Calculations have been performed to determine the frequency dependence of the injection efficiency as a function of four basic parameters: detector conductance and capacitance, CCD input tap transconductance and capacitance. Performance at the minimum frequency of operation has been established as a function of the same parameters. For the baseline parameters of $g_m = 500 \mu\text{mho}$, $G_D = 200 \mu\text{mho}$, $C_D = 20\text{pF}$ and $C_{gs} = 1\text{pF}$, an $f^* = 1.34$ MHz and $\eta_{INJ}(f = f^*) = 0.67$ are calculated.

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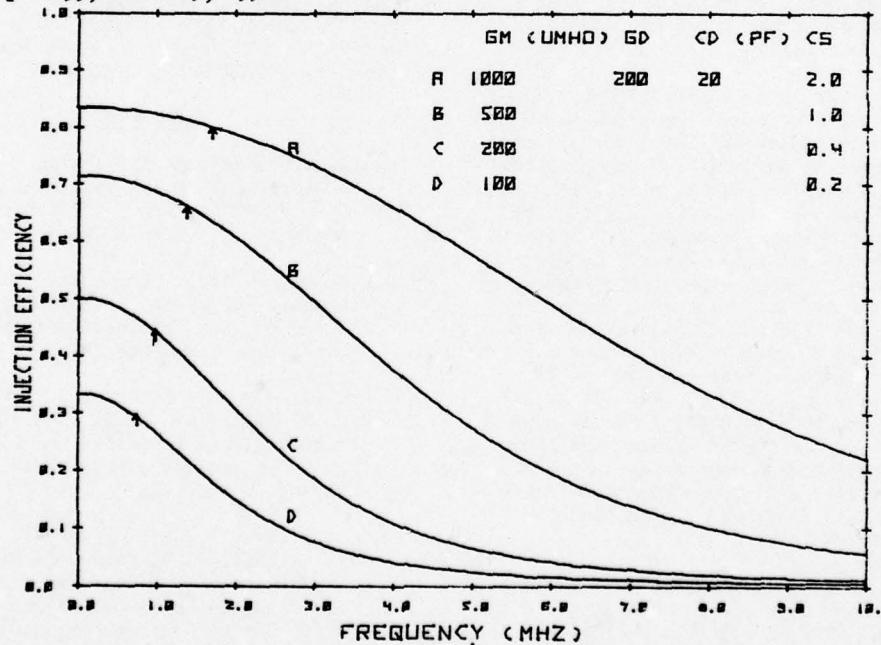


Fig. 4 Injection Efficiency vs. Frequency for Different Values of Input Transconductance and Capacitance

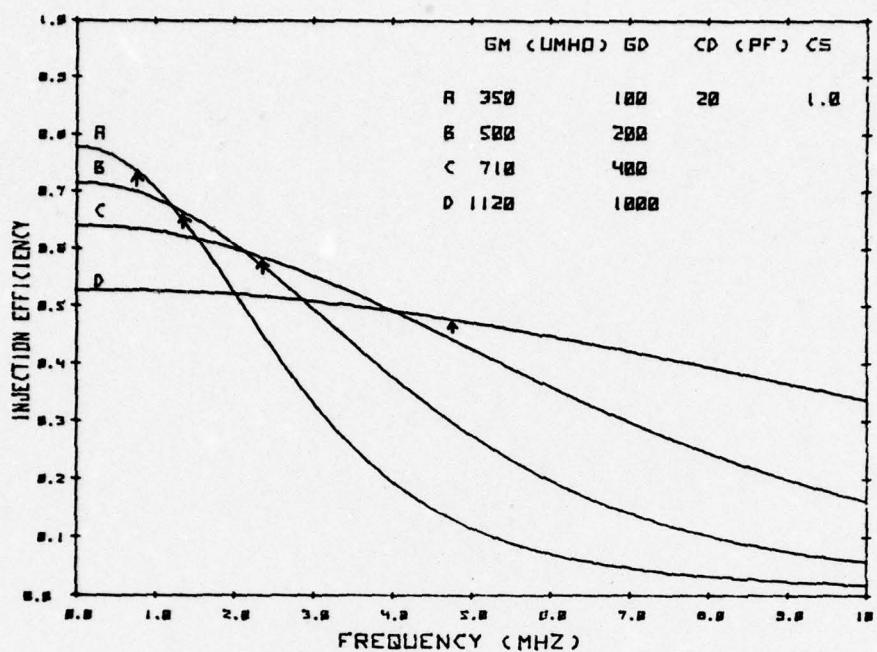


Fig. 5 Injection Efficiency vs. Frequency for Different Values of Detector Conductance

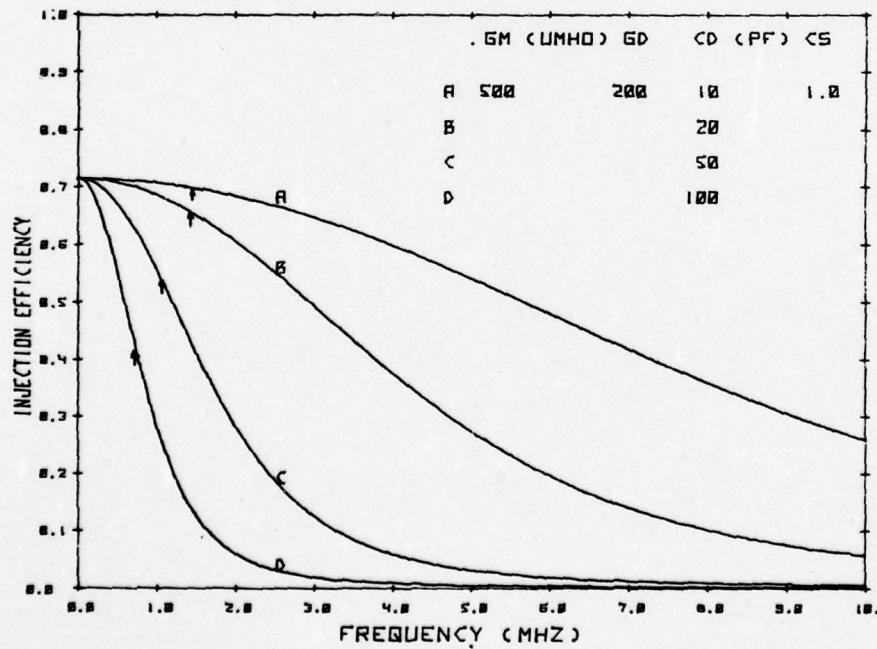


Fig. 6 Injection Efficiency vs. Frequency for Different Values of Detector Capacitance

CID Imaging - Present Status and Opportunities *

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ABSTRACT CID image sensors, which employ intra-cell transfer and injection to sense photon-generated charge at each image site, have evolved from relatively low density sequential-injection structures to high-speed, high-density arrays capable of non-destructive readout. A more recent readout method, termed Parallel Injection, separates the functions of signal charge detection and injection. The level of signal charge at each sensing site is detected during a line scan, and, during the line retrace interval, all charge in the selected line is injected. The injection operation is used to reset (empty) the charge storage capacitors after line readout has been completed. Non-destructive readout is possible by deferring the injection operation.

The parallel injection technique is well adapted to TV scan formats in that the signal is read out at high speed, line-by-line. A 244 line by 248 element TV-compatible imager employing this technique has been constructed and operation demonstrated.

An additional improvement in the CID structure has been the replacement of the opaque aluminum electrodes with transparent conductors. Devices fabricated in this way have achieved quantum efficiencies in the order of 70% over the spectral range of 4000A to 8000A; front illuminated.

The coincident voltage selection method is not constrained to sequential array scanning. Spiral, sub-raster, or "random" scanning can be implemented with appropriate row and column selection circuitry. The capability of repeated readout, during or subsequent to exposure, allows a number of system functions not previously possible. Time exposures can be monitored via NDRO and terminated when the desired information has been acquired. Signal-to-noise performance can also be improved through repeated readout of a stored image.

INTRODUCTION

In contrast to CCD imagers, in which the signal charge is transferred to the edge of the array for sensing, the CID approach confines this charge to the site during sensing. Site addressing is done by an X-Y, coincident voltage technique, not unlike that used in digital memory structures. In the basic structure, readout is effected by injecting the charge from individual sites into the substrate and detecting the resultant displacement current. A number of variations of this technique are possible, some of which will be described below. In this paper we describe the basic CID structure, several

site selection and readout techniques, and CID fabrication methods. Performance data for various CID structures are given and discussed.

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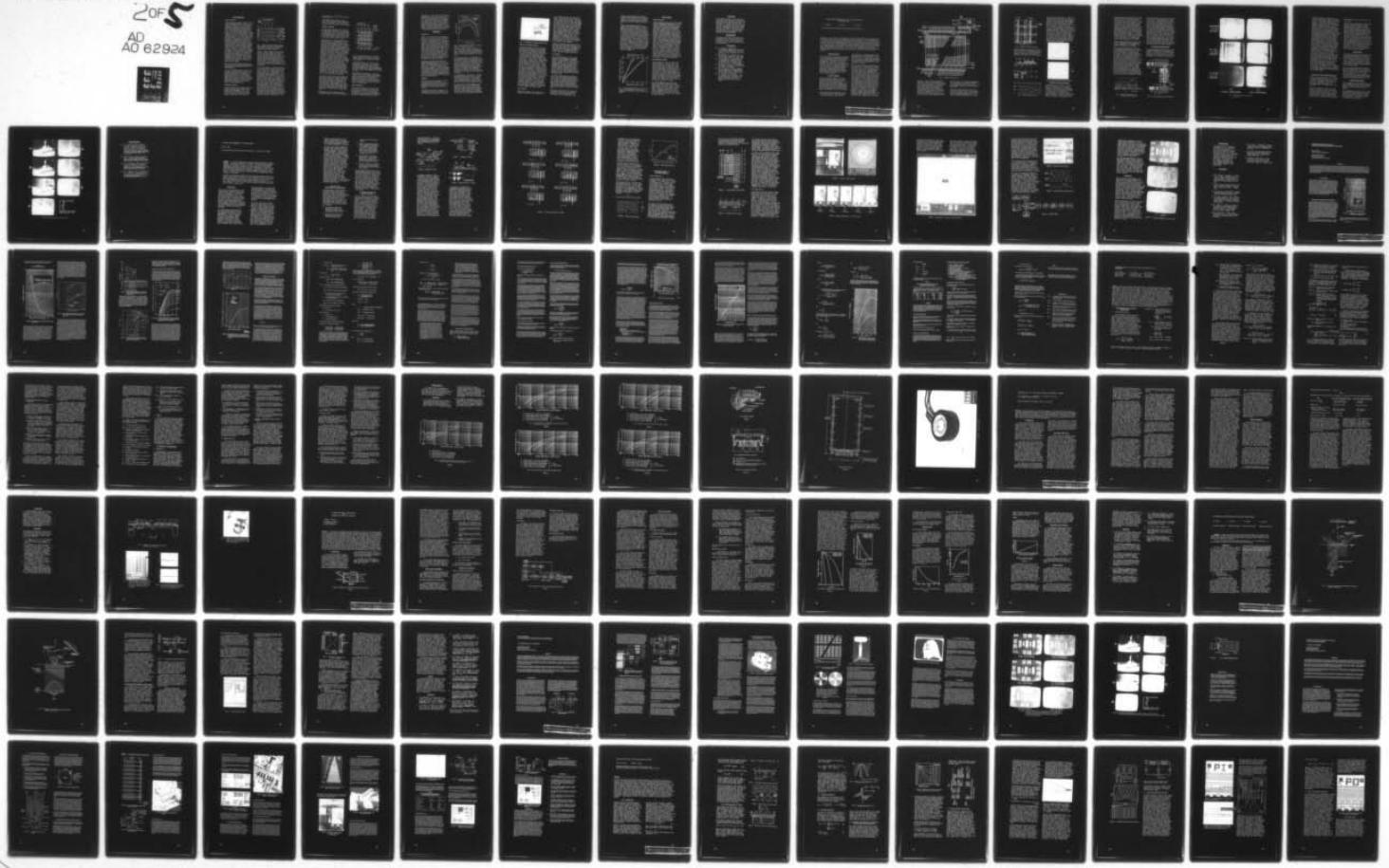
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BASIC DESCRIPTION

CHARGE INJECTION

The CID imaging technique requires that the collected photon-generated charge be ultimately disposed of by injection into the substrate. Upon injection, this charge must either recombine or be collected to avoid interference with subsequent read-outs. For the high-lifetime material usually required for image sensors, recombination is not a suitable method of charge disposition, since re-collection of this charge can give rise to objectionable image lag and crosstalk. For this reason, most CID imagers are fabricated on epitaxial material. The epitaxial junction, which underlies the imaging array, acts as a buried collector for the injected charge. If the thickness of the epitaxial layer is comparable to the spacing between sensing sites, almost all of the injected charge will be collected by the reverse biased epitaxial junction and injection crosstalk is avoided. The time required for charge injected at the surface to be removed from the epitaxial layer has been determined analytically and experimentally to be approximately 100 nsec for the conditions typically used in the CID. The effective thickness of the epitaxial layer can be adjusted during operation by varying the junction bias voltage.

The use of the buried charge collector also modifies the spectral response and MTF characteristics in a manner that will be described below.

For intensified applications, where it is required to thin the silicon substrate for backside illumination by electrons, the epitaxial structure can be replaced by charge collectors on the front surface. These take the form of a grid of diffused conductors separating the rows and columns. CID imagers operated in this fashion exhibit injection characteristics quite similar to epitaxial devices.

SEQUENTIAL INJECTION

An array designed for sequential injection which includes integral scanning shift registers is diagrammed in Fig. 1 (a). Each sensing site consists of two MOS capacitors with their surface inversion regions coupled such that charge can

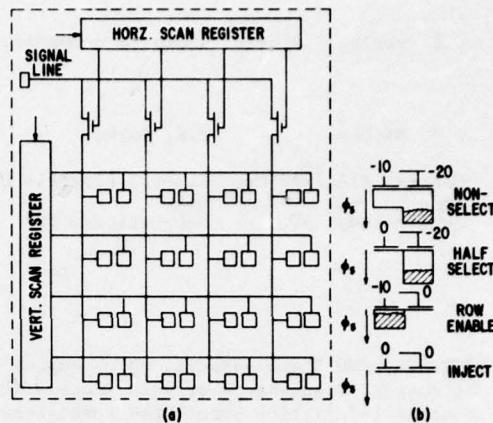


Fig. 1 Basic accessing scheme, (a) schematic diagram of array, (b) sensing site cross-section showing silicon surface potentials and charge locations.

readily transfer between the two storage regions. A large voltage is applied to the row-connected electrodes so that photon-generated charge collected at each site is stored under the row electrode, thereby minimizing the capacitance of the column lines. The sensing site cross-sections, Fig. 1 (b), illustrate the silicon surface potentials and locations of stored charge under various applied voltage conditions.

A line is selected for readout by setting its voltage to zero by means of the vertical scan register. Signal charge at all sites of that line is transferred to the column capacitors, corresponding to the Row Enable condition shown in Fig. 1 (b). The charge is then injected by driving each column voltage to zero, in sequence, by means of the horizontal scan register and the signal line. The basic signal is contained in the majority-carrier displacement current that flows upon injection of the stored charge. This signal can be detected anywhere in the loop composed of the substrate, driver circuit, and the driven array lines. In general, the array lines provide the lowest capacitance environment for signal detection. Charge in the unselected lines remains under the row-connected electrodes during the injection pulse time (column voltage pulse). This

corresponds to the half select condition of Fig. 1 (b).

This readout method has been termed "sequential injection" since, regardless of the scan geometry, the charge at the storage sites is injected in time sequence.

PARALLEL INJECTION

In this readout technique, the functions of signal charge detection and injection are separated. The level of signal charge at each sensing site is detected by intra-cell transfer during a line scan and, during the line retrace interval, all charge in the selected line can be injected.

A diagram of 4 X 4 array designed for parallel injection is illustrated in Fig. 2 with the relative silicon surface potentials and signal charge locations included. As before, the voltage applied to the row electrodes is larger than that applied to the column electrodes to prevent the signal charge stored at unaddressed locations from affecting the column lines. At the beginning of a line scan, all rows have voltage applied and the column lines are reset to a reference voltage, V_s , by means of switches S_1 through S_4 and then disconnected. Voltage is removed from the line selected for readout (X_3 in Fig. 2) causing the signal charge at all sites of that line to transfer to the column electrodes. The voltage on each floating column line changes by an amount equal to the signal charge divided by the column capacitance. The horizontal scanning register is then operated to scan all column voltages and deliver the video signal to the on-chip preamplifier, Q_1 . The input voltage to Q_1 is reset to a reference level prior to each step of the horizontal scan register.

At the end of each line scan all charge in the selected line can be injected simultaneously by driving all column voltages to zero through switches S_1 through S_4 . Alternatively, the injection operation can be omitted and voltage reapplied to the row after readout causing the signal charge to transfer back under the row electrodes. This action retains the signal charge and constitutes a nondestructive readout operation.

The parallel injection approach permits high speed readout and is thus well adapted

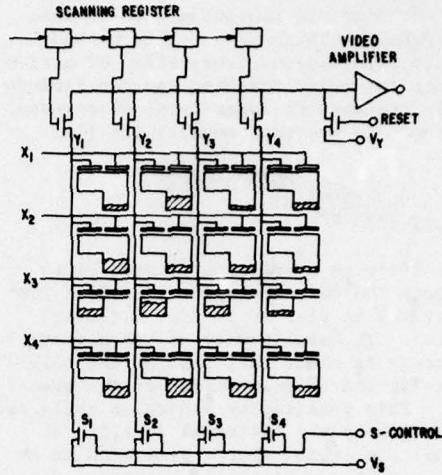


Fig. 2 Schematic diagram of a CID array designed for parallel-injection readout. Surface potentials and charge locations are included.

to TV-scan formats, and offers optional nondestructive readout. A 244 line by 248 element imager, employing this technique and including an on-chip preamplifier, has been designed, fabricated, and evaluated in both the normal and nondestructive readout mode.

For TV-compatible operation, a line time interval of 63 micro seconds (5 MHz element rate) is used and the vertical scan rate is 60 scans per second. The image is completely read out during each interlaced field of the standard TV frame such that video is displayed on all 488 active lines of the 525 line system.

ARRAY FABRICATION

To date, most CID imagers have been fabricated with a p-channel, silicon-gate process modified to provide a top contact to the epitaxial layer. The disadvantages of this method are requirements for a diffused area and an interlevel contact at each

sensing site. This results in some signal degradation as well as an area penalty. Both of these problems have been overcome by a design which employs an overlapping-electrode structure for charge transfer. This technique is now being used to make high-density CID imagers. This method permits simultaneous fabrication of active devices for array scanning and can include highly transparent upper-level electrodes for improved spectral sensitivity (1).

PERFORMANCE

SENSITIVITY

Sensitivity as a function of wavelength for both the bulk and pitaxial 100 X 100 structures is plotted in Fig. 3 (lower curves). The sensitivity of the epitaxial structure is about half that of the bulk imager in the visible region of the spectrum. This sensitivity reduction reflects collection by the epitaxial junction of some of the signal charge generated in the space between sensing sites. Thus, some of the indicated sensitivity loss is not a real loss in that it represents loss of charge that was contributing to cross talk in the bulk sample. The somewhat greater loss in the infrared region is to be expected because of the deeper photon penetration at these wavelengths.

The upper curve shows the sensitivity improvement resulting from the use of a highly transparent material for the upper level in an overlapping electrode configuration. Since this data was taken using a bulk imager, it should be compared to a standard bulk results (middle curve). Of particular significance is the greatly increased blue response which results from the substitution of the transparent material for a large portion of the polysilicon gate-electrode material.

BLOOMING

The CID structure is resistant to image blooming since each sensing site is electrically isolated from its neighbors. Charge spreading in the substrate is minimized by the underlying charge collector.

In sequential injection, blooming of the displayed image occurs if charge is injected from a half-selected site during

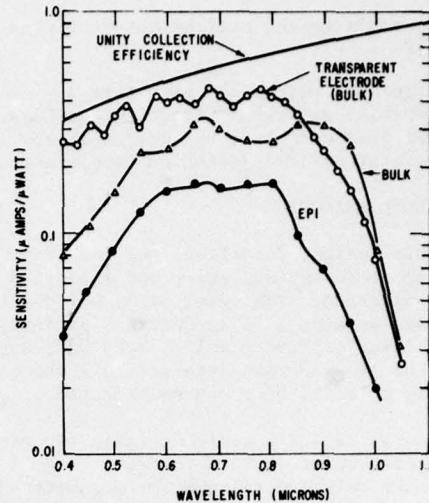


Fig. 3 Sensitivity as a function of wavelength of incident radiation.

readout of another site on the same column. This excess injected charge is detected as signal and adds to the displayed video. This results in brightening of the affected column upon overload of a single site.

The image displayed in the parallel injection approach exhibits relatively little blooming as a result of sensing site overload. This is because the half-select and injection operations occur during the horizontal blanking interval. While excess charge can accumulate during a line scan interval and cause column brightening for overloads occurring in the right-hand portion of the image field, this effect is attenuated by the line-to-frame integration time ratio.

For NDRO operation, virtually no blooming occurs, since the charge is not injected. The affected sites fill to capacity and cease collecting charge. In all cases, radial spreading of excess charge is prevented by the underlying charge collector.

The image shown in the photograph, Fig. 4 was produced by a 244 X 188 CID imager exposed to a high contrast scene. This particular camera uses a modified parallel injection readout method that is highly resistant to image blooming, as indicated by the image of the automobile head lamps.

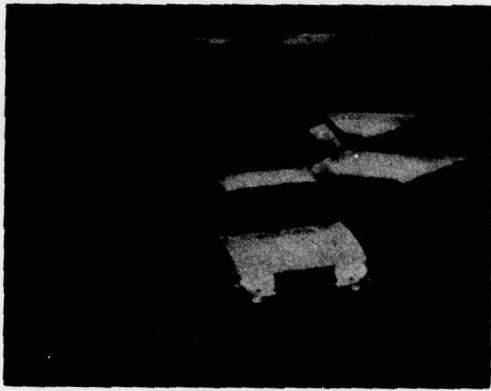


Fig. 4 CID image of high-contrast scene.

MODULATION TRANSFER FUNCTION

Since each sensing site is electrically isolated from adjacent sites, the MTF of CID imagers is intrinsically quite high. This electrical isolation is maintained for both the charge collection and readout operations; the epitaxial charge collector inhibits charge migration in the substrate, and there is no MTF loss effects due to site-to-site transfer during readout. Imagers made on high-lifetime bulk material do exhibit loss of MTF to a degree dependent on the carrier lifetime of the particular material used. Image lag would occur in a like fashion. Since the use of an epitaxial collector reduces the measured sensitivity, particularly for the longer wavelengths, a trade-off situation exists in the design of the structure. By adjusting the epitaxial thickness with relation to the site separation, these two performance characteristics can be tailored to a particular application. The sensitivity loss of the epitaxial structure in the 100 X 100 imager, as shown in Fig. 3, illustrates this effect. In this case, epitaxial thickness is small compared to the site separation, resulting in about a two-to-one loss in measured sensitivity. This same imager exhibits an in-phase MTF of nearly 100% at the Nyquist limit.

NOISE SOURCES

The primary temporal noise sources in CID imagers are amplifier noise, capacitor-

reset (KTC) noise, and bias charge shot noise. Unlike the CCD, the CID has negligible charge transfer noise. The capacitive load seen by the signal charge can be reduced by the use of an on-chip MOSFET as the first stage of the video amplifier. This device should have high transconductance for reduced Johnson noise (2) and a large channel area for reduced 1/f noise (3). In most applications 1/f noise is not a serious problem since correlated double sampling can be used to attenuate noise components that are lower in frequency than the sampling rate. This technique also eliminates KTC noise in many cases. In the parallel injection readout method, the column reset switches introduce KTC noise that is not rejected by correlated double sampling.

Theoretical amplifier noise levels are on the order of a few hundred carriers in the CID, while KTC noise can be negligible or the predominant noise source, depending on the specific array design and readout method. Noise in the bias charge can be of the same order as amplifier noise.

DARK CURRENT

A critical performance factor in image sensors is the magnitude of thermally generated charge, commonly called dark current. In addition to reducing charge storage capacity, dark current limits integration time, and can contribute to undesirable background patterns in the displayed image. Random fluctuations in the dark current contribute to system noise. While cooling the sensor can reduce dark current, the additional system complexity is not desirable for most system applications.

In the CID, significantly more silicon area can be used for photon charge generation than for charge storage and readout. Since the charge generation rate in non-depleted bulk silicon is orders of magnitude less than in depleted silicon (4) the CID collects photon-generated charge from virtually the entire site area while generating dark only in the storage area.

CID arrays are operated with a bias voltage somewhat higher than the threshold voltage to allow the accumulation of a bias charge in the storage area. This

inhibits charge pumping losses during readout and also results in an additional reduction in dark current, since surface leakage is much smaller under inversion conditions than under depleted conditions (5).

Thermal charge generation rates in a typical 100 X 100 CID imager for various operating conditions are shown in Fig. 5. Minimum dark current results from biasing the storage electrodes such that charge is stored under both electrodes, Fig. 5(a). If one of the storage regions is operated in depletion, the increased surface leakage in this region results in a higher dark current, as shown in Fig. 5(b). The effect of temperature on charge generation rate is also shown in Fig. 5. A reduction in temperature of twenty degrees Celsius results in a tenfold decrease in the rate of charge accumulation. This relationship has been found to hold over a wide range of temperatures and amounts to a two-to-one change in charge buildup for each six-degree change in temperature.

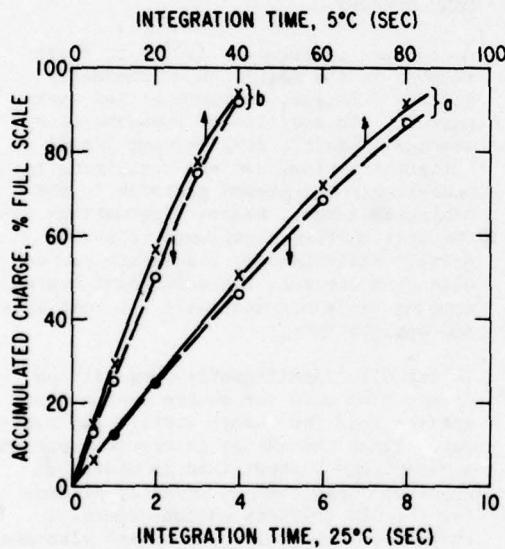


Fig. 5 Thermal charge buildup as a function of time and temperature, with a) both storage regions inverted, and b) one region depleted.

OTHER FEATURES

RANDOM SELECTION

Certain imaging applications, such as those involving bandwidth compression, could be much more effectively implemented if the primary image information could be made available in other than the progressive scan format employed by most currently available imaging devices. The X-Y, co-incident voltage configuration of the CID makes it easily adaptable to special scan formats, including "random" addressing, in which each sensing site can be addressed without regard to its time or spatial sequence with respect to other sites in the array. In many respects, image site selection in the CID resembles MOS memory selection, and many of the decoding techniques developed for these memories could be applied to random access imagers. Charge could be injected during readout in the manner of sequential injection or deferred to a later time as is done in parallel injection. Charge integration time could be held constant for all sites in the array by having the site selection pattern repeat frame-to-frame, or, conversely, the integration time for particular sites could be tailored to local scene brightness.

NONDESTRUCTIVE READOUT

The nondestructive charge readout technique of Tiemann, et al (6), can be effectively applied to CID imagers. This fact, combined with low dark current performance, make image storage in the CID array a practicality. To demonstrate this, a cooled 244 X 248 CID imager has been operated in a nondestructive readout mode for three hours at 30 frames/second with no apparent degradation of the stored image other than a slight increase in background charge. The charge loss during this experiment was estimated to be much less than one carrier per pixel per frame.

In a second experiment, a series of exposures was made at successively lower light levels while operating at 30 frames/second, NDRO. The time to reach a given level of signal was recorded for each exposure. Exposure time was found to be inversely proportional to light intensity with no measurable reciprocity loss down to light levels in the order of two carriers per pixel per frame.

CONCLUSIONS

The CID approach leads to many desirable performance characteristics, including high sensitivity over a wide spectral range, low dark current, high MTF, and resistance to blooming -- in a structure that is tolerant to defects and permits many design options such as nondestructive readout and random scanning. On balance, these features more than compensate for its relatively high thermal noise level as compared to that reported for other approaches.

ACKNOWLEDGMENT

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A HIGH PERFORMANCE 190 x 244 CCD AREA IMAGE
SENSOR ARRAY

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ABSTRACT: The first of a new generation of buried channel CCD area image sensors based on a gapless silicon-gate technology has been developed. The first product to be completed is a 190 x 244 element device which is the successor to a similar device previously developed in undoped polycrystalline silicon isolation technology. In addition to the area array, which uses the interline transfer system, the device includes a floating gate output amplifier, a distributed floating gate output amplifier, two electrical inputs and a column antiblooming structure. The device has been operated at data rates greater than three times the design center of 7 MHz. At low light levels images of half Nyquist frequency bar patterns have been observed at signal levels of less than 30 electrons.

INTRODUCTION

A new generation of processing technology has been applied to an improved design of a 190 x 244 element Charge Coupled Area Imaging Device (CCAID). This device, the AID244 is a member of a family of CCAID's which have been developed during the past two years, using the interline transfer system and undoped polycrystalline gate isolation technology. In this paper the design aspects, processing technology, antiblooming characteristics and low light level performance of the device will be discussed.

DEVICE DESIGN

The front side illuminated area array using the interline transfer system⁽¹⁾ has been retained in the design of the new device family. One hundred ninety columns of 244 elements alternating with optically insensitive vertical shift registers, form the array of the AID244 device. Two other members of the new family of gapless technology devices are currently

in development. A gapless version will supersede the Fairchild CCD201, a 100 x 100 element device, introduced almost two years ago. A larger device designed with 380 columns of 488 elements is being developed for full frame NTSC TV compatible performance.

The overall organization of the AID244 is shown in Fig. 1. The optically sensitive area of the array, detailed in Fig. 2 has an aspect ratio of 4:3. A diagonal of 7.2 mm makes the device compatible with lenses designed for the super 8 mm format. The photoelement cell size is 14 μm x 18 μm with 4 μm of vertical overlap in the channel stop and 16 μm of horizontal separation due to the interleaved vertical shift registers. These dimensions are compatible with the resolution and alignment capabilities of the fabrication process developed for this family of devices. The output signal format provides two interlaced fields of line sequential information in conventional left to right, top to bottom TV sequence. Two output amplifiers are provided in the AID244 design. A single stage floating gate amplifier (SFGA) provides an output level of 300 mV into a 510 Ω load for near saturation level signals at the 7.16 MHz

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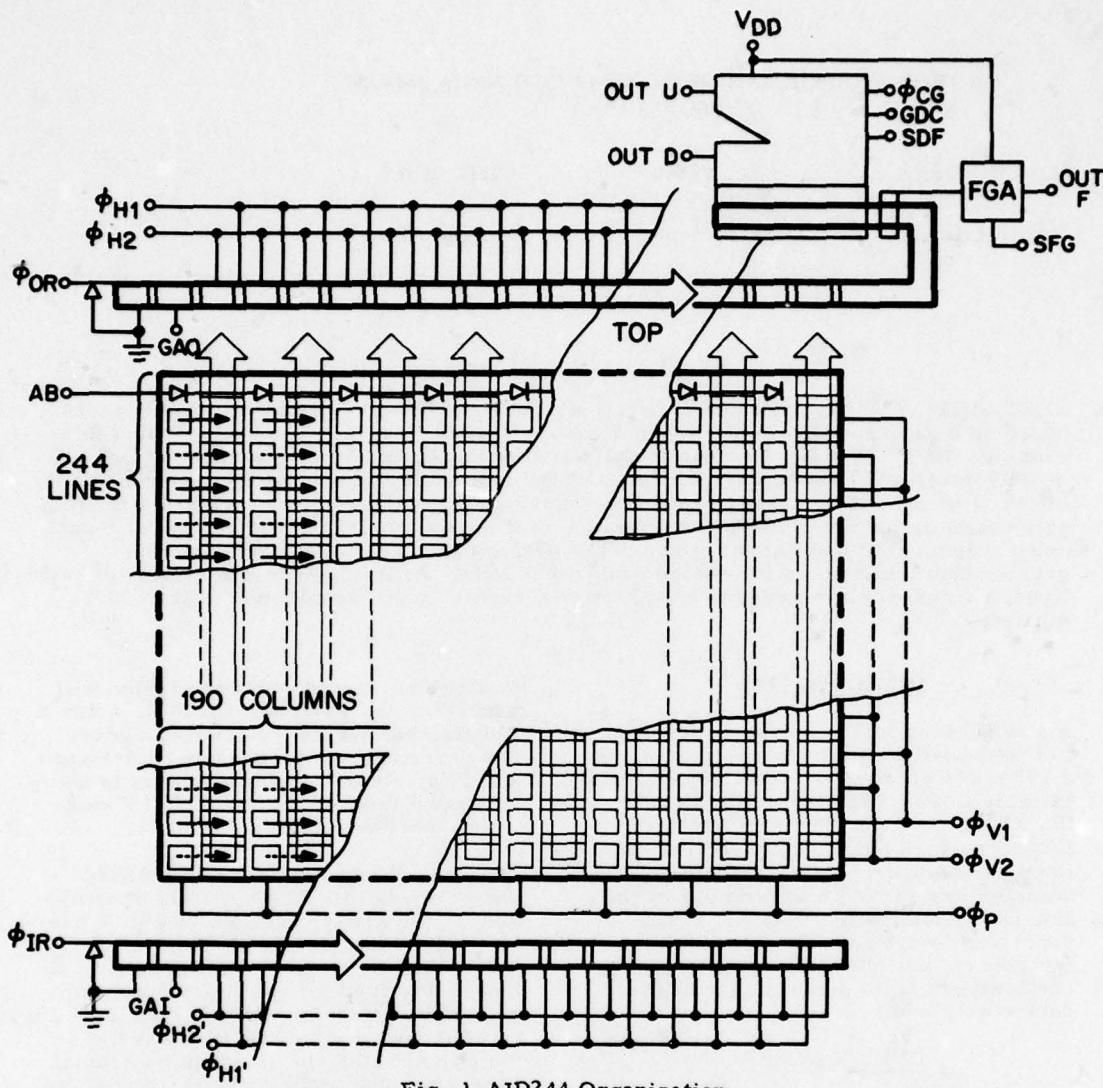


Fig. 1 AID244 Organization

data rate. The floating gate amplifier design was chosen for the AID244 because it provides a video signal free from reset noise and operates with a random noise level of less than 10^4 electrons.⁽²⁾ A twelve state distributed floating gate amplifier (DFGA) is provided for very low light level applications. The DFGA features two outputs, one of which is delayed from the other by half a horizontal clock period. By summing these out-

puts off chip, clock voltage components in the video output are cancelled. Details of the amplifier design are discussed in another paper presented at this conference by D. Wen.

Two linear electrical input circuits are used in the AID244 design, one associated with the input shift register and the other with the horizontal shift register. The latter is intended primarily as a test tool

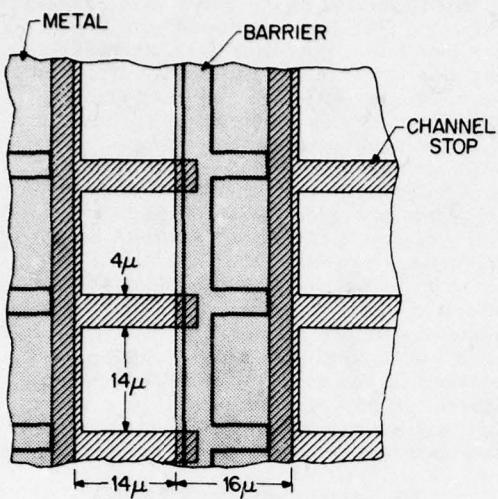


Fig. 2 AID244 Area Array Detail

for calibrating the DFGA signal level, while the former is intended for application of the device as an SPS analog shift register. Both input transducers are identical in design, and are represented

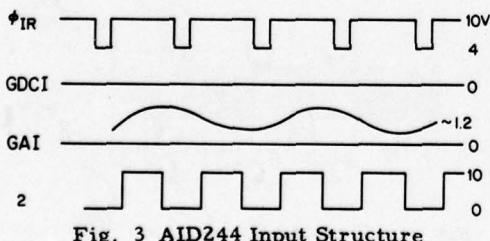
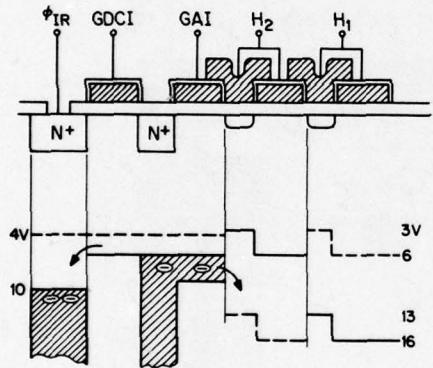
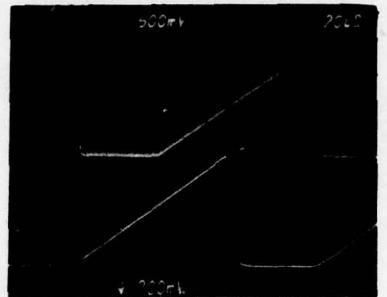
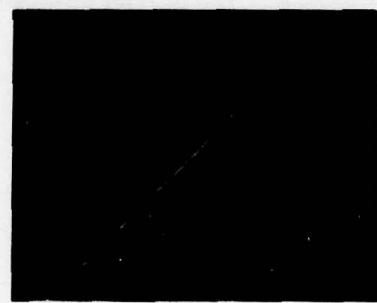


Fig. 3 AID244 Input Structure

by the cross section in Fig. 3. This is similar to the input system referred to by Tompsett⁽³⁾ as the charge equilibration method, in which the input source (Φ_{IR}) is pulsed to a low voltage to inject charge across a barrier formed under GDC1, the DC control gate. Then the source is reversed biased and drains back the excess charge. The input signal is impressed on the analog input gate (GAI) and controls or modulates the flow of charge to the channel. Fig. 4A shows input and output ramp excitation waveforms. The full signal range linearity from the input register to the output is shown in Fig. 4B. Approximately 1500 mV of input signal swing is required to achieve the maximum linear output signal. The nonlinearity for 90% saturation is less than 3%.



A



B

Fig. 4 Electrical Input Characteristics

FABRICATION TECHNOLOGY

The performance of CCAID's, particularly at low light levels, is strongly influenced by the fabrication technology employed. Buried n-channel technology is used for all Fairchild CCAID's, i.e., an n-type layer is ion implanted in a p-type substrate. P+ doped channel stops define the photosite regions and the CCD register channels. The photoelectron

charge packets are moved within the bulk silicon, away from the silicon-silicon dioxide interface. Since they do not contact surface states at the interface, a flat zero charge, which is needed in surface-channel devices to obtain high transfer efficiency, is not required in this technology. Furthermore, the location of the channel in the bulk of the silicon subjects the photoelectrons to a stronger horizontal component of the clock electrode field than it has near the surface. This fringe field aids carrier transport and results in improved transfer efficiency, particularly at high frequencies. The transfer efficiency of the AID244 at a 20 MHz data rate has been measured to be 0.9998.

Undoped polycrystalline silicon gate isolation technology previously applied to similar CCAID's has been replaced by gapless technology in the AID244.

Two principal advantages are attained with the gapless polysilicon gate isolation technology of Fig. 5, which uses two levels of polysilicon to form the gate electrodes. The first level of polysilicon is deposited on the gate dielectric over the substrate which already contains the N-channel but no implanted barriers. This layer is patterned to form the V_1 and V_2 electrodes over the non-barrier sections of the channel. The barrier implant, following next in the fabrication cycle, is masked by these electrodes, providing truly self aligned barriers for 2 phase shift register operation.⁽⁴⁾ A second layer of polysilicon is subsequently used to form the electrodes over barrier sections of the channel. This self alignment of the barrier to the gate electrodes eliminates potential well irregularities caused

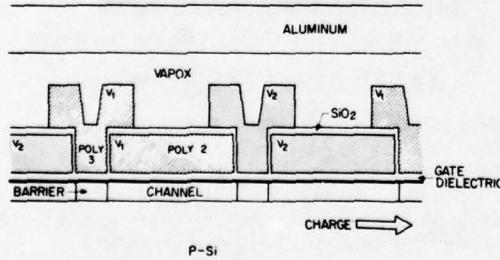


Fig. 5 Gapless Polysilicon Gate Isolation Cross Section

by misalignment of the gates with respect to the barrier in the undoped gate isolation process. Potential well irregularities due to the misalignment have caused poor transfer efficiency at low signal levels and at high operating frequency in devices manufactured with undoped polysilicon isolation technology. In the gapless polysilicon isolation technology silicon oxide provides the electrical isolation between gate electrodes, whereas undoped polysilicon provided this function in the older technology. The insulating characteristics of silicon oxide are superior to those of undoped polysilicon, particularly after subsequent high temperature processing cycles required to fabricate the device. Reductions in gate to gate shorts and leakage have been observed on devices manufactured with the new technology.

BLOOMING SUPPRESSION

A column antiblooming technique has been successfully applied in the design of the AID244. The function of the antiblooming structure is to prevent excess carriers generated by overexposure of one or more photosites in a column from spreading to

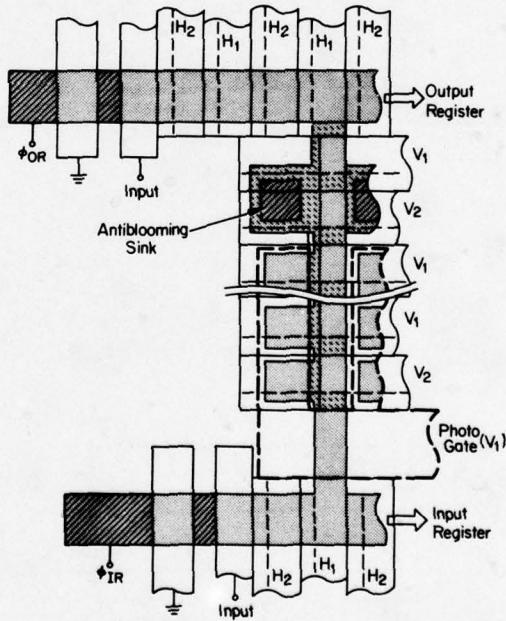
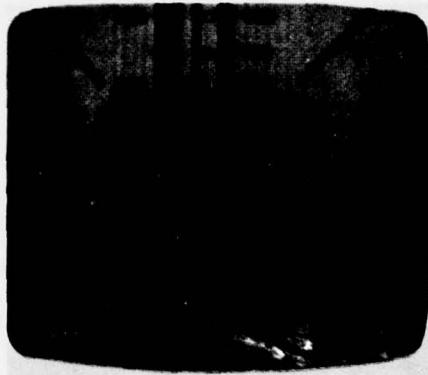
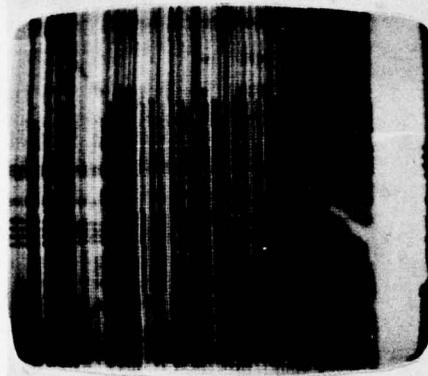


Fig. 6 Blooming Suppression Structure

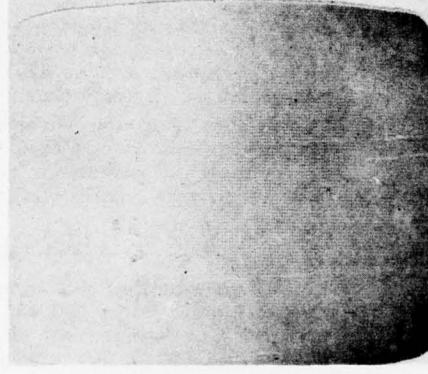
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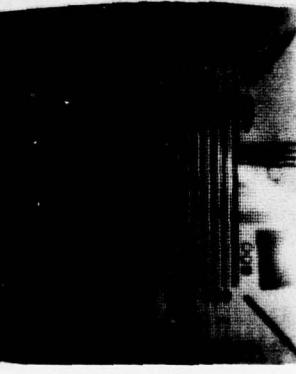
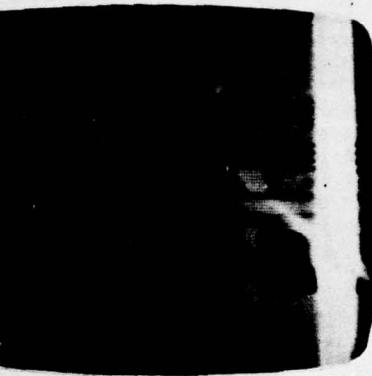
$10^3 \times$ SAT.
→
EXPOSURE



$1.6 \cdot 10^4 \times$ SAT.
→
EXPOSURE



↑
WITHOUT ANTIBLOOMING



↑
WITH ANTIBLOOMING

Fig. 7 Blooming Suppression Characteristics

adjacent columns. A sink for excess carriers is provided at the top and bottom of each vertical shift register, as shown in Fig. 6. At the top, above the last photosite, between the horizontal output register and the area array, a line of N+ regions is diffused into the structure. These N+ carrier sinks are electrically separated from the vertical shift register by a barrier. The N+ regions are connected together by metallization and connected to the antiblooming terminal. When an appropriate positive bias is applied to the antiblooming terminal, any carriers exceeding the barrier potential will be removed before they can reach the horizontal output register, where lateral spreading would occur. At the bottom of each column the horizontal input register, appropriately biased, provides a similar sink. In Fig. 7 the device performance with and without blooming suppression is compared. The intensity of a light spot approximately six elements wide was varied from near saturation to 10^3 times saturation and 1.6×10^4 saturation. At 10^3 times saturation severe image degradation occurred over the entire picture area without blooming suppression; with antiblooming bias applied, the image degradation was limited to about 10% of the picture area. At 1.6×10^4 times saturation exposure the device was completely flooded without antiblooming, while 75% of the image remained unaffected with antiblooming. Some evidence of lens flare is evident in Fig. 7, causing the diagonal white streaks emanating from the fiberoptic light source used to generate the overload image.

LOW LIGHT LEVEL PERFORMANCE

Low light level performance of the AID244 has been demonstrated under a variety of conditions. Application of the device to low light level cameras and results obtained are reported in a paper by K. Hoagland and H. Balapole at this conference.

In all cases custom designed electronic systems consisting of drive electronics and video processors were used. Details of these systems are beyond the scope of this paper but it must be emphasized that careful attention to both systematic and random noise is essential to avoid shading

and noise patterns and to minimize random noise.

In all tests, the calibration technique was based on the measurement of output register current for images near the saturation charge level of 3×10^5 electrons per pixel. Single neutral density filters and lens diaphragm settings were used to reduce the image intensity. Room temperature and cooled measurements have been made using the DFGA output.

Images of half Nyquist frequency bar patterns were observed with highlight charge packets of 25 electrons at 0°C . Fig. 8 shows images obtained at -10°C for signal levels ranging from near saturation to 25 electron highlight charge packets. Equivalent images at room temperature required about twice as much signal charge as required at -15°C . The signal level in the 25 electron image of Fig. 8G is less than the noise equivalent signal.

CONCLUSION

The application of gapless polysilicon gate isolation technology to a 244×190 element CCAID has improved the low light level performance characteristics of the device, to provide useful images with charge packets of 25 electrons. Fabrication yields obtained with this technology are now making commercial introduction of the device possible.

A new distributed floating gate amplifier provides suppression of clock signals to the video output further enhancing the low-light level performance of the device.

New design features, such as a linear electrical input and column antiblooming are expected to extend the range of applications for this family of devices.

ACKNOWLEDGEMENT

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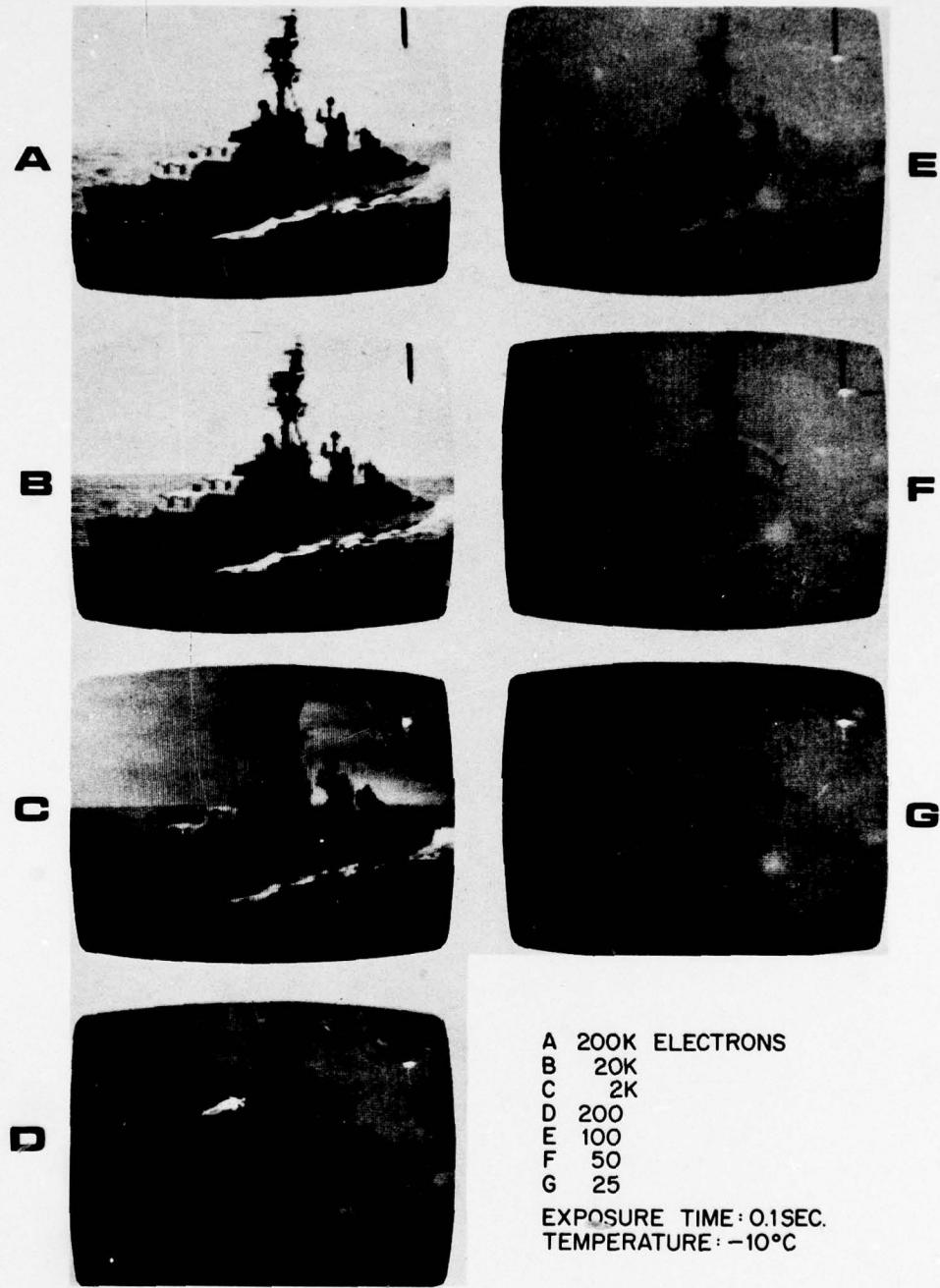


Fig. 8 Low Light Level Performance

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LOW LIGHT LEVEL PERFORMANCE OF CCD IMAGE SENSORS

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ABSTRACT This paper reports the low light level performance of CCD image sensors. Theoretical limitations of transfer efficiency for small charge packets in CCD shift registers are reviewed. Low noise charge detection techniques are discussed. Specifically, the operation of a distributed floating-gate amplifier (DFGA) is described. A DFGA employs several charge amplifiers which repeatedly sense a signal charge packet in a CCD. The outputs of the charge amplifiers are coherently summed in a second CCD shift register. Signal-to-noise ratio is improved so that extremely small charge packets can be detected.

Low light level imaging performance of both linear and area arrays are reported. The linear array contains 1728 photoelements and uses a single-stage floating-gate amplifier (FGA) as the on-chip detector. The area array has 244 x 190 photoelements and contains a twelve-stage DFGA and an FGA. Both arrays employ two-phase, buried channel CCD shift registers. Low light level images at 50 and 25 electron levels have been achieved with the linear and area sensors, respectively.

INTRODUCTION

The low light level performance of CCD image sensors is reported in this paper. The basic requirement of transferring a small charge packet in a CCD shift register is considered first. It is well known⁽¹⁾ that in a surface channel CCD shift register, a background charge (fat zero) is required at all times to suppress charge-trapping effects of surface states. The noise⁽²⁾ associated with the generation of the fat zero makes the surface channel CCD sensor inadequate to perform low light level imaging functions.

In a buried-channel CCD register⁽³⁾, the signal charge packets are stored and transferred in the bulk of the semiconductor so that surface state trapping can be avoided. However, the signal charge packets may be trapped by the crystalline imperfections in the bulk of the semiconductor. The effect of these bulk traps on charge transfer efficiency plays a dominant role in the low light

level performance of buried-channel CCD image sensors. This effect has been analyzed and reported previously by J. Early.⁽⁴⁾ Some of his principal assumptions and conclusions are repeated in the first part of this paper. It is shown that signal charge packets of approximately 10 electrons can be transferred in a buried-channel CCD register.

In order to fully exploit the low light level capability of buried-channel CCD image sensors, a special low-noise, high-gain amplifier must be used. Such an amplifier is the distributed floating-gate amplifier (DFGA)⁽⁵⁾. A DFGA employs several charge amplifiers with floating gate inputs to sense repeatedly a signal charge packet in a CCD register. The outputs of the charge amplifiers are summed using a second CCD register. Since the random noise of the charge amplifiers is uncorrelated, the resulting signal-to-noise voltage ratio is enhanced by a factor equal to the square root of the

number of charge amplifiers used. Signal charge packets of the order of 10 electrons can thus be detected. Operation and experimental results of a twelve-stage DFGA are discussed.

Low light level imaging performance of both linear and area arrays are reported. The linear array contains 1728 photoelements. Charge packets in the photosites are transferred in parallel into an adjacent opaque, two-phase, buried-channel, implanted-barrier CCD shift register. A single-stage floating-gate amplifier is positioned at the end of the register to detect the signal charge packets. The area array has 244 x 190 photo-elements and employs the interline transfer organization. Signal charge packets from each column are transferred into an adjacent opaque two-phase vertical shift register. The vertical shift register in turn transfers each row of signal charge packets into a two-phase horizontal shift register. The signal charge packets are then transferred along the horizontal register and detected by a twelve-stage DFGA and an FGA. Image resolution and noise performance are examined at different light levels.

LOW LIGHT LEVEL CHARGE TRANSFER CONSIDERATIONS

In buried-channel CCD image sensors, the signal charge packets may be trapped by crystalline imperfections in the bulk of the semiconductor. The effect of bulk traps and dark current on charge transfer efficiency and signal-to-noise ratio for a hypothetical 500 x 500 element CCD area image sensor, operating in the standard NTSC mode has been analyzed by J. Early. His analysis revealed the following:

- 1) A reduction in operating temperature reduces dark charge and thereby increases the signal-to-noise ratio.
- 2) An increase in dark current improves charge transfer efficiency because bulk

traps can be filled by dark charges.

- 3) Under worst-case conditions, for an average dark charge of 10 electrons per pixel and a signal of 10 electrons per pixel, the overall transfer efficiency is approximately 0.8, and the signal-to-noise voltage ratio is 1.4.
- 4) Bulk trapping is of consequence only in long registers operating at conventional television horizontal line repetition rates of 15.75 KHz.
- 5) Transfer efficiency and signal-to-noise ratio are excellent at the high horizontal transfer rate of 5MHz.

Charge transfer efficiency of a 15-electron charge packet in a two-phase buried-channel CCD was measured, using statistical methods.⁽⁶⁾ The device was cooled to obtain an average dark charge of 4 electrons per pixel. It was observed that after 238 transfers at a 15.7 KHz clock rate, approximately one electron was lost. This data confirms the theoretical analysis that in a buried-channel CCD shift register there is useful transfer efficiency after 500 transfers in a signal charge packet of approximately 10 electrons.

DISTRIBUTED FLOATING-GATE AMPLIFIER (DFGA)

In a CCD register, the signal charge packet can be detected by a sensing "floating-gate" electrode as shown in Figure 1. It can be seen that the floating gate provides a capacitive coupling between the signal charge packet in the CCD register and the current in the MOS channel without making physical contact with either of them. Since the signal charge packet is not destroyed by the floating gate, it can be transferred along the CCD register and be detected repeatedly by similar structures. In a DFGA⁽⁵⁾, the outputs of several floating-gate structures are summed with a

second CCD register. The signal-to-noise ratio of the summed output is enhanced so that extremely small charge packets can be detected.

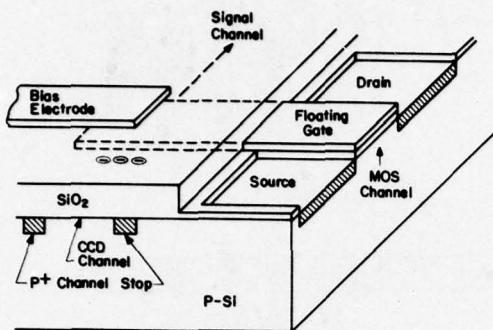


FIGURE 1 Schematic of FGA.

A schematic diagram of a twelve-stage DFGA is shown in Figure 2. It consists of an input register, a bank of twelve charge amplifiers with floating-gate inputs, an output CCD register, and an output amplifier. A signal charge packet is sensed by the floating gates when it is transferred in the input register. The operation of the charge amplifier is illustrated in Figure 3. During the period when the signal charge packet in the input register is under the floating gate, the control gate is pulsed "on" so that a small amount of charge flows into the output register. The magnitude of this charge is determined by the signal charge in the input register through the coupling of the floating gate. This is a charge inverting amplifier in the sense that the larger the signal charge in the input register, the lower the floating gate potential, and the less the charge that flows into the output register. A dc gate is used to eliminate clock coupling from the control gate to the floating gate.

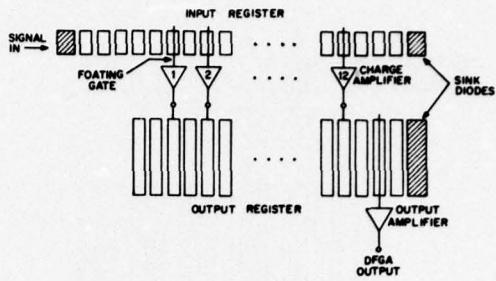


FIGURE 2 Schematic of DFGA.

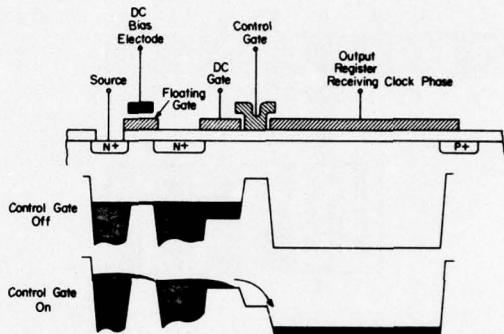


FIGURE 3 Charge amplifier in DFGA.

The operation of a DFGA can be illustrated by considering a hypothetical three-stage structure. Figure 4(a) illustrates the initial charge distribution in the DFGA after a long series of empty charge packets have been transferred along the input register. Figure 4(b) shows that one clock cycle later ($t = t_c$) a large charge packet D has been transferred under the floating gate of the first charge amplifier stage. After the control gate has been pulsed "on" a small amount of charge D is injected into the output register. Figure 4(c) shows that at $t = 2t_c$, charge packet D has been transferred under the floating gate of the second charge amplifier stage while charge packet D' in the output register has also been

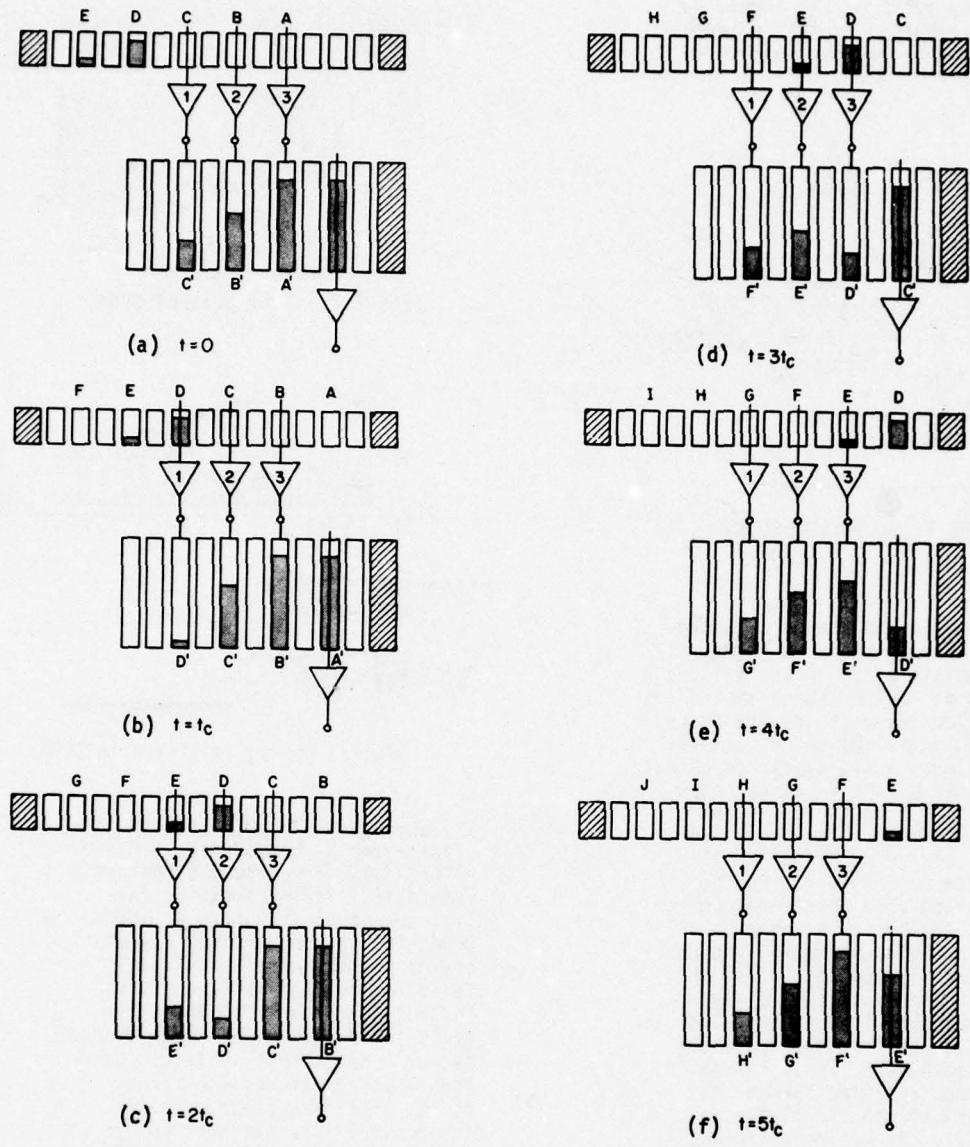


FIGURE 4 Charge distribution in DFGA.

transferred to the corresponding position. After the control gate is pulsed "on", another small amount of charge is added to the charge packet D'. Figure 4(d) illustrates the charge distribution at $t = 3t_c$. At $t = 4t_c$, the charge packet D' has been transferred to the output amplifier where it produces the final DFGA output. Charge packets E and E' in the same sequence illustrate the situation when a small charge packet is transferred along the input register. At $t = 5t_c$, charge packet E' is detected by the output amplifier.

The DFGA output waveform is illustrated in Figure 5. The DFGA output at $t = 4t_c$ corresponds to the initial charge packet D. For zero initial charge in the input register, a maximum amount of charge is injected into the output register. The corresponding output is V_{BIAS} . The signal output for charge packet D which is the difference between the DFGA output and V_{BIAS} , is designated by V_s . The DFGA output at $t = 5t_c$ corresponds to the small charge packet E in the input register.

Twelve-stage DFGA test structures have been built and tested. A typical transfer characteristic curve for a 50nsec control gate "on" time, t_{on} , at 3 MHz bandwidth and room temperature is plotted in Figure 6. The smallest signal level measured is approximately 30 electrons. The RMS Noise measured is 10 to 20 electrons.

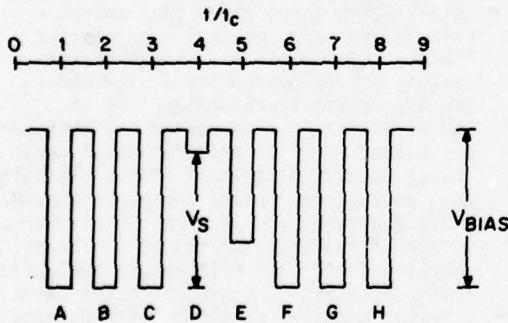


FIGURE 5 DFGA output waveform.

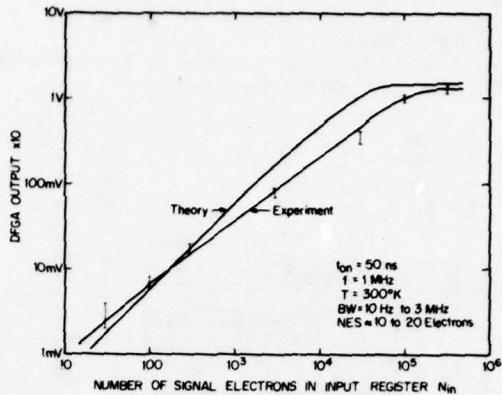


FIGURE 6 DFGA characteristics.

EXPERIMENTAL RESULTS OF CCD IMAGE SENSORS

Linear Image Sensor

A block diagram of the 1728-element interlaced linear image sensor is shown in Figure 7. It consists of an array of 1728 photosites, a two-phase CCD shift register, and a single-stage floating-gate amplifier. An opaque aluminum layer is deposited over the device to block incident light except in the photogate Φ_p area. A positive dc voltage is applied to the photogate to collect the signal electrons in the potential wells formed. The 1728 photosites under the photogate are defined by the p-type channel-isolation diffusion shown in this figure. The center-to-center spacing of these photosites is 13 μ m.

At the end of an integration period, the transfer gate Φ_x is pulsed "high" to transfer the signal electrons in two fields into the neighboring two phase CCD shift register. The signal electrons are then transferred along the shift register and detected by the single-stage floating-gate amplifier. A sink diode and exposure control gate Φ_E are incorporated to provide exposure control and antiblooming functions(7). The CCD

shift register is constructed using two layers of polysilicon with self-aligned ion-implanted barriers(8) as shown in Figure 8. The buried channel is accomplished with the ion-implanted N-layer.

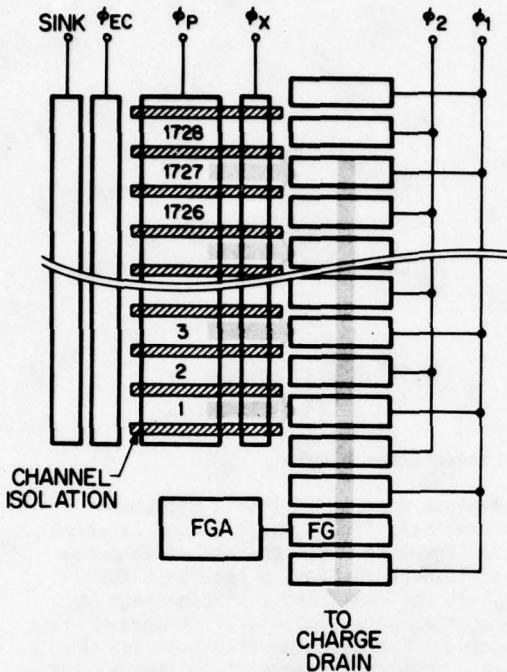


FIGURE 7 A 1728-element linear sensor.

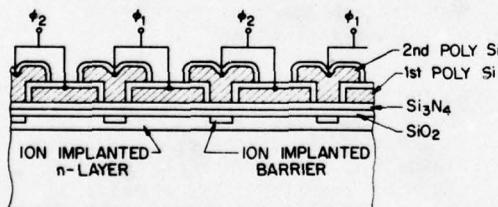


FIGURE 8 Two phase CCD structure.

A CRT monitor display of the IEEE Facsimile Test Chart is shown in Figure 9. The image was horizontally scanned by the image sensor, while vertical scanning was obtained by mechanical rotation of the test chart. A portion of this displayed image is also shown with an expanded monitor sweep. The maximum resolution obtained is approximately 36 line parts/mm.

Low light level performance of this image sensor is illustrated by the photographs in Figure 10. This series of single-frame photographs show the display of approximately 700 photosites at illumination levels successively reduced from near saturation. The ambient temperature was 25°C and the clock rate was 1.5MHz. The high-light area in Figure 10(a) represents an illumination of $200\mu\text{W}/\text{cm}^2$ with a maximum charge per photosite of approximately 500,000 electrons. At a 1/1000 reduction in light intensity, a high-quality image is retained although some dark current spikes appear as vertical streaks. At a 1/10000 reduction in light intensity, the brightest area in the picture represents approximately 50 electrons per photosite. The dark charge per pixel is approximately 800 electrons, resulting in a dark charge noise of 28 electrons. The noise-equivalent-signal per pixel in Figure 10(e) is approximately 100 electrons. The low light level performance of this sensor is therefore limited by the noise in the amplifier.

Area Image Sensor

A photograph of the 244×190 area image sensor (9) is shown in Figure 11. This device employs the interline transfer organization where the signal charge packets are read out in two successive fields. In operation, signal charge packets are generated and stored under the 190 vertical photogates. At the end of an integration period the photogates are pulsed "low" to transfer the signal charge packets from half of the photosites into an adjacent opaque two-phase vertical shift register. The vertical shift register in turn transfers each row of the signal charge packets into a two-phase horizontal shift register. The signal charge packets are then transferred along the horizontal register and detected by the output amplifiers. After all the signal charge



FIGURE 9 Image of linear sensor.

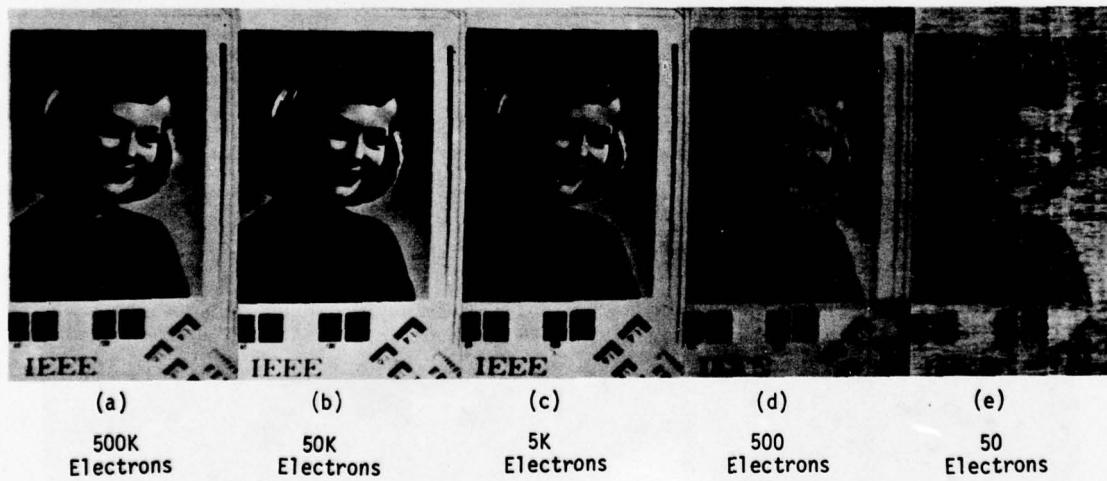


FIGURE 10 Imaging performance of linear sensor.

packets have been detected, the process is repeated to read out the signal charge packets from the remaining photosites. Both the vertical and horizontal shift registers are two-phase, buried-channel structures identical to that shown in Figure 8. The photoelement center-to-center spacing is 30 μ m horizontally and 18 μ m vertically.

This device employs a twelve-stage DFGA, and a single-stage floating-gate amplifier similar to that used in the linear image sensor described earlier. A photograph of the DFGA area is shown in Figure 12. This DFGA is identical to the twelve-stage DFGA test structure described in Section III, except that the structure of the output register has been modified.

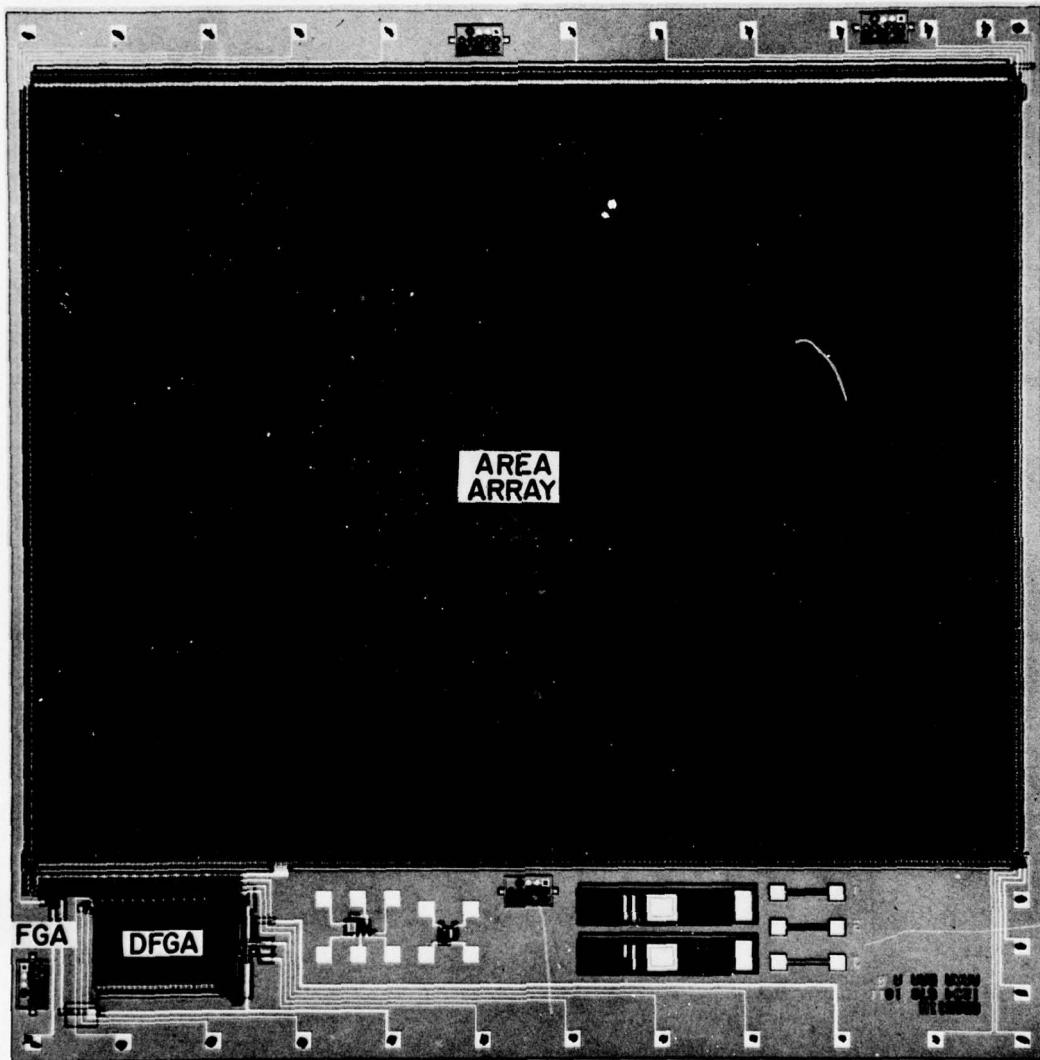


FIGURE 11 Photograph of the 244 x 190 area sensor.

It can be seen that the output register separates into two parallel registers after the twelfth charge amplifier stage. An output amplifier is provided at the end of each register, one being delayed from the other by one half horizontal clock period. By summing these two outputs off chip, the large output swing V_{BIAS} can be cancelled, as illustrated in Figure 13 and the resulting waveform can be much more easily processed. A theoretical analysis indicates that the noise equivalent signal of this DFGA is approximately 17 electrons at room temperature and 3 MHz bandwidth.

A block diagram of the imaging test set-up is shown in Figure 14. The regular and delayed DFGA outputs are combined to remove V_{BIAS} in the output waveform. The output is amplified and then dc restored during each horizontal blanking period with the line clamp circuit. It is amplified again and displayed on a monitor.

Low light level imaging performance of this sensor is illustrated in Figure 15. These photographs show DFGA images at -10°C. The horizontal clock frequency was 2MHz, resulting in a frame rate of 23 frames/sec. The light integration time was 43 msec. The width of the coarse bars is 120 μ m, and the width of the fine bars is 60 μ m on the CCD image plane. Figure 14(a) shows the image at a near saturation exposure of approximately 4.7 μ W/cm². The bright areas in this photograph contain approximately 200,000 electrons per photoelement. Figure 15(b) and (c) show the same image when the

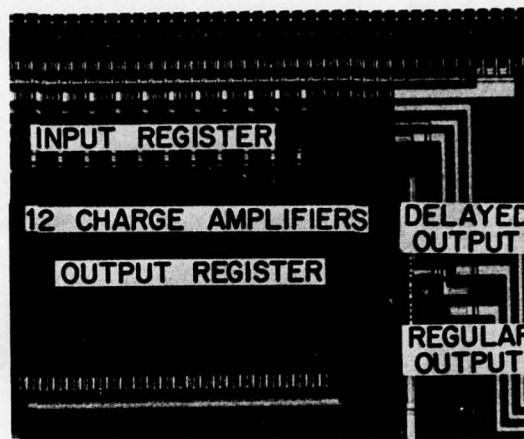


FIGURE 12 DFGA on the area sensor.

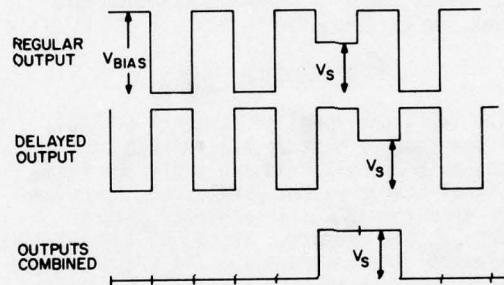


FIGURE 13 Modified DFGA output waveform.

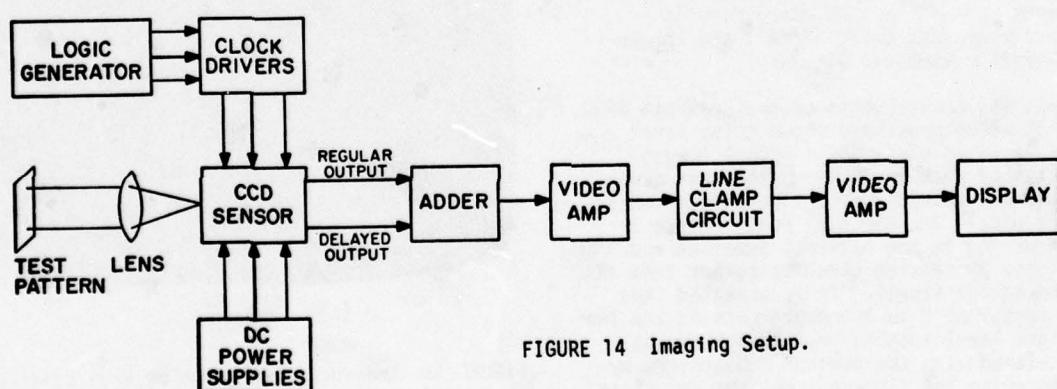


FIGURE 14 Imaging Setup.

light level is reduced by a factor of 1000 and 8000, respectively. At the 1/8000 reduction in light level, there are approximately 25 electrons per photoelement. A good transfer efficiency is maintained. The coarse (1/4 Nyquist) bars are visible and some of the fine (1/2 Nyquist) bars can also be recognized. Noise-equivalent-signal per pixel is probably 2 to 3 times higher than the 10 to 20 electron level which is predicted and measured on separate DFGA test structures.

At -10°C, the dark charge per pixel is approximately 1000 electrons. The dark charge noise should be approximately 32 electrons. The dominant noise source in Figure 15(c) is not the dark charge noise since it can not be reduced by cooling the array further. The limiting factor of the low light level performance of this array is not known. The most probable sources are the noise on the clock drivers, power supplies, and signal processing circuits.

CONCLUSION

The low light level performance of CCD image sensors have been examined. An analysis of bulk trapping indicates that signal charge packets of ten electrons can be transferred in large buried-channel CCD sensors operating at the NTSC mode. 1728-element linear arrays and 244 x 190-element area arrays both showed excellent transfer efficiency at signal levels well below 100 electrons. Using a twelve-stage DFGA, the area image sensor has demonstrated half Nyquist limit (60 μ m width) bar images at a signal level of approximately 25 electrons at -10°C. The corresponding irradiance was $6 \times 10^{-4} \mu\text{W}/\text{cm}^2$, and the integration time was 43 msec.

Separate measurements on twelve-stage DFGA test structures have shown noise level of 10 to 20 electrons. Actual images obtained with the DFGA on the area array, however, showed 2 to 3 times higher noise per pixel. The dominant noise source is suspected in the external supplies and signal processing circuits rather than in the sensor itself. It is expected that a factor of 2 to 3 improvements in the low light level imaging performance can be achieved with the present CCD sensors by improving the external supplies and signal processing circuits.

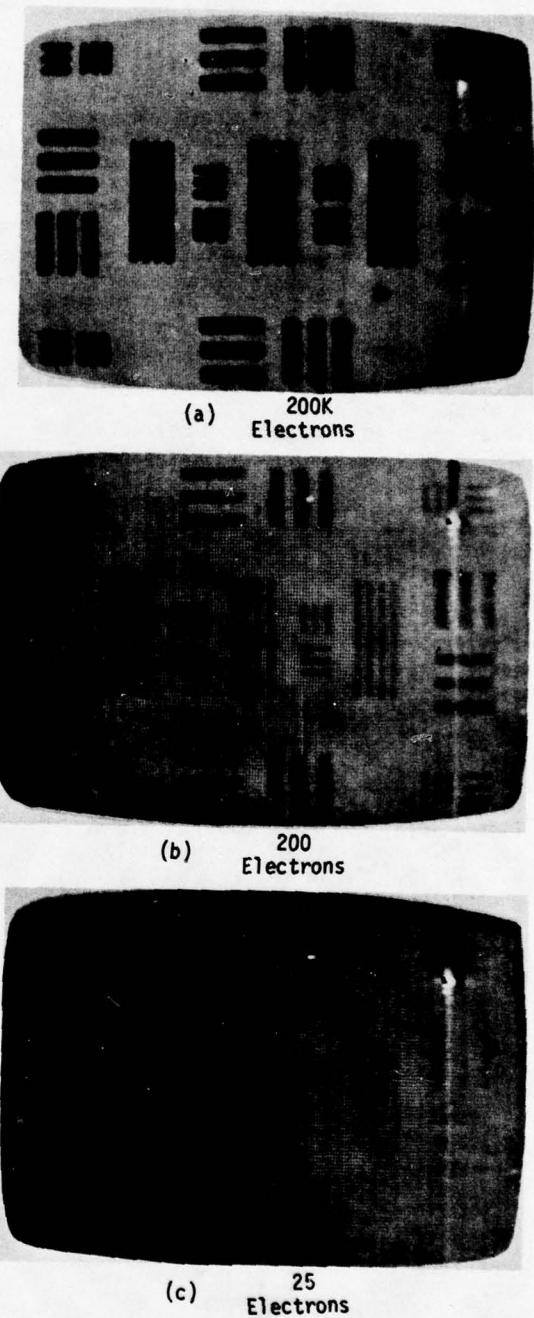


FIGURE 15 Imaging performance of area sensor.

ACKNOWLEDGEMENT

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PARAMETRIC SYSTEM ANALYSIS IN CHARGE COUPLED DEVICE IMAGING APPLICATIONS

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ABSTRACT

The advent of Charge Coupled Device (CCD) imaging sensors has required the development of specific techniques of parametric analysis which are of use to systems designers and engineers in the synthesis of electro-optical imaging systems employing these sensors. This paper describes the development and application of several of these methods and techniques including: The evaluation of a photometric/radiometric model, together with a simple method for conversion from one domain to the other; a description of a signal-to-noise model of particular applicability to this type of sensor; an analysis of operational parameter space which includes modulation considerations, noise considerations detective quantum efficiency evaluation and signal characteristics; and illustrative examples of how the techniques described may be applied.

INTRODUCTION

The applicability of Charge Coupled Device imaging sensors to specific system requirements can be readily assessed, provided the parametric analysis of the system is conducted along proper lines. In order for this to be done, it is necessary to understand the interrelationships among the functional characteristics of the devices contemplated for use in a specific application. Pre-ordained system specifications tend to force solutions to follow in such a way that if the system designer is not cautious, several device operational characteristics which are mutually exclusive (although attainable individually) may become part of the analysis. The object of this paper is to provide the Electro-Optical System Designer with the analytic tools needed for the parametric design of imaging systems employing Charge Coupled Devices.

PHOTOMETRIC/RADIOMETRIC RELATIONSHIPS

When Charge Coupled Device imaging sensors (CCD's) are used as radiation detectors, it is essential to know how the responsivity of the sensor matches the radiation output of the scene being viewed. Under unusual circumstances, the system designer has control over both the sensor and the source of scene illumination, and can therefore optimize the combination. More usually, however, the sensor must perform when coupled with naturally illuminated objects. Since scene illuminance related to such natural conditions as "sunlight", "moonlight", "starlight", etc. is generally stated in photometric units (foot candles), while electro-optical system performance is most easily evaluated on the basis of radiometric units (watts per square centimeter), it has proved highly useful in parametric analysis to develop a simple scheme by which the former may be readily converted to the latter for any given blackbody color temperature.

The relationship of blackbody source temperature (T) in degrees Kelvin is related to luminosity (lumens/watt) as shown in Figure 1.

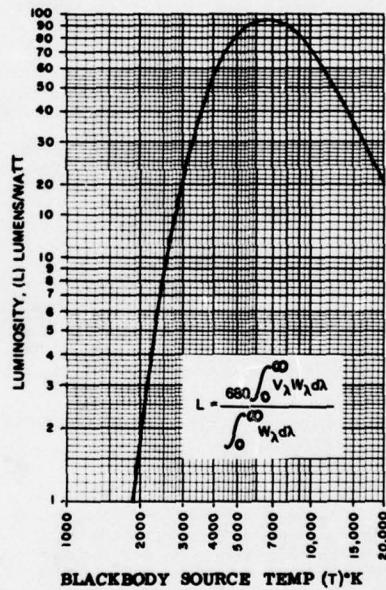


FIGURE 1. LUMINOSITY AS A FUNCTION OF BLACKBODY TEMPERATURE

Since a foot candle is defined as one lumen per square foot, a conversion to watts per square centimeter can be made using the relationship:

$$W \cdot cm^{-2} = I \cdot P$$

Where I is the illuminance in foot candles, and P a photometric/radiometric conversion factor as shown in Figure 2 where:

$$P = \frac{0.001076}{\text{Luminosity in Lumens/watt}}$$

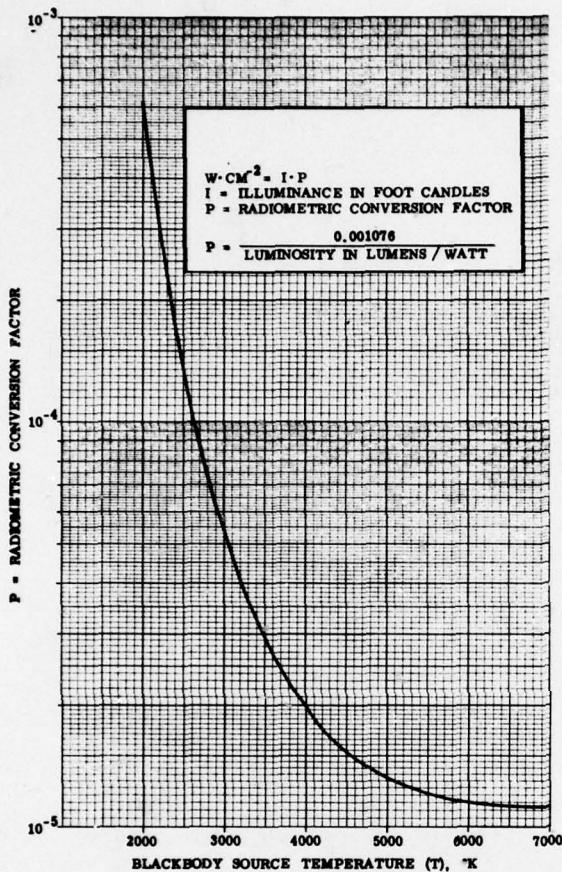


FIGURE 2. PHOTOMETRIC/RADIOMETRIC CONVERSION EXPRESSION

The desirability of going through this procedure, rather than simply working in radiometric units to begin with results from the fact that insofar as a spectrally unflat sensor working in conjunction with spectrally different sources is concerned, watts, like Orwell's animals, are not really all equal. It is necessary to evaluate sensor sensitivity to sources of different blackbody color temperatures. It is also necessary to take the blackbody color temperature of the illumination into account when performing system analysis. The cascade and integration of the appropriate values over the spectral region of interest yield radiometric values of parametric validity and utility, without the necessity for performing extended integrations of cascaded values for sensor response and illuminance data in the form of $\text{W cm}^{-2} \cdot \text{Sr}^{-1} \cdot \mu\text{m}^{-1}$.

When dealing with "sunlight", the blackbody color temperature selected as representative will differ depending upon the atmospheric path. For example, instruments in a high flying aircraft may see the earth illuminated by a source effectively significantly cooler than 5000°K while under other circumstances, solar illumination more closely approaches 6000°K . (Ref 1). The blackbody color temperature of scene illumination also varies widely with solar altitude. This change results from a variety of causes, but conforms generally to the data presented in Figure 3. The $15^{\circ}-0^{\circ}$ plane is one tilted 15 degrees from perpendicular with the sun "behind" the observer. It is apparent from the figure that as the sun approaches the horizon, the blackbody color temperature of the illumination decreases so that, at sunset, one is likely dealing with illumination in the 2854°K (nominal tungsten) color temperature region.

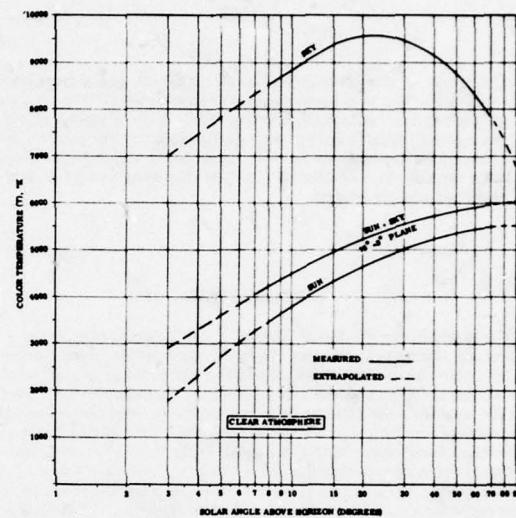


FIGURE 3. RELATIONSHIPS AMONG SOLAR ELEVATION ANGLE AND ILLUMINATION COLOR TEMPERATURE

Because of their high level of sensitivity CCD image sensors have been hypothesized for use in low light level applications. The moving image integrating mode device (described in another paper presented at this conference) is one example of a sensor especially designed for low light level use. Illumination conditions change not only quantitatively, but qualitatively when natural light levels fall. When the sun is well below the horizon, and the moon is taken as the chief source of illumination, the resultant blackbody color temperature may be seen to be highly dependent upon the altitude and phase of the moon (Ref 2). This is shown in Figure 4 where the relative radiance of different lunar illumination conditions are shown as a function of wavelength. Plotted together with the illumination data are straight-line approximations of blackbody curve segments for the indicated spectral interval. These approximations were obtained by joining the 500 nm and 1100 nm portions of the respective blackbody curves by a straight line. As is shown in the Figure, the blackbody color temperature varies from about 2854°K , with no moon, to about 5400°K with nearly full moon at a 45 degree altitude.

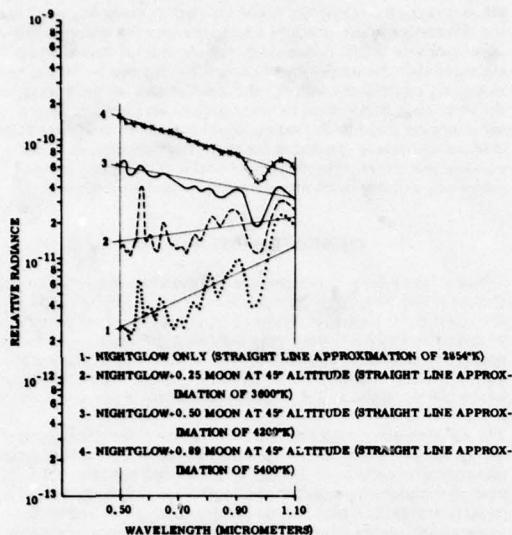


FIGURE 4. RELATIONSHIPS AMONG ILLUMINATION CONDITIONS AND BLACKBODY SOURCE TEMPERATURE

The extreme condition represented by the illumination received from starlight and airglow alone may be evaluated through the use of Figure 5. The Figure shows the relative number of photons emitted by a blackbody as a function of wavelength. It also has plotted on it (at the same scale) the relative number of photons collected at the surface of the earth from the night sky (starlight plus airglow) (Ref 3). By mentally "sliding" the plot of night sky photons over the figure, one may arrive at a "best fit" between the data. It is apparent that this fit occurs somewhere in the region of 2854°K–3000°K.

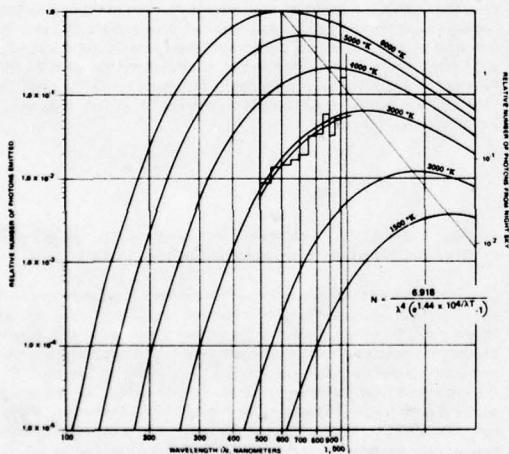


FIGURE 5. COMPARISON OF NIGHT SKY PHOTON COUNT VS. WAVELENGTH WITH BLACKBODY CHARACTERISTICS

Since daytime operation would not require performance at a blackbody color temperature greater than 6000°K, it may be concluded that the viability of a CCD image sensor system depends upon its ability to function within the blackbody color temperature range of 2800°K–6000°K.

BLACKBODY SOURCE DEVICE RESPONSIVITY

The responsivity (ρ) of the type of silicon used in the subject devices has been evaluated as shown in Figure 6. The values of ρ_λ (spectral responsivity) were taken from measured Fairchild data. It must be noted that the responsivities which may be taken from the graph refer to light which has "gotten into" the silicon. If no special steps were taken to develop a structure receipt to optimize the optical admittance factor, the achievable practical sensitivity could reach only about 35 per cent of the theoretical values shown on the graph.

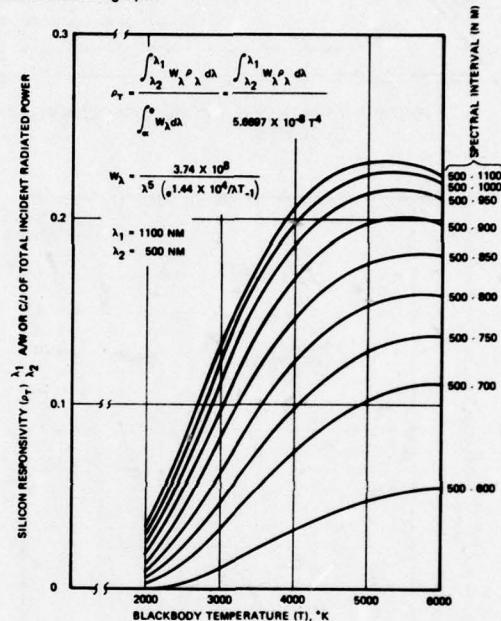


FIGURE 6. SILICON RESPONSIVITY AS A FUNCTION OF BLACKBODY SOURCE TEMPERATURE FOR VARIOUS SPECTRAL INTERVALS

Because of optical interference effects and simple absorption by the several layers of different materials comprising the CCD image sensor structure, the spectral responsivity of a specific device will be dependent upon its construction. (For example, linear devices may require only one layer of polycrystalline silicon, while area devices may require two or more). These effects must be accounted in the determination of specific device responsivity. As an example of what can be accomplished interactively between the system designer and the sensor manufacturer, consider the results of a recent experiment. By using current analytical structure design methods and a newly developed evaluation program, it has proved possible to engineer practical manufacturable layering structures for the subject devices which will more than double the original rather pessimistic responsivity estimate. Twelve such improved structure receipts were selected from a series of 100 evaluated.

Of the twelve, receipt No. 8 was found to be optimum over the blackbody color temperature range of from 2000°K to 6000°K. Data for the optimum improved structure are presented in Figure 7&8. The integral evaluated in this latter case includes the expression T_{λ} so that the resultant responsivity values are those which can be attained when all reflection and unwanted absorption losses are accounted.

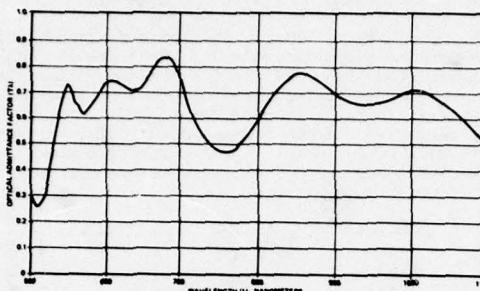


FIGURE 7. OPTICAL ADMITTANCE FACTOR FOR RECEIPT 8

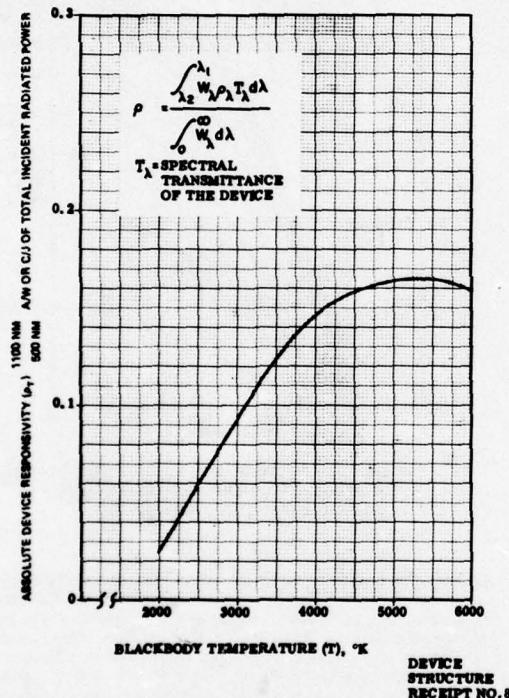


FIGURE 8. DEVICE SENSITIVITY AS A FUNCTION OF BLACKBODY SOURCE TEMPERATURE FOR THE SPECTRAL INTERVAL 500-1100 NANOMETERS

While Structure Receipt No. 8 was the best of the group developed, the differences in performance among the selected group of twelve were relatively small. Subsequent manufacture of devices in accordance with the model specifications yielded sensors whose responsivity equaled or exceeded the predictions. In most instances the fortuitous relationship between system designer and device manufacturer cited in this example will more than likely not exist. It remains crucially important for the system designer to know, evaluate and understand the impact of the illumination source/sensor responsivity relationship on system performance.

SIGNAL TO NOISE MODEL

The analysis of sensor performance in a system is directly tied to the definition of a suitable system input signal to noise ratio (S/N). Although the two general classes of CCD image sensors (linear devices and area devices) operate in somewhat different ways, it is possible to develop such a model applicable to both. The model may also be applied to the moving image integrating mode device, which can be considered as a special case of the linear sensor type.

The signal to noise model presented here was originally developed for use in calculating predicted performance for the moving image integrating mode type of device. In the model, the term (η) is used to designate the number of integrations. The same model is directly applied to linear devices (in this case ($\eta = 1$) and with a somatic difference to area sensors where the readout of several frames may be integrated by the eye-brain combination of the observer via a visual display. In this latter instance (η) is redefined as the number of visual integrations performed within the integration period of the eye ($\cong 0.2$ Seconds).

A fundamental requirement for an imaging system analysis is the derivation of a mathematical expression for the calculation of the resultant system input signal-to-noise ratio in terms of the various system and mission parameters.

This expression will first be developed for an ideal system, i.e., one that contributes no system noise. For the ideal noiseless system, the only noise present is the statistical noise of the signal itself. A sufficiently close approximation is obtained by considering that part of the system having the lowest discrete unit count as a representation of the signal value. In an electro-optical system, that point is usually the electron stream immediately following the photoelectric conversion whether this be by a photo cathode emitting electrons in a vacuum tube or generation in a solid state photoconductor. The number of electrons representing the "signal" and the number of electrons representing the "noise" or "signal uncertainty" are the valid quantities to use. The signal-to-noise ratio is then:

$$(S/N) = \frac{\epsilon_s}{\epsilon_n}$$

where ϵ_s = the number of electrons representing the "signal" and ϵ_n = the number of electrons representing the "noise".

In an imaging system, where the ultimate final interpretative receiver and decision mechanism is the eye - brain combination, the "signal" which is meaningful is the difference in gray level between one small scene area and an adjacent one - the image characteristics which the brain has been trained to interpret as "detail", as distinguished from the interpretation of "no detail" for an area of uniform gray level. Therefore, for a meaningful analysis of a system's capabilities, it is customary to analyze its treatment of certain specific targets - such as the USAF standard tri-bar target. For such a target, which contains repetitive lines and spaces, we consider one line pair, i.e., one bar and one space and then the signal is:

$$\epsilon_s = \epsilon_{s_{\max}} - \epsilon_{s_{\min}}$$

where $\epsilon_{s_{\max}}$ = the number of electrons from the brighter area, i.e., a bar.

$\epsilon_{s_{\min}}$ = the number of electrons from the dimmer area, i.e., the space between bars.

and the noise is:

$$\epsilon_n = \sqrt{\epsilon_{s_{\max}} + \epsilon_{s_{\min}}}$$

To evaluate these terms:

$$\epsilon_{s_{\max}} = 6.24 \times 10^{18} \rho I_{\max} P \eta t a_{\text{bar}}$$

$$\epsilon_{s_{\min}} = 6.24 \times 10^{18} \rho I_{\min} P \eta t a_{\text{space}}$$

where: ρ is the photo-electric responsivity in amp/watt

I_{\max} is the illuminance of the bar on the image plane

I_{\min} is the illuminance of the space on the image plane

P is the photometric to radiometric conversion factor for the particular radiation

$\eta \cdot t$ is the integration time (η = number of integrations, t = element exposure time)

a_{bar} is the area of the bar in the image plane

a_{space} is the area of the space in the image plane

For the target referenced, and for this analysis:

$$a_{\text{bar}} = a_{\text{space}} = \sigma a$$

σ = the number of "pixels" in a bar

where, by definition:

a = area of a pixel

$a = \delta^2$ (assumed square pixel)

δ = photosite side dimension

For convenience, substitute C for $6.24 \times 10^{18} \rho P \eta t a \sigma$

The expression for the Signal to Noise Ratio is:

$$\frac{\epsilon_{s_{\max}} - \epsilon_{s_{\min}}}{\sqrt{\epsilon_{s_{\max}} + \epsilon_{s_{\min}}}} = \frac{C(I_{\max} - I_{\min})}{\sqrt{C(I_{\max} + I_{\min})}}$$

The Sensor MTF describes the ratio of an output signal to the input signal. It is a useful parameter for analyzing the capabilities of imaging systems. The MTF is a spatial frequency dependent term and applies to the sinusoidal signal component for a particular spatial frequency. When dealing with periodic bar targets the MTF is somewhat different than for sinusoidal ones. However, the implicit simplifying assumption that the MTF is not different has been made here. It follows then that the sensor MTF, denoted by M, is as follows:

$$M = \begin{cases} \frac{(I_{\max} - I_{\min})}{(I_{\max} + I_{\min})} & \text{out} \\ \frac{(I_{\max} - I_{\min})}{(I_{\max} + I_{\min})} & \text{in} \\ \frac{(I_{\max} - I_{\min})}{(I_{\max} + I_{\min})} & \text{in} \end{cases}$$

where I_{\max} and I_{\min} are the signal intensities for the maximum and the minimum signals respectively. Since the system is assumed to be linear and since no energy is either added or lost, but is only redistributed between the bars and spaces,

$$(I_{\max} + I_{\min}) \text{ out} = S(I_{\max} + I_{\min}) \text{ in}$$

where S is a scale factor:

$$\frac{M \cdot S(I_{\max} - I_{\min}) \text{ in}}{S(I_{\max} + I_{\min}) \text{ in}} = \frac{(I_{\max} - I_{\min}) \text{ out}}{(I_{\max} + I_{\min}) \text{ out}}$$

or, cancelling out the denominators, which are equal:

$$M \cdot S(I_{\max} - I_{\min}) \text{ in} = (I_{\max} - I_{\min}) \text{ out}$$

Substituting in the sensor signal-to-noise expression,

$$\frac{\epsilon_s}{\epsilon_n} = \frac{C \cdot S(I_{\max} - I_{\min}) \text{ in} \cdot M}{\sqrt{C \cdot S(I_{\max} + I_{\min}) \text{ in}}}$$

$$(I_{\max}) \text{ in} = I \cdot R_{\max}$$

$$(I_{\min}) \text{ in} = I \cdot R_{\min}$$

Where

I = Illuminance of the bar in the object plane

R_{\max} = Reflectance of the bar

R_{\min} = Reflectance of the space

$$(I_{\max} - I_{\min}) \text{ in} = I(R_{\max} - R_{\min})$$

$$(I_{\max} + I_{\min}) \text{ in} = I(R_{\max} + R_{\min})$$

Substituting:

$$\frac{\epsilon_s}{\epsilon_n} = \frac{C \cdot S \cdot I \cdot M (R_{\max} - R_{\min})}{\sqrt{C \cdot S \cdot I (R_{\max} + R_{\min})}}$$

The scale factor of a linear imaging system is:

$$S = \frac{(I) \text{ out}}{(I) \text{ in}}$$

where

$$(I) \text{ out} = I_j = \text{the image illuminance}$$

$$(I) \text{ in} = B_0 = \text{the object brightness}$$

The relationship is:

$$I_i = \frac{B_0}{4(T\#)^2}$$

$$S = \frac{1}{4(T\#)^2}$$

Where there is an intervening atmosphere,

$$CSI = \frac{6.24 \times 10^{18} \rho P_{\text{IR}} \alpha T}{4(T\#)^2} = Q$$

where T is the atmospheric transmission

or:

$$\left(\frac{S}{N}\right) = \frac{\epsilon_s}{\epsilon_n} = \frac{Q(R_{\max} - R_{\min})M}{\sqrt{Q} \sqrt{(R_{\max} + R_{\min})}} = \frac{\sqrt{Q}(R_{\max} - R_{\min})M}{\sqrt{R_{\max} + R_{\min}}}$$

for the noiseless case.

When additional "non-quantum" noise is present, the expression becomes more complex:

$$\left(\frac{S}{N}\right) = \frac{\epsilon_s}{\epsilon_n} = \frac{Q(R_{\max} - R_{\min})M}{\sqrt{Q}(R_{\max} + R_{\min}) + \sigma \beta^2}$$

Where β is the number of uncancelable noise electrons per pixel referred to the input of the on-chip amplifier.

The relationship between the value of the quantity (S/N) as derived here and system "resolution" ultimately involves an observer. Whether that observer looks at a video "soft copy" presentation or a "hard copy" output will depend upon system-specific requirements.

Threshold observed signal-to-noise ratio values required for an observer to perceive image information for both "soft copy" (live) and "hard copy" displays have been extensively investigated over the past few decades. Refs 4, 5. Although psychophysical aspects of the perception problem have yet to be established on a firm theoretical basis, a number of investigators have successfully demonstrated system analytical techniques based on models of the vision process formulated to conform with the results of numerous controlled experiments. Results specifically applicable to CCD imaging sensor systems include:

Simple aperiodic shapes such as disks and squares viewed against a uniform background have been found to require signal-to-noise ratios perceived by the observer of $\geq 5:1$ for observers viewing images with temporally-fixed noise and signal patterns (i.e., hard copy or stored single-frame television displays). In this case (S/N) is given by the signal to RMS noise ratio determined for the total aperiodic image area and an equivalent area of adjacent background. The "signal" in the photographic image case is the mean difference in events (i.e., darkened specks on film) between the image and background areas, while the noise is determined by the RMS value of background (non-signal) noise events for both areas.

Photographic images of periodic test patterns, such as U.S.A.F. three bar test targets, may be resolved with threshold (S/N) values $\geq 4:1$ where (S/N) is determined over image and background areas equivalent in size to the area of a single test pattern bar. Ref 6. The criterion adopted here was 50 per cent probability for the detection of line structure in one of the two orientations of three bar images presented to the observer.

In addition to the above, results for television imaging show that long rectangular areas (viewfield angular subtense $0.5^0 \times 6^0$) are detected with threshold observed (S/N) values $\geq 3:1$.

The latter result suggests a remarkable observational ability for effective integration over the entire length of long lines. For a rectangular area of height $= 20 \times$ width ($a = 20$) the corresponding elemental (S/N) value for an area of height equal bar width is only $3\sqrt{20} \approx 0.7:1$. These experimental results are confirmed by the critical nature of coherent signature problems, which must be controlled to eliminate streaking in the display output of line-scanning systems.

From the foregoing, we can deduce that "worst case" (S/N) requirements correspond to the detection of objects with image dimensions at the array approaching the minimum sample aperture size of the CCD sensor chip.

Investigation of threshold signal-to-noise ratio requirements for "night vision" applications have been primarily concerned with "live" viewing conditions, with the observer viewing images containing temporal noise variations. Threshold observed (S/N) values appropriate to the latter viewing condition are computed using an assumed value for the effective eye integration time, i.e., 0.1 to 0.2 second for normal display illuminance levels.

The (S/N) model developed above includes the term (η) , the number of picture integrations. These integrations may be obtained thru the use of a moving image mode integrating sensor chip, or thru the addition of information in the brain of the observer viewing a "live" display. In the latter case, the number of integrations is limited by the integration time of the eye, while in the former it is a function of sensor chip construction. In either event, the integration effect is accounted in the model, so that a minimum value for (S/N) corresponding to a 50 per cent probability of "resolution" is ≥ 4 .

Similarly, the (S/N) model considers the aspect ratio of a line or periodic target, since the number of pixels in a "bar" (a) is included in its calculation. This also causes convergence of the required (S/N) to ≥ 4 for 50 per cent probable "resolution". While no hard and fast rule may be established to relate (S/N) values as calculated from the derived model to "resolution", the selection of $(S/N) = 4$ as a minimum requirement for periodic targets has been applied with considerable success.

OPERATIONAL PARAMETER SPACE

Having derived the appropriate system input signal-to-noise ratio (S/N) , it is necessary to determine the interrelationships among those sensor characteristics that effect the quantities in the expression:

$$(S/N) = \frac{Q(R_{\max} - R_{\min})M}{\sqrt{Q(R_{\max} + R_{\min}) + \sigma \beta^2}}$$

Let us examine each of the quantities in that expression and the effects of sensor characteristics upon their quantification.

FACTORS IMPACTING SIGNAL LEVEL

The quantity "Q" has been defined as:

$$Q = \frac{6.24 \times 10^{18} \rho P \cdot I_{\text{max}} \sigma T}{4(T\#)^2}$$

6.24×10^{18} is the number of electrons per coulomb and is constant.

" ρ " is the responsivity of the sensor in coulombs/joule or amps/watt. This quantity varies with the wavelength or color temperature of the illumination, which must be considered in selecting the proper value for ρ . Rho is based on a 100 per cent area utilization factor in the chip.

" $P \cdot I$ " is the product of the scene illumination in foot candles and a Photometric-Radiometric conversion constant which in turn is dependent upon illumination color temperature. It assumes that the illumination source is a blackbody. If this is not the case, the values for ρ and the equivalent of $P \cdot I$ (in watts/cm² on the scene) must be appropriately computed. The type and color temperature of the illumination also effects such parameters as crosstalk, and array MTF (m_{array}).

" η " is the number of image integrations - either during image gathering (as with a moving image integrating mode chip) or during display (based on the time-constant of the eye). System requirements for specific light level performance or display characteristics may influence the needed value.

" t " is the elemental exposure time in seconds. This will be determined by the frame repetition rate or the linear device read-out rate in frames or lines per second respectively. In terms of system operation, these rates may be established from such diverse requirements as vehicle rate, scene overlap, ambient light level, or display frequency.

" a " is the area of a pixel. It applies to the entire area of a picture element (active area plus inactive area). Note that responsivity (ρ) is also computed on the basis of total pixel area. Coupled with the object space system resolution requirements, the pixel size tends to define the required optical scale of the system.

" σ " is the number of pixels in the area of a bar of a (square wave or tribar) bar type of target.

" T^* " is the atmospheric transmission.

" $(T\#)$ " is the (F#) of the optical system divided by the square root of the optical transmission of that system.

The quantities most amenable to trade-off in the course of system analysis are exposure time (t), $(T\#)$, and (σ) . The latter is directly connected with image resolution.

The maximum and minimum scene reflectances R_{max} and R_{min} are most likely either specified or implied by the system specification. In any event, they are not variable from the system trade-off analysis standpoint. However, their absolute values, as well as the target contrast ratios, are important in system analysis.

MODULATION CONSIDERATIONS

The quantity M which appears in all S/N computations is used to designate the Modulation Transfer Function of the "system" and consists of the following factors:

$$M = (m_{\text{optics}}) (m_{\text{motion}}) (m_{\text{array}})$$

It should be noted immediately that the evaluation of "M" does not contain constant terms for either the modulation of the optics or the scene contrast ratio. Even though, for simplification of calculations a constant m_{optics} may be assumed, the quantity is spatial frequency dependent and must ultimately be recognized as such. The scene contrast ratio (in terms of R_{max} and R_{min}) is also accounted for in the (S/N) computation, but not as a "modulation" term.

The first of the cascaded values which go to make up the system MTF (M) to be considered is m_{optics} . System designers are familiar with the variation of m_{optics} with spatial frequency. However, a note of caution if appropriate. Many attempts are made to configure CCD image sensor based systems around photographic optics which were designed for optimum performance within a different spectral domain than the "wide-open" silicon response spectrum. The values for m_{optics} used in system performance prediction must correspond to the weighted spectral interval appropriate to the operational system.

The evaluation of the effects of image motion must be conducted differently for cases where such image motion is inadvertent (due to platform instability, object motion etc) and where the motion of the image past a linear sensor is implicit in the generation of one dimension of the picture (strip mode or panoramic cameras for example).

In the first instance, where undesired image motion during exposure is encountered, the MTF due to motion (m_{motion}) may be evaluated from the expression:

$$m_{\text{motion}} = \frac{\sin(\pi\theta f t R)}{(\pi\theta f t R)}$$

where θ is the image motion rate in radians per second, f the lens focal length in units of length consistent with R , the spatial frequency of interest in line pairs per unit length.

Where image motion past a linear sensor is used to generate one dimension of the "picture", the linear rate of image motion (V) and the exposure time (t) combine to establish the value for m_{motion} for a given spatial frequency (R)

$$m_{\text{motion}} = \frac{\sin(\pi V R t)}{\pi V R t}$$

Note that the number of integrations no longer forms a part of the expression.

For a given spatial frequency R , it can be shown that

$$(S/N)_R \approx \frac{\sin(\pi W)}{\pi W}$$

where W is the image motion in lp/sec. and also that:

$$(S/N)_R = \max \text{ when the argument } \sin(\pi W) = 1 \\ \text{or, } Wt = 1/2R$$

which implies that the maximum $(S/N)_R$ is obtained when one line readout is made per $1/2R$ wide line progression in the image.

Strictly speaking, the optimization applies only to the spatial frequency R . A small gain in "resolution" may be obtained by reading out the array more than once per line progression in the image even though this degrades the value of (S/N) at spatial frequency R . This follows from the fact that even for a value of R corresponding to the Nyquist limit (the limiting geometrical unambiguous resolution of the sensor is set at the Nyquist limit) the sensor may well exhibit response beyond that frequency. With more than one readout per line progression, a greater amount of these higher frequency components may be passed by the system resulting in sharper edges even though the (S/N) at spatial frequency R is no longer optimum. In instances where there is an image motion error associated with the picture generation by a scanning linear sensor, the MTF contribution of the error can be calculated from the same general sinc function as that given previously for inadvertent image motion viz:

$$m_{\text{motion}} = \frac{\sin(\pi\theta\eta fR)}{\pi\theta\eta fR}$$

In this instance θ is the image motion error rate in radians per second, and η is normally unity for a linear sensor.

The MTF of the array (m_{array}) is a quantity which varies not only as a function of sensor geometry, but with several operational characteristics as well. Also the combinations of operating characteristics possible within the permissible working range of a given sensor may result in very significantly different values for m_{array} . The MTF of the array must be modeled in accordance with the conditions of use in the system and the appropriate values used in the system performance prediction calculations. Different types of devices (frame-transfer devices and interline transfer devices for example) exhibit different array MTF characteristics. Ref 7. The specific properties of each system candidate array should be investigated using whatever device MTF model is appropriate. As an example, an MTF model for a typical linear array under one set of operating conditions is presented in Figure 9. The curve labeled "model" represents the "most likely" phase relationship between a square wave target and the array. Experimental data points obtained from 1×500 element linear arrays are also shown in the Figure. It may be seen that the experimental points agree reasonably well with the derived model for the conditions assumed for this system.

Unfortunately, there is no single characteristic curve of m_{array} for a given image sensor device. Instead, the parameter varies as a function of several system-connected operational characteristics. The most significant of these areas effecting this spatial frequency dependent parameter includes:

- Array Geometry
- Readout Rate
- Illumination Color Temperature (Cross Talk)
- Charge Transfer Efficiency (which in turn is effected by)
 - Signal Level
 - Operating Temperature
 - Device Type

Succinct questions as to these sensor and system characteristics must be asked and answered by the system designer in the course of preparing the array MTF model to be used in subsequent system analysis. Failure to generate a model of the necessary accuracy can lead to grossly inaccurate performance predictions.

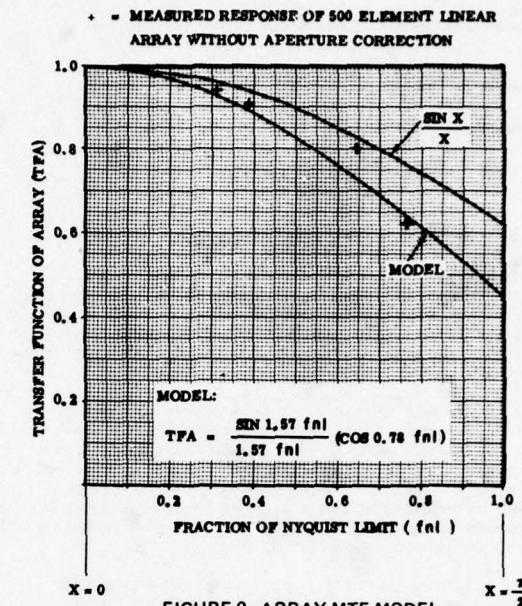


FIGURE 9. ARRAY MTF MODEL

NOISE CONSIDERATIONS

The final quantity in the expression for (S/N) is (β) , the number of uncancelable noise electrons referred to the input of the on-chip amplifier associated with each pixel readout. This constitutes the non-quantum noise of the sensor and is Root Sum Squared with the quantum noise in the determination of (S/N) .

No attempt is made in this paper to establish all the physical sources of noise within a CCD imaging sensor chip, since from a system designer's point of view the precise source of the noise is of only academic interest. There are however two generalized sources of noise electrons: Those associated with thermal generation within the sensor chip, and those having their origin elsewhere.

Thermally generated noise electrons are the result of dark current statistics (uniform dark current itself can be electrically canceled) and dark current non-uniformities. While quite low values of dark current density ($10nA/cm^2$ is not atypical) are commonly measured, the mistake of multiplying this density times the pixel area to determine the dark signal must be assiduously avoided. It must be remembered that the photosensitive area is not the only portion of the sensor real-estate contributing to the dark signal. So while on the basis of $10nA/cm^2$ dark current density one might compute the dark signal for a pixel to be of the order of from 10 to 100 electrons in a $53\mu s$ integration time the actual dark signal for a commercial device with these characteristics averages more nearly 2500 electrons dark signal with a dark signal statistics noise contribution of 50 electrons (at $25^\circ C$).

Dark signal non-uniformity is generally described in terms of "per cent". This does not refer to per cent of average dark signal, but to per cent of saturation signal. Variations in dark signal of as much as 1 per cent of saturation are not uncommon in today's devices operating at $25^\circ C$. For a sensor with a pixel which is saturated by 250,000 electrons, this corresponds to 2500 electrons. Such a number, though

large, is not particularly bothersome when the device is operating at signal levels of 50 per cent saturation or above. However, let the signal level drop to 1 per cent of saturation, and the impact of the dark signal non-uniformity is severely felt.

The system designer has within his control an option whereby the effects of thermally generated noise may be greatly minimized or essentially eliminated. He may elect to cool the sensor. By "Rule of Thumb", the number of thermally generated electrons is halved for every 9°C drop in operating temperature. A plot of the Dark Charge Temperature Characteristic for a sample device is presented in Figure 10. Since cooling is effective against variations in dark signal as well as against dark signal itself, the 2,500 noise spike electrons per pixel given in the previous example (with the sensor operating at 25°C) would be reduced to 20 noise electrons by cooling the sensor to -38°C . Meanwhile, the average dark signal level of the example would have similarly been reduced from 2500 to 20 with the dark signal statistics noise equal to 4.5 electrons per pixel.

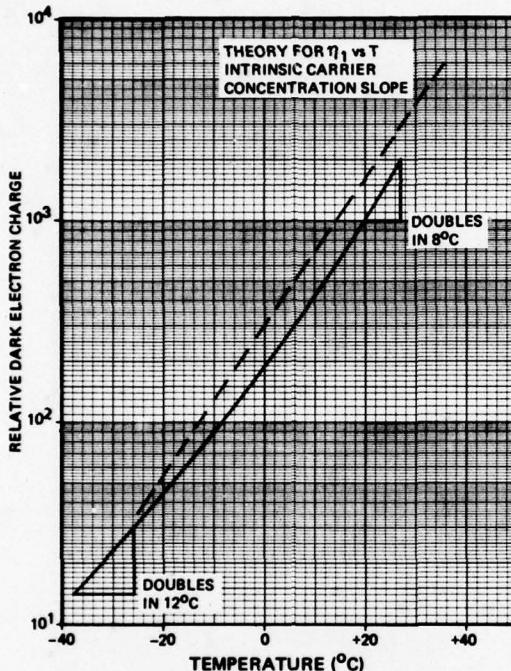


FIGURE 10. TYPICAL DARK CHARGE TEMPERATURE CHARACTERISTICS

Whether or not cooling the sensor will offer a system advantage depends upon what forms the predominant noise source in the specific sensor device being considered. In many instances, the dominant noise source is in the on-chip amplifier and/or the way in which the sensor array is read out. When such is the case, the effects of cooling are to eliminate the few large dark signal variation spikes and to lower the overall RMS noise level slightly, but to not dramatically improve the imagery obtained. Cooling of the

sensor chip does have a minimizing effect on other (non dark-signal associated) noise sources. Both kT/c noise and Johnson noise for example are reduced somewhat when the sensor is cooled. However, the effect on such noise sources is small compared to the effect on dark signal related noises. Therefore, the system decision as to whether or not to cool a given sensor chip will most probably be regulated by the relative importance of dark signal associated noise.

Of the types of on-chip amplifiers in use today or contemplated for the near future, two generalized categories exist: The gated charge integrator (used either alone or in combination with an on-chip compensation amplifier), and the floating gate amplifier (the latter can be of one or multiple stages, with the multiple stage version being described as a distributed floating gate amplifier). The number of noise electrons per pixel readout associated with specific amplifiers may vary from as many as 2000 to as few as 20. Generally speaking the relative ranking (from least to most "noisy") is: distributed floating gate, floating gate, gated charge integrator with on-chip compensation amplifier, and the uncompensated gated charge integrator.

One might reasonably ask why a single amplifier type (logically the least "noisy") is simply not settled down upon for all applications, and the entire matter set to rest for all time. Unfortunately, low noise demands a price, and that price is usually a reduced amplifier saturation threshold. The implication of this for system applications is reduced in-scene dynamic range reproduction.

From a system designer's point of view it would be optimum to have each sensor chip come equipped with multiple on-chip amplifier options so that the optimum amplifier could be switched on-line with varying operational conditions. Experimental sensor chips incorporating such a feature have been produced.

The noise metric used in the (S/N) model involve the quantity (β) which represents the number of uncancelable noise electrons referred to the input of the on-chip amplifier. Deriving this quantity from published device data at times presents a challenge. The approach usually taken is to reduce the published noise equivalent signal or noise equivalent exposure data to an equivalent number of electrons. If cooling below the temperature at which values for these quantities were obtained is anticipated, the specific effects of this cooling on (β) must be calculated or obtained from the manufacturer.

DETECTIVE QUANTUM EFFICIENCY CONSIDERATIONS

A part of any system analysis which considers the use of CCD imagers logically involves comparison with other sensor types. One such type of comparison involves the use of the quantity Detective Quantum Efficiency (DQE). While DQE does not constitute a single simple figure of merit, it is one significant performance characteristic. It describes how efficiently the detector makes use of the information present in a photon image. (Ref 8). It may be mathematically defined as:

$$\text{DQE} = \frac{(S/N)^2_{\text{out}}}{(S/N)^2_{\text{in}}}$$

In this instance the value of (S/N) calculated for our model represents (S/N) out, while the ideal (S/N) inherent in the signal sensed by a perfect sensor represents (S/N) in.

$$\text{Now, } (S/N)_{\text{out}} = \frac{Q (R_{\max} - R_{\min}) M}{\sqrt{Q (R_{\max} + R_{\min}) + \alpha^2}}$$

where

$$Q = \frac{6.24 \times 10^{18} \rho_T^* P I \eta \alpha \sigma T}{4(T\#)^2}$$

For the ideal case,

$$(S/N)_{in} = \frac{Q^* (R_{max} - R_{min}) M}{\sqrt{Q^* (R_{max} + R_{min})}}$$

where

$$Q^* = \frac{6.24 \times 10^{18} \rho_T^* P I \eta \alpha \sigma T}{4(T\#)^2}$$

and

ρ_T^* = Blackbody responsivity of a 100% quantum efficient detector at a blackbody temperature T

$$\rho_T^* = \frac{\lambda_1}{\lambda_2} \frac{8.068 \times 10^{-1} W_\lambda d\lambda}{5.6697 \times 10^{-8} T^4}$$

and,

$$W_\lambda = \frac{3.74 \times 10^8}{\lambda^5 (e^{1.4388 \times 10^4 / \lambda T} - 1)}$$

also,

$$Q^* = Q \frac{\rho_T^*}{\rho_T}$$

Now, by definition (S/N) for a "noiseless" system is \sqrt{Q} when all modulation, reflectivity, and transmission terms are disregarded. For this case then, $(S/N)_{in}^2 = Q^*$

and

$$(S/N)_{out}^2 = \frac{Q^2}{Q + \beta^2}$$

and

$$DQE = \frac{Q^2}{Q^* (Q + \beta^2)}$$

For completely "real world" cases,

$$(S/N)_{out}^2 = \frac{Q^2 (R_{max} - R_{min})^2 M^2}{Q (R_{max} + R_{min}) + \alpha \beta^2}$$

and

$$(S/N)_{in}^2 = \frac{Q^2 (R_{max} - R_{min})^2 M^2}{Q^* (R_{max} + R_{min})}$$

from which

$$DQE = \frac{Q^2}{Q^*} \times \frac{(R_{max} + R_{min})}{[Q(R_{max} + R_{min}) + \alpha \beta^2]}$$

As an example we have taken the case of an ideal detector and plotted its responsivity alongside that of a CCD imaging sensor having the characteristics represented of Receipt 8. These data are shown in Figure 11.

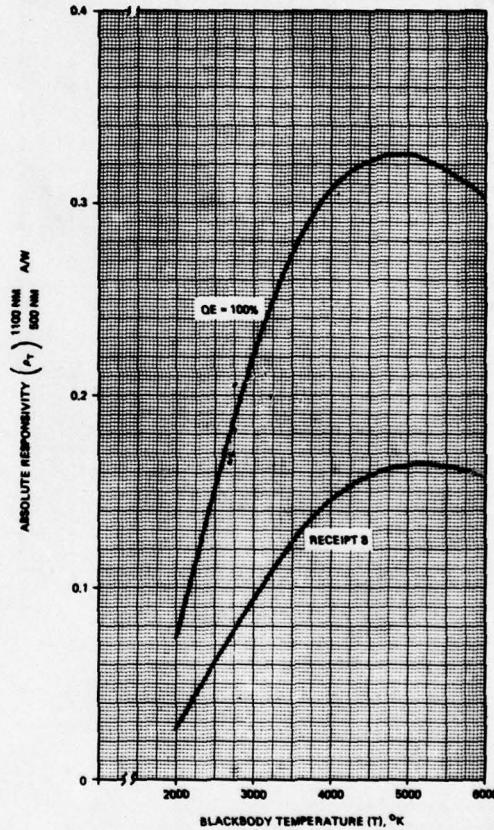


FIGURE 11. RESPONSIVITY AS A FUNCTION OF BLACKBODY TEMPERATURE FOR REAL AND IDEAL DEVICES

For a situation where:

$$\begin{aligned}
 T &= 6000^{\circ}\text{K} \\
 R_{\max} &= 0.5 \\
 R_{\min} &= 0.25 \\
 \beta &= 40 \text{ electrons} \\
 \rho &= \text{Receipt 8} \\
 \sigma &= 5
 \end{aligned}$$

The Detective Quantum Efficiency is computed to be a function of Q as shown in Table I.

TABLE I
RELATIONSHIPS BETWEEN SIGNAL LEVEL
AND DQE FOR ONE EXAMPLE

Q ELECTRONS PER SIGNAL AREA	ELECTRONS PER PIXEL	Q* IDEAL ELECTRONS PER SIGNAL AREA	DQE
100,000	20,000	190,000	0.475
10,000	2,000	19,000	0.254
1,000	200	1,900	0.045
100	20	190	0.005

EXAMPLE

The following example of system calculations is presented not as a solution to any particular "real world" problem, but rather as a guide to the application of the methods described in the previous sections of this paper. The device characteristics chosen are not specifically representative of a particular sensor, but fall within the current State of the Art.

SYSTEM REQUIREMENTS

A low altitude reconnaissance aircraft is to fly at an altitude of 3000 feet at a maximum V/H of 0.15 knots per foot.

Scene illumination will be daylight, down to sun angles corresponding to 100 foot candles scene illuminance (minimum) with cloud cover.

Scene contrast ratios of 2:1 and above are anticipated, with average scene reflectivities of 0.3.

Ground resolution of 6" per line pair is desired.

Continuous angular coverage of $\pm 20^{\circ}$ from nadir is required.

TENTATIVE SYSTEM CONCEPT

As a starting point the system designer might consider a strip mode type of system consisting of a series of linear sensor chips arranged to form a (optically or electronically) contiguous line in the image plane of a vertically oriented objective lens. It is necessary to check this concept against available sensor characteristics.

ASSUMED SENSOR DEVICE SPECIFICATIONS

- Type: 1 x 1500 pixel linear chip
- Pixel Size: 0.0007" x 0.0007"
- Active Pixel Area: 100%
- Responsivity: In accordance with Figure 8
- Dynamic Range: 1000:1
- Saturation: 300,000 electrons
- Average Dark Signal: 50 electrons/ $\mu\text{Sec}/\text{Pixel}$ at 25°C
- Dark Signal Non-Uniformity: 1% of Saturation
- Readout Rate: 0.1 - 6.0 M Samples/Sec
- Array MTF: In accordance with "Model" Figure 9 within 0.1 - 6.0 M Sample/Sec readout rate
- RMS Noise (excluding dark signal associated noise): 150 electrons/pixel readout when operated between 0.1 - 6.0 M Samples/Sec.

PRELIMINARY SYSTEM ANALYSIS

The requirement for 6"/l.p. ground resolution demands a lens focal length of at least

$$f = \frac{0.0007}{3.00} \times 3000 \times 12 = 8.4 \text{ inches}$$

In order to set the required 6"/l.p. resolution module at 0.84 of the Nyquist limit, a 10" e.f.l. lens is selected.

The $\pm 20^{\circ}$ field of view represents a line 7.28 inches long in the focal plane. This requires 7 sensor chips (each with a 1.05" long sensor area). A seven-channel system is therefore tentatively hypothesized.

At the V/H of 0.15 knots/foot and the altitude of 3000 feet, the vehicle velocity V is seen to be 9120 inches per second from which the image velocity using the 10" e.f.l. objective lens calculates to be 2.53 inches per second. $V = 2.53$.

If each channel is read out once per line progression in the image, the readout rate is

$$RR = 1500 \frac{2.53}{0.0007} = 5.42 \times 10^6 \text{ Samples/Sec and}$$

$$t = 2.76 \times 10^{-4} \text{ Sec.}$$

This falls within the optimum operational range of our hypothetical sensor chip.

At a "sunlight" illumination of 100 foot candles, the scene irradiance may be seen to be (from figure 2) 1.15×10^{-3} watts/cm² at $T = 6000^{\circ}\text{K}$. $I \cdot P = 1.15 \times 10^{-3}$.

The responsivity of our sensor (from figure 8) is 0.158 amps/watt at that color temperature. $\rho = 0.158$.

A preliminary calculation of a value for "Q" assuming a (T#) = $\sqrt{20}$ lens yields:

$$Q = \frac{(6.24 \times 10^{18})(0.158)(1.15 \times 10^{-3})(2.76 \times 10^{-4})(3.16 \times 10^{-6})(7)}{80}$$

where $\sigma = \frac{5}{(0.84)^2} = 7$ because the aspect ratio of the USAF tri-bar target is 5:1, and the required limiting resolution is at 0.84 of the Nyquist limit.

$$Q = 8.65 \times 10^4 \text{ electrons}$$

Calculation of the dark signal yields:

$$\text{Dark Signal} = 50 \frac{2.76 \times 10^{-4}}{10^{-6}} = 1.38 \times 10^4$$

from which the noise in the dark signal is 117 electrons RMS.

If the occasional dark signal noise spike from areas of dark signal non-uniformity is ignored, the RMS noise may be computed to be (exclusive of quantum noise in signal)

$$\beta = \sqrt{117^2 + 150^2} = 190 \text{ electrons}$$

The system resolution corresponding to 6"/lp on the ground is 600 lp/inch or 23.6 lp/mm at the 10 inch (254 mm) focal length selected. At that spatial frequency a specially designed F/4 ($T = \sqrt{20}$) lens should be capable of exhibiting a minimum MTF of 60 per cent throughout the field of view. $m_{\text{optics}} = 0.60$

The MTF of the sensor is taken from Figure 9 for the 0.84 FNL point to be $m_{\text{array}} = 0.58$.

Since the sensor chip will be read out each 2.76×10^{-4} sec, m_{motion} may be computed from:

$$m_{\text{motion}} = \frac{\sin(\pi VRt)}{(\pi VRt)}$$

$$m_{\text{motion}} = \frac{\sin[\pi(2.53)(600)(2.76 \times 10^{-4})]}{\pi(2.53)(600)(2.76 \times 10^{-4})}$$

$$m_{\text{motion}} = 0.74$$

$$M = (0.60)(0.58)(0.74) = 0.26$$

Since the average scene reflectivity is 0.3 and the Contrast Ratio is 2:1 (minimum),

$$\frac{R_{\max} + R_{\min}}{2} = 0.3, \quad \frac{R_{\max}}{R_{\min}} = 2$$

$$\frac{2R_{\min} + R_{\max}}{2} = 0.3 \quad \frac{3R_{\min}}{2} = 0.3$$

$$R_{\min} = 0.2, \quad R_{\max} = 0.4$$

$$(S/N) = \frac{(8.65 \times 10^4)(0.2)(0.26)}{\sqrt{(8.65 \times 10^4)(0.6) + 7(190)^2}}$$

$$(S/N) = 8.1$$

Since a 4:1 (S/N) ratio is the minimal acceptable for "resolution", the system as outlined passes the first hurdle of parametric viability.

In the interests of brevity, the analysis has been kept to a rudimentary parametric form. The exercise, however, does serve to illustrate how the techniques outlined here may be applied.

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**PERFORMANCE ANALYSIS OF EBS-CCD IMAGING TUBES/STATUS OF ICCD
DEVELOPMENT***

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ABSTRACT. The low-light-level imaging performance of different EBS-CCD tubes are analytically compared, along with that predicted for direct-view CCD imagers, using the psychophysical model of Rosell and Willson. Because its primary photosurface is silicon, the quantum efficiency of the direct-view CCD is higher than that of the EBS-CCD. However, since there is no gain prior to CCD readout, the noise-equivalent signal is considerably higher for the direct-view CCD, even when it is assumed that the noise is dominated by amplifier noise of a few tens of electrons per packet. For this assumption to be valid, the CCD must be cooled below room temperature in some fashion. Thus, in comparison with other forms of low-light-level image sensors, the EBS-CCD tube appears to offer significant advantages in terms of size, sensitivity, and temperature of operation. The second part of this paper briefly outlines the primary objectives of the current intensified CCD programs being pursued jointly by Texas Instruments and the ITT Electro-Optical Products Division. A discussion is given of the compatibility problems associated with subjecting a CCD array to the effects of vacuum tube processing. The two CCD tube designs being developed are described, and results are presented based on current data available.

**I. PERFORMANCE ANALYSIS OF EBS-CCD
IMAGING TUBES**

A. PSYCHOPHYSICAL MODEL

The psychophysical model used in the analysis of low-light level television (LLLT) imager performance presented in this paper is based on the model developed by Rosell and Willson¹ for conventional imaging tubes. Through an extensive series of psychophysical experiments with observers watching TV displays of selected imagery, these two researchers have verified that the limiting resolution to which an observer can perceive a bar pattern is proportional to the display signal-to-noise ratio, over a wide range of conditions. Rosell and Willson define the display signal-to-noise ratio ρ_D , for imaging a dark and light bar pattern as follows:

$$\rho_D(f) = \frac{R_t^{\text{SF}}(f) C_M 2 N_{av}}{B \left[(N_{av} + N_{ns})^{1/2} \right]}, \quad (1)$$

where $R_t^{\text{SF}}(f)$ = total square-wave flux response of the system at the bar pattern spatial frequency, f ,

$$= \frac{8}{\pi^2} \left| \sum_{n=1,3,5,\dots} \frac{1}{n^2} R_t(nf) \right|;$$

$R_t(f)$ = total modulation transfer function (MTF) of the system at spatial frequency, f ;

C_M = modulation contrast of the bar pattern focused onto the sensor

$$= \frac{H_{\max} - H_{\min}}{H_{\max} + H_{\min}};$$

H_{\max} = maximum sensor irradiance;

H_{\min} = minimum sensor irradiance;

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N_{av} = average number of signal photoelectrons actually generated within the image of a bar during τ_{eye} , averaged over a bar pair, where τ_{eye} is the integration time of the eye (Rosell and Willson use 0.1 second for τ_{eye})

= N_{np}^2 , where N_{np} is the rms noise on the Poisson process of generating photoelectrons at the primary photosurface (photon noise);

N_{ns} = equivalent rms number of noise electrons per bar added to the video signal by other noise sources in the system; and

B = operator which represents noise reduction by system MTF effects.

With this definition of p_D , Rosell and Willson have shown that a bar pattern imaged by a sensor can just be resolved by an observer viewing the output of the sensor on a display when p_D for that pattern and sensor combination is equal to about 2.5. The observer is allowed to optimally adjust the display contrast and brightness and his own viewing distance. This threshold value, p_{th} , for p_D is not absolutely constant, but varies somewhat as the bar length-to-width ratio, r_{LW} , is changed, with a somewhat larger value of p_{th} required for larger values of r_{LW} ($\leq 25\%$ increase as r_{LW} is varied from 5 to 20). p_{th} also depends on f , the spatial frequency of the pattern, being slightly smaller for the higher frequencies ($\approx 25\%$ decrease as f varies from 100 to 500 TV lines per picture height, for $r_{LW} = 5$). In the present treatment, the somewhat conservative value of 3.0 has been used for p_{th} throughout, regardless of the values of r_{LW} and f .

There are noise sources in a CCD that insert a fixed system noise component into each picture element once each frame, or once each field in the case of interlaced operation. An example of this type of noise is the preset noise introduced at the CCD output by a simple precharge amplifier. The time averaged value of this noise, averaged over τ_{eye} , thus depends on the frame rate. For the CCD, therefore, it is preferable to redefine N_{av} and N_{ns} as averages over τ_f , a single frame time, or field time for interlaced mode, and to account for the eye's integration time through a separate factor,

$$\sqrt{\tau_{eye}/\tau_f} .$$

Equation (1) then becomes:

$$p_D(f) = \frac{R_t^{SF}(f) C_M 2 N_{av} \sqrt{\tau_{eye}/\tau_f}}{B \left[(N_{av} + N_{ns}^2)^{1/2} \right]} . \quad (2)$$

This use of the eye integration factor is justified only if the noise is uncorrelated from one frame to the next, but this will, in general, be true. The only exception is so-called "fixed pattern noise," resulting from fixed spatial variations in the sensor background level or responsivity. The amplitudes of these variations add directly, rather than in quadrature. If N_{nf} is the equivalent rms number of fixed pattern noise electrons per bar image, averaged over a bar pair and integrated over τ_f , the appropriate modification of Equation (2) to include fixed pattern noise is

$$p_D(f) = \frac{R_t^{SF}(f) C_M 2 N_{av}}{B \left\{ [(N_{av} + N_{ns}^2)(\tau_f/\tau_{eye}) + N_{nf}^2]^{1/2} \right\}} . \quad (3)$$

This treatment of fixed pattern noise represents an extension beyond the work of Rosell and Willson, and is consequently somewhat speculative. For this reason, fixed pattern noise is ignored in most of the computer predictions of limiting resolution presented here. However, the arguments seem plausible enough to justify a plot that includes an estimate of fixed pattern noise.

In applying the results of Rosell and Willson to CCD's, it is more convenient to express the signal and noise in terms of electrons per picture element, or pixel, rather than per bar. If we assume for the moment that system MTF effects are negligible and that all noise sources are white, we can write Equation (3) as

$$p_D(f) = \frac{R_t^{SF}(f) C_M 2 mn N'_{av}}{\left\{ (N'_{av} mn + N_{ns}^2 mn) (\tau_f/\tau_{eye}) + N_{nf}^2 mn \right\}^{1/2}}$$

$$= \frac{2 R_t^{SF}(f) C_M N'_{av}}{\left\{ [(N'_{av} + N_{ns}^2)(\tau_f/\tau_{eye}) + N_{nf}^2]/mn \right\}^{1/2}}, \quad (4)$$

where N'_{av} = average number of signal photoelectrons collected per pixel during τ_f , averaged over a bar pair;

N'_{ns} = equivalent rms number of system noise electrons per pixel per frame (or field), averaged over a bar pair;

N'_{nf} = equivalent rms number of fixed pattern noise electrons per pixel per frame (or field), averaged over a bar pair;

m = number of pixels per bar height; and
 n = number of pixels per bar width.

The reduction in noise power by the divisor, mn , may be interpreted as bandlimiting by the eye as it integrates over a bar. Elaborating on this interpretation, we set

$s_p(f_x, f_y)$ = spectral density of average photon noise per pixel,

$s_s(f_x, f_y)$ = spectral density of system noise per pixel, and

$s_f(f_x, f_y)$ = spectral density of fixed pattern noise per pixel, where f_x, f_y are frequencies in the two-dimensional transform space of the two-dimensional sensor surface.

$$\text{Then } \frac{N'_{av} + N'^2 \left(\frac{\tau_f}{\tau_{eye}} \right) + N'^2_{nf}}{mn}$$

$$= \int_0^{f_{Nx}/n} df_x \int_0^{f_{Ny}/m} df_y \left\{ [s_p(f_x, f_y) + s_s(f_x, f_y)] \right. \\ \left. \times (\tau_f / \tau_{eye}) + s_f(f_x, f_y) \right\}, \quad (5)$$

where f_{Nx} = Nyquist frequency in the x -direction,

f_{Ny} = Nyquist frequency in the y -direction.

Substituting Equation (5) into Equation (4) yields

$$\rho_D(f) = \frac{2 R_t^{\text{SF}}(f) C_m N'_{av}}{\left(\int_0^{f_{Nx}/n} df_x \int_0^{f_{Ny}/m} df_y \left\{ [s_p(f_x, f_y) + s_s(f_x, f_y)] \left(\frac{\tau_f}{\tau_{eye}} \right) + s_f(f_x, f_y) \right\} \right)^{1/2}} \quad (6)$$

If the spectral densities in Equation (6) are interpreted as representing noise referred to the CCD output channel, then this expression for ρ_D is general enough to

include non-white noise sources and sub-unity MTF's.

The bandlimiting of noise spectral density is explicitly represented in Equation (6) by the integration limits in the denominator, with a maximum noise bandwidth equal to the maximum signal bandwidth (Nyquist frequency). The divisors, n and m , are functions of f , through the relationships:

$$\begin{aligned} \text{Vertical Bars} \quad & \left\{ \begin{array}{l} n = f_{Nx}/f, \\ m = nr_{LW}, \end{array} \right. \\ \text{Horizontal Bars} \quad & \left\{ \begin{array}{l} m = f_{Ny}/f, \\ n = mr_{LW}. \end{array} \right. \end{aligned}$$

In the graphical presentation of computational results that follow, the spatial frequencies are expressed in TV lines per picture height (TVL/PH). The presentation in terms of TVL/PH is consistent with Rosell and Willson's graphical format and is of more direct utility to the display observer than a presentation in terms of line pairs per millimeter ($\ell p/mm$), since it includes information concerning sensor size in addition to sensor resolution density.

In order to use Equation (6) to compute ρ_D , expressions were developed for $R_t^{\text{SF}}(f)$, $s_p(f_x, f_y)$ and $s_s(f_x, f_y)$ in terms of predictable system parameters. For the present computations, the MTF factors that were used to calculate $R_t^{\text{SF}}(f)$ were the following:

- (1) Diffusion MTF;
- (2) Secondary generation MTF (for EBS-CCD only);
- (3) Pixel collection MTF;
- (4) Charge transfer MTF;
- (5) Lens MTF;
- (6) Tube pretarget MTF (for EBS-CCD only).

The noise components that were considered in calculating $s_s(f_x, f_y)$ were the following: (1) Dark current noise, and (2) Amplifier noise.

fat zero input noise and fast interface state noise were not included, as the sensors were assumed to be buried channel. Bulk state trapping noise was not included, as measurement data on this noise source are somewhat sparse. The expressions developed for these various MTF's and noise spectral densities are too detailed to be presented here, but are contained in a report to NVL.²

B. COMPUTER PREDICTIONS OF LIMITING RESOLUTION

Five different types of CCD imagers were analyzed by computer using the display signal-to-noise ratio model described in the preceding section to predict limiting resolution versus illumination level. More precisely, five different applications of the same CCD array in image sensor configurations were analyzed:

- (1) Direct-view CCD sensor, cooled to $T = 210\text{ K}$, with responsivity of 90 mA/W for 2854 K illumination = 5.6 mA/lm ;
- (2) Proximity-focused EBS-CCD tube, operating at $T = 300\text{ K}$, with S-20 extended red response photocathode (responsivity of 7 mA/W for 2854 K illumination = $440\text{ }\mu\text{A/lm}$);
- (3) Proximity-focused EBS-CCD tube, at $T = 300\text{ K}$, with GaAs photocathode (responsivity of 6.4 mA/W for 2854 K illumination = $390\text{ }\mu\text{A/lm}$);
- (4) EBS-CCD inverter tube, at $T = 300\text{ K}$, with 25 mm S-20 extended red response photocathode;
- (5) EBS-CCD inverter tube, at $T = 300\text{ K}$, with 25 mm GaAs photocathode.

The CCD array assumed for each of these applications is a thinned, rear-illuminated (or bombarded), 500×500 -element CCD with a 3:4 aspect ratio, operated in the frame transfer mode with 2:1 interlace (resulting in a possible 500 displayed TV lines). The pixel dimensions are assumed to be 0.9 mil by 1.35 mil, resulting in an active sensor diagonal of 14.3 mm.

These five configurations are compared in a series of plots of limiting resolution, evaluated at the center of the active sensor, versus average sensor irradiance in Figures 1 through 5, where each plot represents a different set of operating conditions. The

first case analyzed is the photon-noise-limited resolution of 50% contrast vertical bars, where all system noise and MTF effects are removed. The bar length-to-width ratio is 5:1. Because of the 3:4 aspect ratio of the sensor area, the Nyquist limit for vertical bars is 375 TV lines per picture height. The direct-view silicon sensor, with the high quantum efficiency of silicon, is the most sensitive sensor in the absence of system noise.

Case 2, shown in Figure 2, is again for 50% contrast vertical bars, but now includes system noise and MTF effects. RMS amplifier noise for the direct-view sensor is assumed to be 30 electrons per packet, while that for the EBS-CCD imagers is assumed to be 150 electrons. The EBS gain used is 2000, which is typically obtained in SIT tubes with V_{acc} of 10 keV. The proximity tube photocathode-to-target separation is 20 mils which is probably a lower limit for this parameter. No fixed pattern noise is included in this case. A detailed list of all other model parameter values used is given at the end of this section.

The EBS-CCD sensors outperform the direct-view CCD sensor at sensor irradiance levels below $6 \times 10^{-6}\text{ W/m}^2$. Above this irradiance level, performance is roughly comparable for all sensors. The average sensor irradiance at which sensor-limiting resolution drops to 100 TVL/PH is about a factor of eight darker for the proximity tubes than for the direct-view CCD, and about a factor of 25 darker for the inverter tubes than for the direct-view CCD.

Case 3, shown in Figure 3, is a variation on Case 2 in which the gain of the EBS-CCD tubes has been reduced to 1000. The overall relationship of the curves to one another has not changed appreciably. The 100 TVL/PH limiting resolution point still occurs at a sensor irradiance level about a factor of 7 darker for the proximity tubes than for the direct-view CCD, and about a factor of 20 darker for the inverter tubes than for the direct-view CCD.

Case 4, shown in Figure 4, is another variation of Case 2, this one having fixed pattern noise included. The rms fixed pattern noise is assumed to be 30 electrons per pixel per field for the direct-view CCD, and 1000 electrons for the EBS-CCD tubes. All the curves have moved to higher irradiance

levels, but the EBS-CCD sensors still outperform the direct-view CCD. The 100 TVL/PH limiting resolution point occurs at an irradiance level about a factor of four times darker for the proximity tubes than for the direct-view CCD, and about 13 times darker for the inverter tubes than for the direct-view CCD.

Case 5, shown in Figure 5, is yet another variation on Case 2, in which the photocathode-to-target separation for the two proximity-focused tubes is increased to 50 mils. The curve for the GaAs proximity tube is essentially unchanged by this increase, while the curve for the S-20 proximity tube has dropped a little at the higher spatial frequencies. The reason for the different results is the wider angular distribution and higher emission energy for electrons emitted from the S-20 photocathode. Even for the S-20 proximity tube, however, the change is small, particularly at the lower light levels.

We now list the model parameter values not already given that have been used in the preceding analyses.

$\tau_f = 16 \text{ msec}$ (sensor field time)
 $\tau_{\text{eye}} = 0.1 \text{ sec}$ (eye integration time)
 $\alpha = 350 \text{ cm}^{-1}$ (effective silicon optical absorption coefficient)
 $R = 0.3$ (effective silicon optical reflectivity)
 $S = 1000 \text{ cm/sec}$ (surface recombination velocity)
 $D = 35 \text{ cm}^2/\text{sec}$ (minority carrier diffusion coefficient)
 $\tau = 100 \mu\text{sec}$ (minority carrier lifetime)
 $L_n = 6 \mu\text{m}$ (thickness of neutral bulk layer)
 $L_s = 10 \mu\text{m}$ (total thickness of CCD substrate)
 $n_\phi = 3$ (number of phases)
 $\epsilon_x = 10^{-5}$ (loss per transfer in output serial register)
 $\epsilon_y = 10^{-5}$ (loss per transfer in sensor and storage registers)
 $J_D = 10 \text{ nA/cm}^2$ (dark current density in CCD at $T = 300 \text{ K}$)
 $f_c = 7.8 \text{ MHz}$ (output pixel clocking rate)
 $f_{co} = 150 \text{ lp/mm}$ (lens cutoff frequency)

$m_{pt} = 0.57$ (photocathode-to-target minification for inverter tube)

$f_o = 35 \text{ lp/mm}$ (one-sigma frequency for Gaussian pretarget MTF of inverter tubes)

$V_{\text{acc}} = 10^4 \text{ V}$ (accelerating voltage for proximity tubes)

$E_e = \begin{cases} 0.5 \text{ eV}, & \text{for S-20 photocathodes, and} \\ 0.026 \text{ eV}, & \text{for GaAs photocathode,} \\ & \text{(typical photoelectron emission} \\ & \text{energies for proximity tubes)} \end{cases}$

$\theta_e = \begin{cases} 30^\circ, & \text{for S-20 photocathode, and} \\ 7^\circ, & \text{for GaAs photocathode,} \\ & \text{(typical} \\ & \text{photoelectron emission angles for} \\ & \text{proximity tubes).} \end{cases}$

C. SUMMARY

The low-light-level imaging performance of different EBS-CCD tubes has been analytically compared, along with that predicted for direct-view CCD imagers. Because its primary photosurface is silicon, the quantum efficiency of the direct-view CCD is higher than that of the EBS-CCD. However, since there is no gain prior to CCD readout, the noise-equivalent signal, referred to the CCD output, is considerably higher for the direct-view CCD, even when it is assumed that the noise is dominated by amplifier noise of a few tens of electrons per packet. For this assumption to be valid, the CCD must be cooled below room temperature in some fashion. Thus, in comparison with other forms of low-light-level image sensors, the EBS-CCD tube appears to offer significant advantages in terms of size, sensitivity, and temperature of operation.

II. STATUS OF ICCD DEVELOPMENT

A. INTRODUCTION

The development of charge coupled devices has had a major impact on all of the semiconductor industry. The self-scanning and direct read-out capabilities of these arrays eliminate the requirement of storage targets and read-out guns used in conventional camera tubes. The use of a CCD array incorporated into a vacuum tube envelope for operation in the electron bombarded mode utilizing a photocathode as the electron source will permit the advent of miniaturized

rugged, compact and simplified camera tubes and a new class of video processing devices for military and commercial applications.

The EOPD Tube and Sensor Laboratories at Fort Wayne, Texas Instruments, the Night Vision Laboratories at Fort Belvoir, and the NASA Goddard Space Center in Greenbelt have been working on the development of CCD devices for camera tube applications. Current development programs being carried out include the following.

- The development of a proximity focused diode tube incorporating a TI CCD array for operation in the electron bombarded mode.
- The development of a magnetically focused tube incorporating a TI CCD array for operation in the EB mode.

In addition, a general development program has been initiated within ITT to design and develop the necessary equipment to permit the monitoring of CCD electrical characteristics as a function of exposure to tube processing parameters and provide the means for the test and evaluation of the vacuum tubes being developed.

The following sections will briefly outline the primary objectives of the current programs, discuss the compatibility problems associated with subjecting a CCD array to the effects of vacuum tube processing, describe the two CCD tube designs being developed, and present results based on current data available.

B. PROGRAM OBJECTIVES

The primary objective of the current programs is to provide operational vacuum devices that will permit the test and evaluation of the performance characteristics of a charge coupled device, CCD, that is mounted in a vacuum tube envelope and operated in the electron bombarded mode. Two tube types are being developed, a proximity focused diode and a magnetically focused tube. Both tube types incorporate a TI 100 x 160 CCD array that has been mounted on a specially designed output flange.

The determination of the compatibility problems associated with subjecting a CCD array to the effects of vacuum tube processing as required for the development of CCD

camera tubes is of prime importance. Specific compatibility problems under investigation include the following.

- The determination of the ability to incorporate a CCD header assembly into a vacuum tube envelope using standard heliarc welding procedures.
- Determination of the effects of vacuum baking during tube processing on the vacuum integrity of the CCD header assembly.
- Evaluation of the effects of vacuum baking on CCD electrical characteristics such as dark current and transfer efficiency.
- Evaluation of the effects of exposing the CCD array to alkali vapors required for photocathode formation.
- Determination of the performance characteristics of a CCD array operated in the electron bombarded mode.

C. PROXIMITY AND MAGNETIC FOCUS CCD TUBE DESIGNS

Both the proximity focused and the magnetic CCD tubes being developed consist of an all-metal-ceramic tube envelope, an output CCD header assembly, and magnesium fluoride input window. Both tubes are fabricated using ITT remote processing techniques wherein the photocathode is formed on the input window while physically isolated from the tube envelope in the vacuum forming chamber. Present contracts call for the use of a bialkali KCsSb cathode. After cathode formation, the input faceplate is transferred and indium sealed to the tube body. Both tube types use the same TI CCD header assembly, mounted on an ITT output flange. The CCD header assembly is shown in Figure 6.

An outline drawing of the ITT proximity ceramic envelope, the heliarc welded CCD header assembly and the re-entrant magnesium fluoride input window. The overall tube length is .60 inches. The tube has been designed to permit operation with 10-15 KV applied between the photocathode and the CCD array. The re-entrant cathode faceplate can be modified to accommodate changes in spacing required to achieve optimum resolution, consistent with acceptable field gradients and input energy levels required for optimum performance of the CCD array.

The magnetic tube design is shown in Figure 8. It consists of a brazed ceramic-metal stack that is 1.70 inches in diameter and approximately 3.6 inches in length. The tube utilizes the same TI CCD header assembly that is heliarc welded into the output section. A gating mesh has been included and an indium sealed plano-plano magnesium fluoride input window completes the basic tube assembly. The tube is designed to operate at 20 KV and requires a 200 gauss magnetic field for first loop focus. The limiting resolution of the tube electron optics is in excess of one hundred line pairs per mm, exclusive of the CCD array characteristics.

An output photo of a potted ITT CCD diode is shown as Figure 9.

D. RESULTS TO DATE

To date, only tubes of the proximity focused design have been processed, using available CCD header assemblies. It is expected that CCD header assemblies will be available in the near future to permit fabrication of the magnetic tubes.

Three TI CCD header assemblies were heliarc welded into ITT diode assemblies. The tubes were subjected to a 325°C vacuum bake, cathodes were remotely processed, transferred and sealed to the tube envelopes. All three tubes were shipped to NVL for test and evaluation. All tubes had TI arrays of the 100 x 160 buried channel design, mounted on a 33-pin header assembly and providing an active area of .08 cm² with a pixel dimension of 0.9 x 0.9 mils. All three tubes were checked for cathode stability for a minimum period of three weeks prior to shipment. No measurable change in cathode sensitivities was detected.

The first tube was operated in the EB mode at the NASA Goddard Space Center with the following preliminary results reported.

- The tube was operated with 12.5 KV applied between cathode and the CCD array.
- The array dark current from the active area was measured at 9 na, relative to an original measurement of 5.2 na measured prior to tube processing. This indicates less than a factor of

two change in the total CCD dark current after being subjected to all tube processing parameters.

- An output resolution of 4 to 8 line pairs/mm was observed. Maximum resolution capability was not established. (The photocathode to CCD separation of .27 in. used would limit resolution to approximately 8 lp/mm.)
- Comparison of the output image quality with the CCD array operated in the EB mode to the image obtained with the array operated in the photoemissive mode showed no essential difference, with the exception of a somewhat higher granular appearance of the EB output.

It should be noted that the first tube processed and described above did not contain a re-entrant cathode faceplate, and therefore, did not provide optimum cathode to CCD array spacing. The array dark current on the second and third tubes delivered indicated an increase by a factor of three and ten relative to original measurements prior to processing. In addition, preliminary tests on these two tubes have indicated the presence of an inoperable sector within the 100 x 160 CCD arrays. The nature and cause of these conditions is currently under further investigation.

Although the above data is preliminary, and indeed limited in detail and scope, it does permit the following observations to be made.

- TI CCD header assemblies can and have been subjected to heliarc welding, vacuum bake, and tube processing cycles without loss of vacuum integrity.
- Tube processing and cathode formation had no known adverse effects on the electrical characteristics of the CCD array. Dark current on the first array remained within a factor of two of original levels.
- Output imagery has been achieved from a TI CCD array sealed into a miniaturized ITT diode structure and operated in the electron bombarded mode.

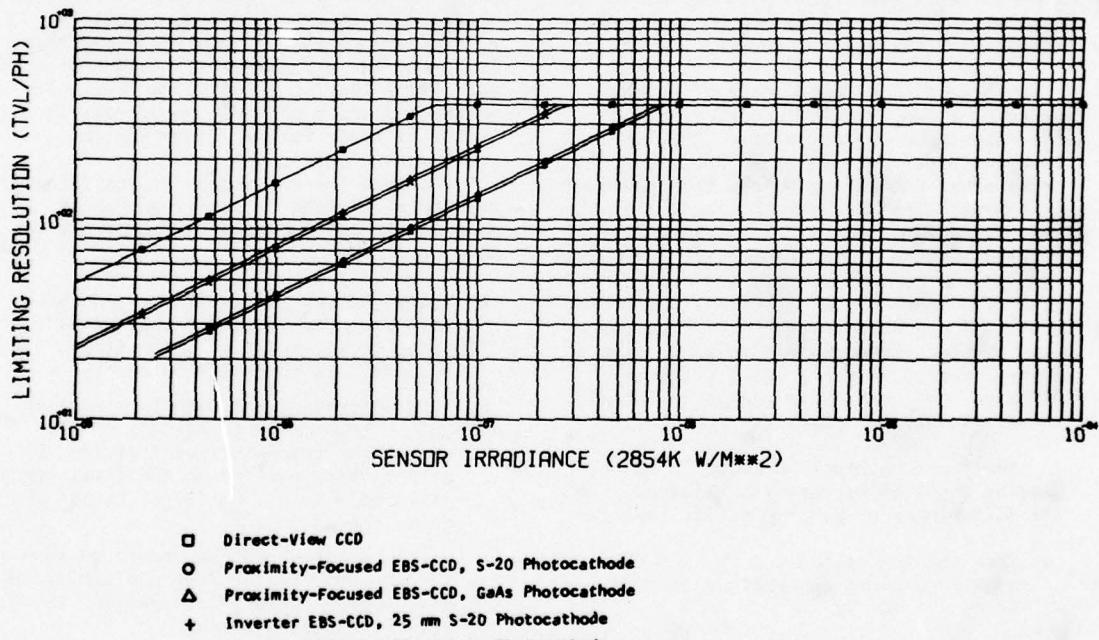
Additional data and information will become available as programs similar to those discussed herein proceed beyond their first year of implementation.

ACKNOWLEDGEMENTS

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Case 1. Photon-Noise-Limited Resolution of 500 x 500 Imagers; No MTF Effects Included; Vertical Bars in Test Pattern

FIGURE 1

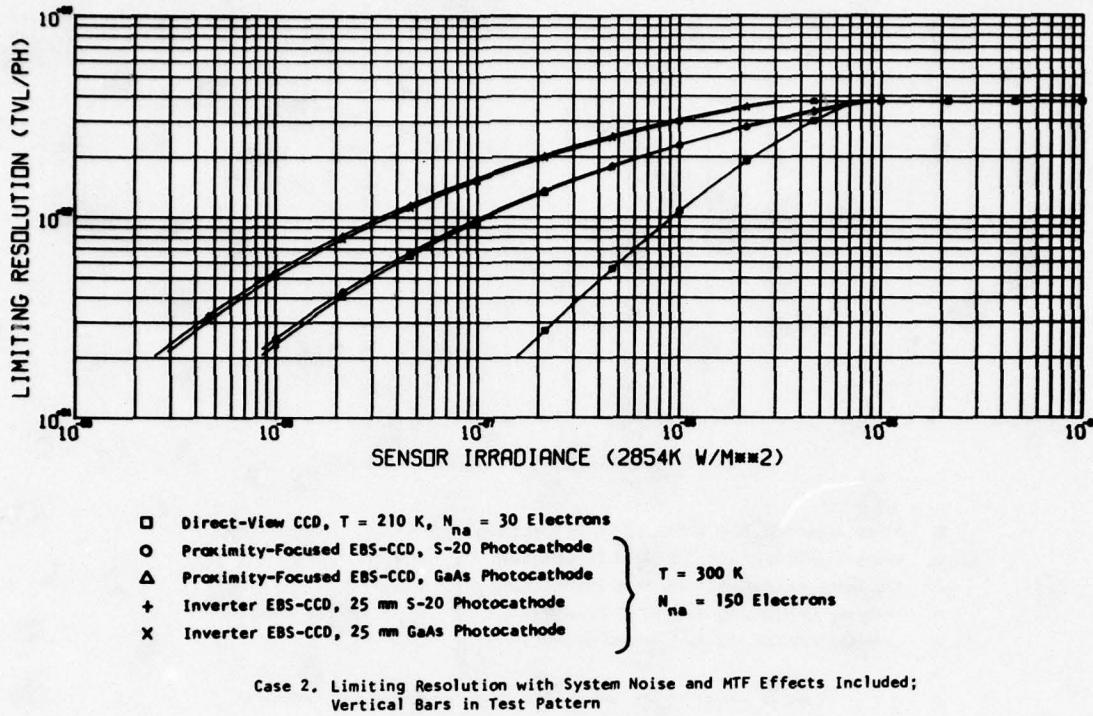


FIGURE 2

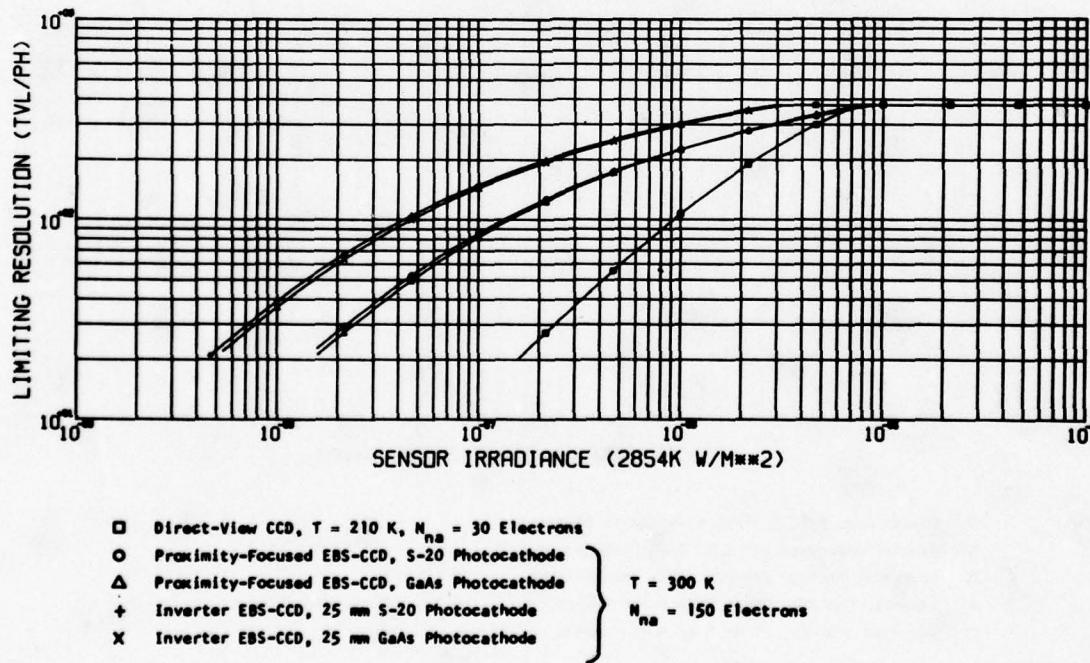
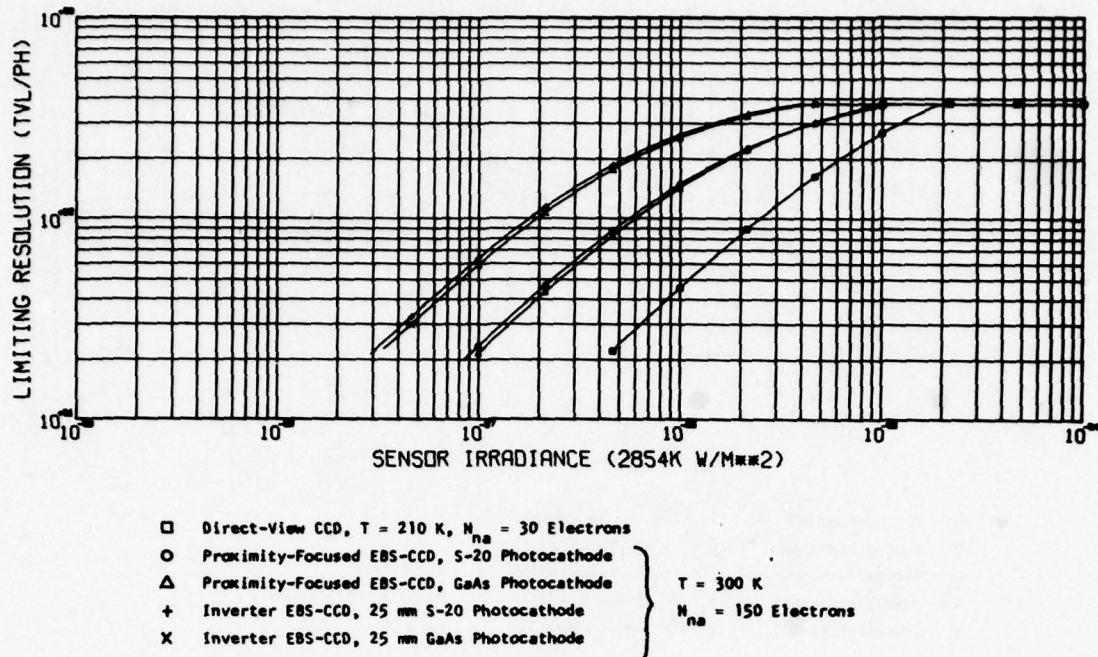
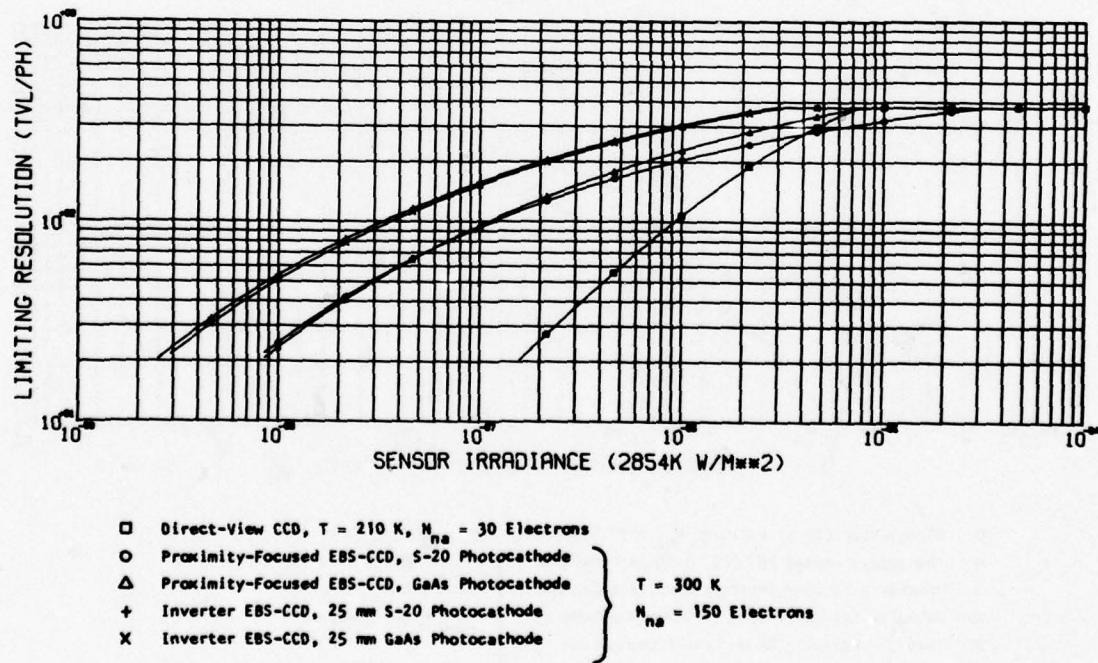


FIGURE 3



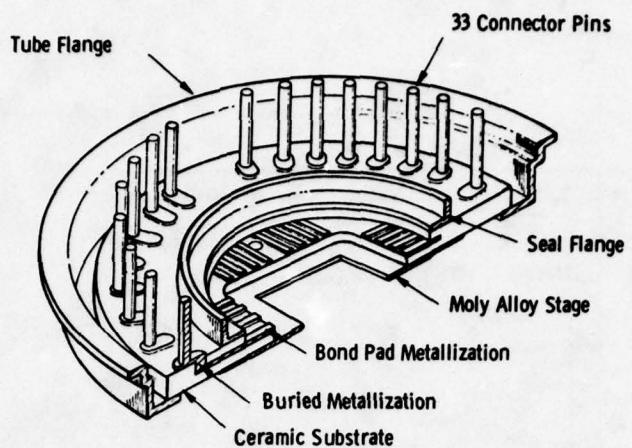
Case 4. Variation on Case 2, with Fixed Pattern Noise Included

FIGURE 4



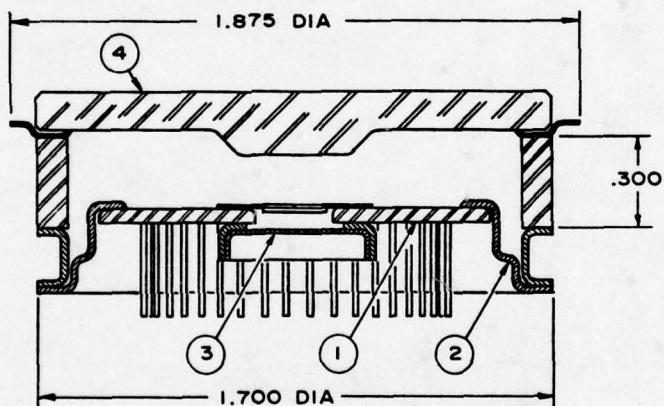
Case 5. Variation on Case 2, with Proximity Tube Photocathode-to-Target Separation Increased to 50 Mils

FIGURE 5



TI CCD Header Assembly

FIGURE 6

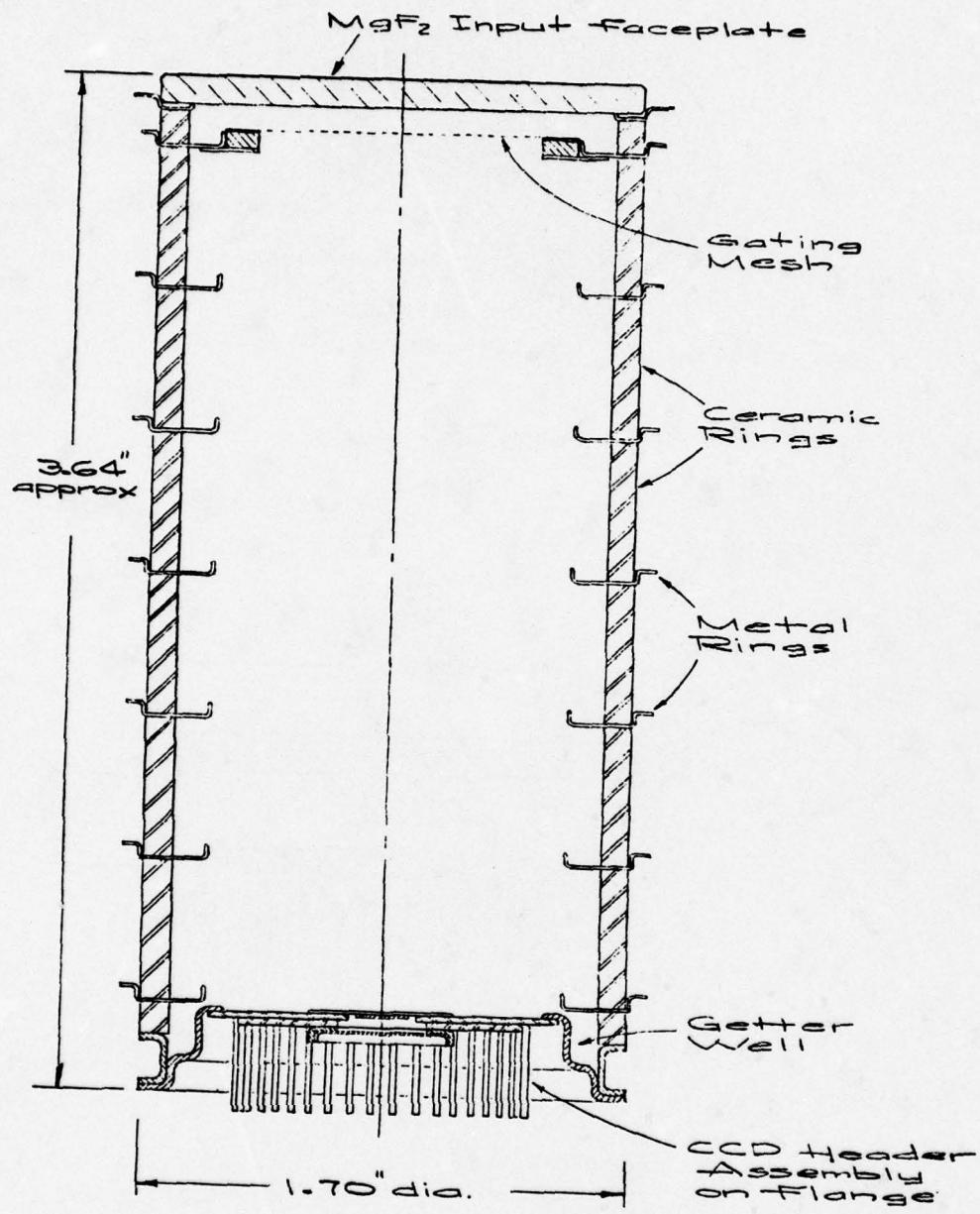


ALL DIMENSIONS ARE IN INCHES

- (1) CCD-HEADER
- (2) MOUNTING FLANGE FOR CCD HEADER
- (3) NIROMET CAP
- (4) MAGNESIUM FLUORIDE OR DYNASIL UV1000
FUSED SILICA INPUT WINDOW

ITT Proximity Focused CCD Diode

FIGURE 7



Magnetic Focus ICCD

FIGURE 8

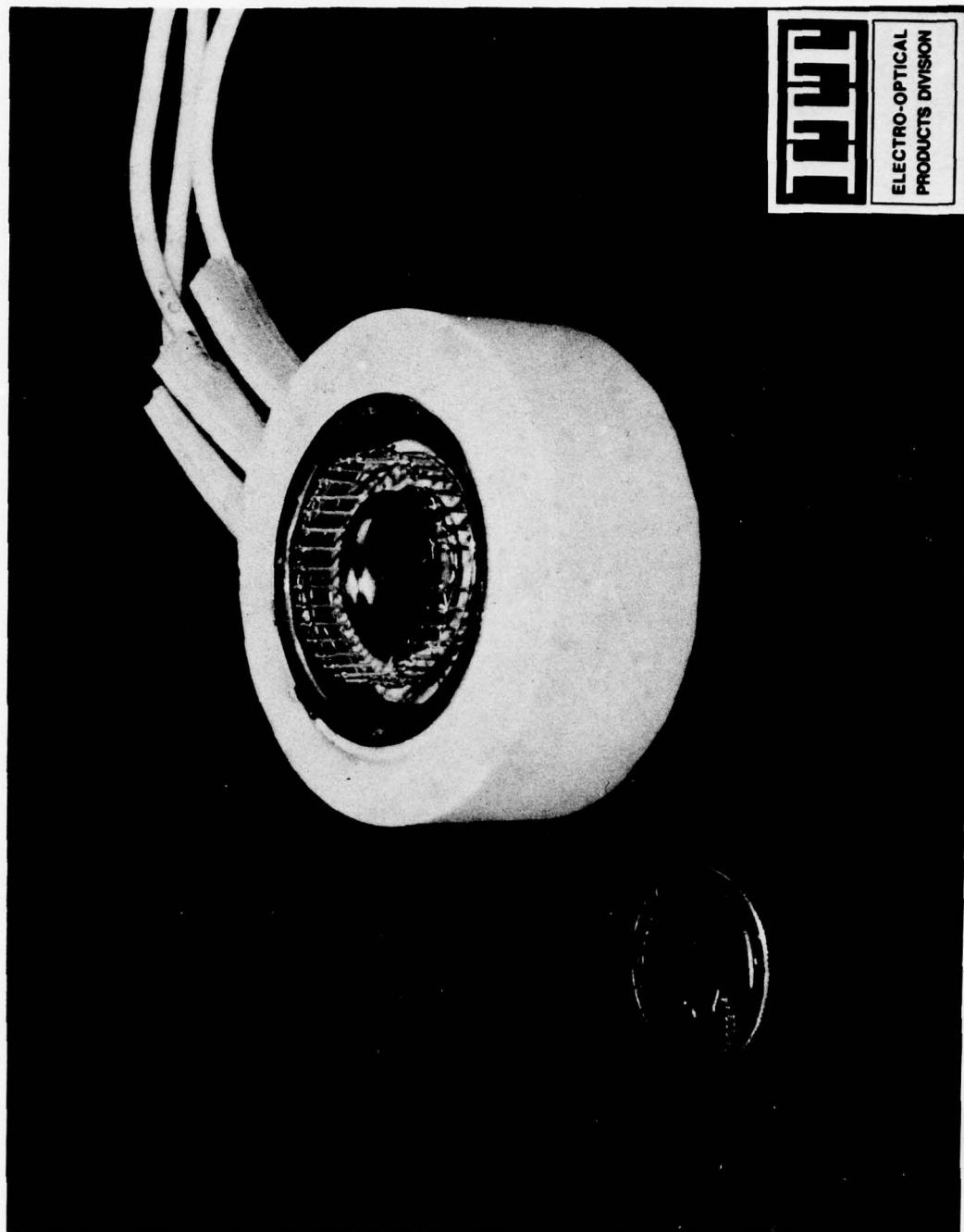


FIGURE 9. Potted CCD Diode

DEVELOPMENT OF A 400 x 400 ELEMENT, BACKSIDE ILLUMINATED CCD IMAGER*

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ABSTRACT. Thinned, backside illuminated CCD imagers with 400 x 400 resolution elements have been fabricated using a double level anodized aluminum electrode system. These imagers have been developed for application to deep space photography where array read out rates of about 10 kHz and operating temperature near -40°C are envisioned. The performance of the 400 x 400 will be discussed and comparisons made to the operating parameters of a smaller 160 x 100 array fabricated with the same technology.

INTRODUCTION

Several CCD technologies have been successfully applied to fabricate large area imaging arrays.¹⁻³ Illumination may be incident on the front, or electrode side of the array, but interference and absorption in either polysilicon or metal oxide electrodes can limit performance. Backside illumination, where radiation is focused on the planar back surface remote from the CCD electrodes, gives uniform and high spectral responsivity. Backside illumination⁴⁻⁷ requires however that the CCD be thinned to about 10 µm to provide high resolution.

Large area CCD arrays are being considered for application in deep space photography where the requirements are such that the imager should operate at low data rates (~ 10 kHz) which requires device cooling (~ -40°C) to reduce thermally generated dark current during the long read out sequence. In this application the self-scanned CCD may replace the conventional electron beam scanned vidicon. However, the processing complexity of the CCD as compared to the vidicon presents formidable problems in obtaining high quality, defect free devices which are greater in area than present commercial MOS integrated circuits.

This paper describes the development at Texas Instruments of a three phase 400 x 400 thinned, backside illuminated CCD array. Double level anodized aluminum technology

is utilized. The performance of a 160 x 100 array was discussed recently,⁶ and in this paper we extend this discussion to the 400 x 400 imager. Both arrays have essentially the same serial-parallel-serial organization. Some of the processing details of particular concern with large arrays will be discussed.

DESIGN AND FABRICATION

The 400 x 400 is an n-channel, three-phase (3φ) CCD, typically fabricated on 10-15 ohm-cm p-silicon. The resolution element size is 0.9 x 0.9 mil² which requires that each parallel and serial electrode be 0.3 mil in width. The channel width in the parallel section is 0.7 mil with 0.2 mil channel stop regions for an active area of 360 x 360 mil² on a 496 x 496 mil² chip of silicon. First and second level aluminum electrodes are isolated by about 2500 Å of Al₂O₃ formed by first level anodization. The structure is shown schematically in Figure 1 where it is apparent that a given phase occurs alternatively on first and second level electrodes. A photomicrograph of the corner of the array showing the output amplifier is shown in Figure 2. Since in the 3φ design,⁷ each level is formed at an independent step in the CCD process, integration under a single parallel phase could possibly introduce line to line variation in the video output. Oscilloscope photographs showing several video lines are shown in Figure 3. Figure 3a indicates

video resulting from integration under ϕ_1 only and Figure 3b shows video after integration under both ϕ_2 and ϕ_3 . The line pairing, which is a feature of the 3 ϕ design is completely eliminated by using two electrodes. Square wave amplitude response (SWAR) data, giving resolution performance of the imager, is more reproducible using the two electrode scheme.

The second level electrodes overlap those on the first level by 0.05 mils to give a completely sealed electrode system. This allows buried channel array operation with high charge transfer efficiency (CTE). This design leaves 0.2 mil separation between electrodes which is the minimum that can reliably be opened by conventional wet etching technique. To maintain the design overlap of 0.05 mil in both parallel and serial sections presents formidable difficulties in both optical photomask generation and slice processing. CCD processing requires nine photomask levels which must be registered with each other, although of course, some are more critical than others. Random variations inherent in the generation of the master masks, which are due to mechanical limitations, can amount to ± 0.015 mil and this can significantly affect a design overlap of 0.05 mil. The design overlap must also be maintained over many repeated arrays on the working photomasks used in processing. For processing on two inch diameter silicon slices, six to seven bars can be used while for three inch processing, 21 bars can be used.

A second factor which impacts device yield is the occurrence of random defects in the photomasks such as accidental bridging between two channel stops (nonfatal) or between two metal electrodes (fatal). Individual treatment to eliminate these defects is often necessary on the master reticle. These defects can be due to imperfections in the Si_3N_4 used for the working masks or to dust particles in related processing and individual treatment is again used in most cases to remove most of these defects. In spite of these problems, however, it has been found that the design tolerances can be maintained over sufficiently wide fields so that processing can be performed on three inch silicon slices. At the present time device performance in so far as it is effected by photolithography, does not appear to be significantly affected by location on a processed slice. Extension to larger arrays, for which

the tolerance must be maintained over larger areas will be a progressively more difficult problem.

The 400 x 400 is designed to operate in the full frame imaging mode. An upper and lower output serial register is provided to allow forward or reverse array operation which increases device yield in the event of a malfunction of one of the on-chip output amplifiers. The array is divided electrically into four independent 100 x 400 sections so that a fatal processing defect in one section does not preclude operation of a partial array. This design feature allows an increased amount of performance data from a processed lot to be obtained for evaluation purposes. All electrical inputs necessary for array operation can be brought to bond pads along two edges of the CCD chip. Thus each 400 x 400 chip can be cut with a few mils of the two remaining array edges to allow a 800 x 800 mosaic to be made with the loss of only 5-10% of the active area.

The output from the CCD is by a simple precharge amplifier with reset switch (buried channel) and source follower (generally surface channel). For generation at 10 kHz follower load, resistors of up to 50 K are possible to reduce on chip power dissipation and membrane heating while maintaining low MOSFET noise.

Bond pads are extended some 50 mils from the active array so that the edges of the thinned silicon can extend outside this area but still leave a thicker 25 mil rim for membrane support. Thinning is performed by chemical etching techniques in which either a selected chip or complete slice can be thinned. The resulting membrane surface is highly reflective and can readily be coated with an antireflection (AR)/passivating layer of SiO_2 . Although the membrane is generally somewhat nonplanar due to process-induced stress, device performance does not appear to be affected, even by repeated temperature cycling between 24°C and -40°C. A photograph of a CCD mounted in a 40 pin dual in line header is shown in Figure 4.

Buried channel operation of the array is necessary to achieve high performance at all points in the array. A 0.5 to 1.0 μm deep channel is formed by implanting phosphorus and a CTE > 0.9999 is measured in the serial register with 8-10 V clocks and no electrically introduced fat zero. Equally good CTE

In the parallel section is inferred from the square wave amplitude response (SWAR) data and is also measured by electrically injecting a pulse into the upper serial register and transferring through the parallel section to the power output amplifier.

CCD device processing generally makes use of conventional MOS techniques. p^+ channel stops and n^+ diodes are formed by boron and phosphorus diffusion, respectively. Typical gate oxide thickness for the CCD's is 1350 - 1500 Å. The buried channel is then formed by the phosphorus implant and subsequent drive in diffusion. This process is critical to obtain low dark current imagers. After first level metal patterning, the metal is protected by a layer of photoresist (vias) in certain areas which must connect to subsequent second level metal electrodes. Vias eliminate the need for less reliable n^+ diffused tunnels as a means of interconnection for the electrode structure and allows all electrodes to be brought out on the same side of the array (Figure 2). The exposed metal is anodized and interconnects which had been required for electrical continuity during anodization are removed. Second level metal is then patterned to give a completely sealed electrode system. Detailed inspection of the first level pattern after etching generally revealed undesirable accidental bridges between adjacent metal electrodes due to either resist contamination during processing or to photomask defects. These would result in intralevel shorts if not removed prior to anodization. Pinholes in the anodic oxide which isolates first and second level electrodes will result in interlevel shorts. Anodization is a self-healing process and the quality of the interlevel isolation is very high. Nevertheless, metal defects are the dominant failure mode for our CCD's. Pinholes in the gate insulator are also fatal defects and considerable effort has been made to grow high quality SiO_2 layers. Dry oxidation between 1000°C and 1100°C, with and without HCl impurity doping and steam oxidation at 950° have been investigated as well as the influence of chemical and vapor cleaning techniques on the pinhole density in the gate oxide layer. At present, the CCD gate is grown by steam oxidation and pinhole densities well below $1/\text{cm}^2$ have been achieved. The formation of pinholes appears to result from nonrandom defects or particles at the silicon surface prior to oxidation. Over the range 1000 Å to 1500 Å, the pinhole density does not

appear to depend strongly on oxide thickness.

The thermally generated array dark current in the buried channel arrays can be very low (1 nA/cm^2), provided bulk gettering processes are applied in processing. At these levels the dominant dark current contribution is generated at the surface rather than in the bulk silicon as evidenced by a weak dependence of array dark current on clock voltage. Storage times to reach full well of 15 sec at 24°C and about three hours at -40°C have been achieved with the smaller 160×100 array. The incidence of localized dark current spikes in these devices is essentially zero. Since the generation rate for these spikes does not decrease with temperature as does the bulk silicon contribution, long storage times (or low dark currents) at reduced temperature require low defect density devices.

IMAGER PERFORMANCE

The successful use of large area CCD imagers in any application requires that an array meet many performance criteria simultaneously. In particular, low dark current with high uniformity must be combined with high uniform spectral responsivity to optical radiation. This latter parameter is of particular concern because large pixel to pixel nonuniformity in response may require excessive data reduction programs to allow maximum information to be obtained from the array. High CTE will result in maximum SWAR across the array while the backside illuminated geometry will provide the highest responsivity and quantum efficiency. Other parameters, such as their membrane planarity, will impact the final design of the optics which focus the image onto the CCD surface.

Operation of a 400×400 array at 10 kHz requires a read out time of 16 sec versus 1.6 sec for the 160×100 . The read out sequence must be performed in the dark to avoid image streaking. Low data rates also streak out any individual blemished pixels so that defects which appear strongly localized at 3 MHz are not as well defined at 10 kHz. While this will improve uniformity of response, it limits the dynamic range of the imager. Imagery taken with the 400×400 at -40°C with a 0.25 sec integration time and a 10 kHz read out is shown in Figure 4.

Performance parameters for two representative 160×100 buried channel arrays

have been presented elsewhere. In Table I,

TABLE I

Characteristics of Typical (Best in Brackets) 160 x 100 Arrays and Initial 400 x 400 Arrays

CTE	160 x 100: 0.9999 (8V Clocks)	400 x 400: 0.9999 (8V Clocks)
Dark Current 24°C -40°C	6.5 (1.8) nA/cm ² 0.008 (0.0011) nA/cm ²	7.4 nA/cm ² 0.19 nA/cm ²
Responsivity	90 mA/watt (No AR)	72 mA/watt (No AR)
SWAR at the Nyquist Frequency		
Parallel to Serial	49% (Array center)	39% (Center)
Perpendicular to Serial	50% (Array center)	36% (Center)
Uniformity of Response (-40°C)	0.12 (0.08)	0.16
Dark Uniformity (-40°C)	0.50 (0.14)	0.43

representative average and best parameter values are given for 160 x 100 devices based on experience gained during a twelve-month period. Also shown are values for initial buried channel, 400 x 400 arrays. Excellent charge transfer characteristics are evidenced by high CTE and SWAR. For the larger array, there is only a few percent decrease in SWAR going from a pixel near the output to one far from the output.

The 160 x 100 array design has on chip preamplifiers with MOSFET loads which result in heating of the membrane and this can limit device storage time. The storage times quoted above were determined by disabling the amplifiers during a variable integration period and reading out the serial register rapidly at 1 MHz. Membrane heating from the source follower on the 400 x 400 can also be observed at long integration times where typical on chip power dissipation is 20-40 milliwatts for a 5 kΩ off chip load. This lead to increased dark current nonuniformity. These effects can be minimized however by positioning the amplifier on the thick silicon rim or by using a higher load resistor (say, 50 kΩ) which is certainly permissible for 10 kHz data rates. As indicated in Table I, initial 400 x 400's, which were processed on three-inch silicon, typically showed a higher density of localized dark current blemishes than expected from recent 160 x 100's. The contribution of these blemished pixels to array dark current does not decrease like $T^{3/2} \exp(-Eg/2kT)$ as predicted and higher than expected dark current is measured at -40°C. These localized spikes

may be due to defects in the silicon substrate, residual impurities in the silicon, or implant damage which is not completely annealed. Subsequent processing improvements are expected to significantly reduce these localized dark current sites to the low levels seen in the smaller arrays.

The backside illuminated CCD should be characterized by highly uniform responsivity since optical radiation is focused on an etched silicon surface. However, membrane thickness non uniformities often result in bands of higher (or lower) sensitivity. Uniformity of response, as measured by sampling each pixel with a multichannel analyzer and defined as the standard deviation divided by the mean, has been limited to about 8%. Variations in the backside accumulation process used at the membrane surface also lead to non uniformities in response, particularly at shorter wavelengths. Devices with 70% quantum efficiency at 4000 Å have been fabricated but at present an average value is in the range 10 - 20%. High QE devices often show some variation in responsivity as the temperature is decreased from 24°C to -40°C which is generally not observed in the lower QE devices. Surface passivation with AR coatings of SiO have been applied to the membrane surface and appear to stabilize device response against long term variations. It is expected that improved etching techniques together with passivation will eventually result in response uniformity of 5% or better.

CONCLUSIONS

High performance, backside illuminated CCD arrays have been demonstrated in a configuration sufficiently large to have application in a spacecraft environment. Operation at low data rate and -40°C appear to be compatible with the thinned CCD technology. Further improvement in array performance is predicted and improved packaging techniques, particularly aimed at increasing stability of the thin membrane, will be implemented to allow eventual application in the spacecraft camera system.

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*This work was performed for the Jet Propulsion Laboratory, California Institute of Technology, sponsored by the National Aeronautics and Space Administration, under Contract No. NAS7-100.

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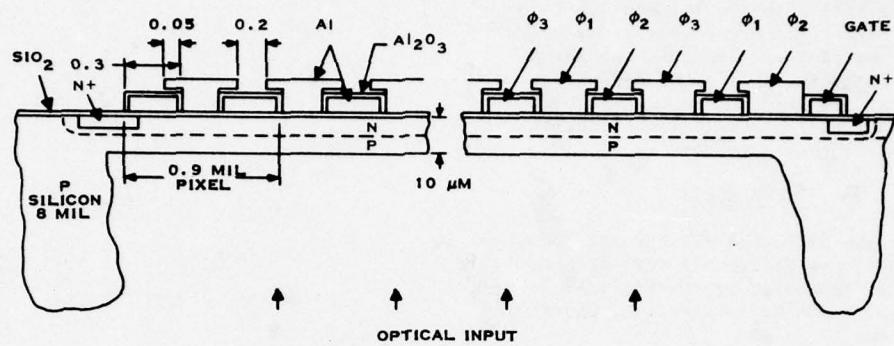


Fig. 1. Schematic of backside illuminated, double level metal CCD.

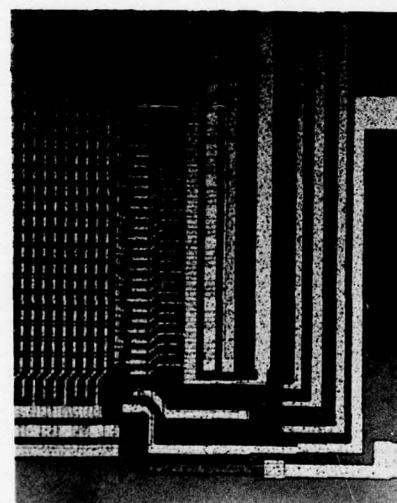


Fig. 2. Photomicrograph of one corner of the 400 x 400 array showing both serial and parallel busing from one side. The output amplifier is a reset switch and source follower.

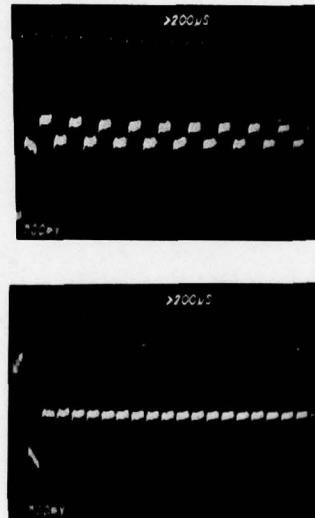


Fig. 3. Line video output from CCD using ϕ_1 parallel for integration (a) and $\phi_2 + \phi_3$ for integration (b).



Fig. 4. Imagery of the IEEE Standard taken with a 400 x 400 at 24°C and 1 MHz data rate corresponding to a frame time of 163 msec.

AN INTENSIFIED CHARGE COUPLED DEVICE
FOR
EXTREMELY LOW LIGHT LEVEL OPERATION

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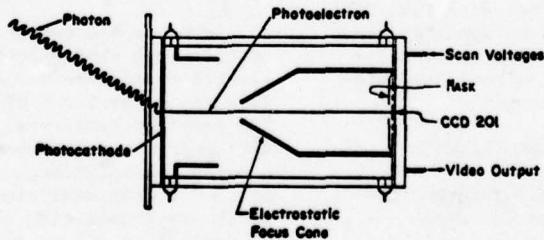
ABSTRACT An internally Intensified Charge Coupled Device (ICCD), using a semi-transparent photocathode and front illuminated Fairchild CCD201 is described. A light detection system incorporating the ICCD should ultimately permit single photoelectron discrimination at a scan rate of about 350 frames a second. This will provide a data rate which is an order of magnitude larger than comparable systems. Such a device, the first of this type, has been fabricated by the Electronic Vision Company and recently tested at the University of Maryland. The tested unit, after being sealed off, had a good photocathode and the CCD operated properly after the bakeout procedure. Successful measurements of video noise, electron gain, penetration of the transfer registers and damage to the CCD were conducted. Before becoming gassy, this tube performed acceptably in the critical areas as an intensified television camera for the low light level detection. Although single photoelectron discrimination was not possible due to excess random noise, the results of the tests indicate that the expected single photoelectron operation is feasible. Another ICCD has been fabricated which has solved some of the problems found in the first device.

INTRODUCTION

An internally Intensified Charge Coupled Device (ICCD) using a semi-transparent photocathode (S-20) and a front illuminated Fairchild CCD201 has been designed, fabricated and tested. This was the first successful test of an imaging ICCD. It is designed ultimately to permit single photoelectron discrimination at a scan rate of about 350 frames per second. For diffraction-limited astronomical observations on large telescopes,

a detection system using an ICCD has a data rate which is better, by a factor of ten to thirty, than the best available or projected detection system.

This ICCD, to be operated as a photon counting array, is a sealed off device and has the basic configuration indicated in Figure 1.



Schematic Diagram of Intensified Charge Coupled Device
Figure 1

An incident photon is converted to a photo-electron at the photocathode (an S-20 in this case). This photoelectron is accelerated to an energy of about 15 Kev and electrostatically focused onto the front surface of a Fairchild CCD201. By ionization within the active silicon, the accelerated photoelectron creates a large number of hole-electron pairs at a particular photosite on the CCD. These charges created by the single photoelectron, are collected and form a charge packet which is "scanned" from the CCD by the electrical pulse trains generated from an external clock. After a stage of amplification, which is performed on the chip, the voltage levels which represent the magnitude of the charge packet leave on a single video output line. This data stream is then electronically processed to individually detect the charge packet produced by each photoelectron.

The current status of the work being done at the University of Maryland on the internally Intensified Charge Coupled Device (ICCD) will be discussed. A general description of the theory and method of operation of the ICCD was presented in March 1975 at the Symposium on Charge Coupled Device Technology for Scientific Imaging Applications held at the Jet Propulsion Laboratory¹. The fabrication of such a tube at the Electronic Vision Co., a division of Science Applications, Inc. has also been described in some detail² by John Choisser.

In this paper we shall discuss the results of a series of measurements made on a CCD and on an ICCD. The latter was fabricated at the Electronic Vision Company and was received at the University of Maryland in late June.

PHOTO SENSOR REQUIREMENTS

This development effort with the ICCD is motivated by two different applications being developed at the University of Maryland. These related applications have significantly different requirements.

AMPLITUDE INTERFEROMETER REQUIREMENTS

The primary application of the ICCD will be as the light sensor for a new instrument, the Multi-Aperture Amplitude Interferometer (MAAI), which yields diffraction-limited image information when used on a large telescope. This instrument

is a multi-channel version of a similar instrument which has been used in an astronomical observation program over the last few years^{3,4,5,6}. Basically, this application requires an array of photosensors, each of which has a high speed response and the ability to discriminate at the single photoelectron level. The requirements are:

1. The ability to discriminate reliably among zero, one, two, or more photoelectrons per pixel per scan.
2. The ability to complete the scan of an entire frame in a few milliseconds.
3. Very low lag, i.e., very little memory from one frame to the next frame.
4. Minimal cross talk between spacial channels (or pixels).

IMAGING CAMERA REQUIREMENTS

The other application in which the ICCD will be used in conjunction with the MAAI consists of an imaging camera in the focal plane of a large telescope. For this application, the first of the above requirements is very important, while the latter three are important but not paramount. The imaging use has the additional requirements of:

1. Very large dynamic range
2. Very low blooming

The electronic operating conditions for the ICCD will be somewhat different for each of the two applications.

METHOD OF CCD OPERATION

THEORY OF OPERATION OF THE CCD

Photons are converted on the photocathode into photoelectrons. These photoelectrons are accelerated to 15 Kev and focused on the front of a Fairchild CCD201. The transfer registers, which carry the charge from the photosensitive sites to the on-chip preamplifier, operate independently of, and at the same time as the photosites which are integrating the electrons produced by ionization due to incident photoelectrons. Thus the transfers or "scanning" take place during the integration period, and the array is sensitive more than 99% of the time.

The transfer registers are protected by a layer of aluminum on the CCD which is about one micron thick. The accelerating voltage is chosen so that the bombarding electrons do not reach the active silicon and produce ionization or "noise" in the transfer registers.

ICCD DESIGN

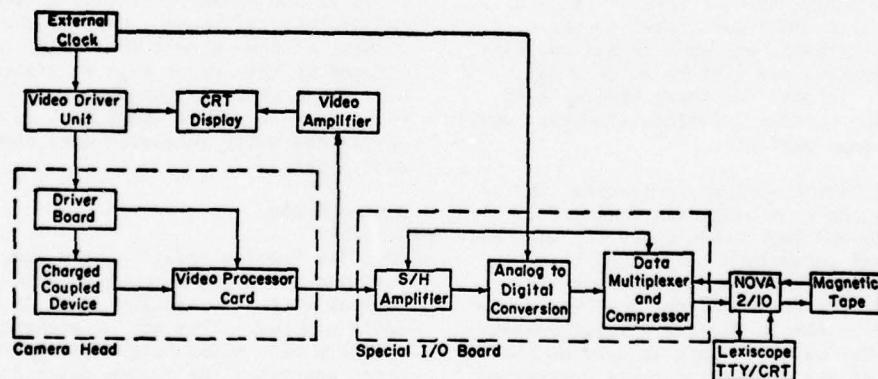
The design of the ICCD incorporates a number of features which enhance the ability to discriminate at the single photo-electron level. A special CCD201, which has the S10₂ scratch protection layers removed, was mounted by the Fairchild Corporation on a special ceramic header designed by the Electronic Vision Company. The external portion of this header provides the required electrical contacts for the CCD in a circular pattern of pins. Thus it may be socket mounted into the special camera head developed for the ICCD. The header also provides the support for the electrostatic focus cone, and the special mask which exposes the active array and protects the preamplifier and other circuitry at the edge of the chip from damage by accelerated photoelectrons. The chip is bonded directly to the ceramic header so the CCD may be readily cooled using a probe attached to an area which is clear of pins. This cooling may be required to reduce the thermally generated dark current on the chip.

OPERATION OF THE CCD

In order to permit operation of the ICCD on the telescope, most of the electronics must be located a significant distance from the camera head. To handle such long cables, a special camera head has been fabricated which minimizes cross-talk and coherent noise. The pulse trains are transmitted to the camera head or telescope as low current signals and are converted to the required high current pulses by clock drivers within the camera head. The camera head also contains amplifiers, a sample and hold circuit, a video clamping circuit, and a discriminator.

DATA RECORDING SYSTEM

The data recording system which is presently being used to test the CCD's and the ICCD's has the form indicated in the block diagram of Figure 2.



Block Diagram of Single Scan Data Recording System

Figure 2

This "Single Scan Data Recording System" is described in more detail in University of Maryland Technical Report #76-038⁷. This system records a full field of video data onto digital magnetic tape. It also provides amplification, a sample and hold operation, an analog-to-digital conversion, and proper timing and scanning voltage drives. This data recording system will operate at data rates as high as 4 MHz but can record only about a frame per second due to the writing speed of the digital magnetic tape unit.

For the tests described in this paper, the CCD was operated at a data rate of 0.625 MHz (about fifty frames per second) and thus only one frame in fifty can be recorded. In order to reduce the operating time of the tube, at the termination of each recording cycle, the computer provides a signal that indicates that further data may now be accepted. This signal operates a light-emitting diode which illuminates a broad pattern (about 13 pixels across) on the photocathode. The typical length of this light pulse is 0.1 milliseconds and its output power is peaked around 6000Å. The circuitry described in this paragraph does not appear in Figure 2.

The results of these measurements are contained in several thousand digitized arrays stored on magnetic tape. These arrays are processed in the UM Computer Science Center UNIVAC 1108, using a specially developed family of programs, the Image Processing System (IPS)⁸. The IPS may be used to read and transform the arrays, to produce averaged frames and difference frames, and perform pulse height analysis. It can, for later studies also be used for various transform (Fourier, etc.) and for image analysis.

The normal analysis procedure for this data was to average ten frames for which data had been taken under the same set of external parameters. PHD's of this averaged frame and of the difference between a single frame and the averaged frame were used to obtain Figures 4 and 3 respectively. The relative gain as well as the increase of the dark current was determined by printing out selected rows and columns of the averaged arrays, and by studying arrays which were the differences between mean dark arrays and mean "flashed" arrays.

VIDEO NOISE SOURCES

In this section we consider various aspects of the noise which are important when using the CCD both as a photoelectron sensor and as a device for the conversion of the parallel arrangement of the charge packets to the serial arrangement of the data leaving on the video output line. The relevant types of noise are defined, the physical sources of the noise are discussed, and the results of the measurements are presented.

OPERATIONAL DEFINITIONS

We first define our use of the terms "random noise" and "fixed pattern noise".

Fixed Pattern Noise

In order to define the "mean array" which corresponds intuitively to the fixed background pattern, let us consider a very large number of frames of data which are recorded consecutively under the same set of external parameters. The value at a given picture element (or pixel) of the "mean array" is determined by averaging the values of that pixel in each of the successive frames. Thus, the "mean array" is an array of elements each of which is the average of many samples. The variation of this mean array from one pixel to the next pixel is defined as the "fixed pattern noise". This data will be presented in the form of a pulse height distribution (PHD) which is the probability that a given pixel voltage will be found. Most of the discussion of mean arrays which will be considered in this paper will be limited to data taken with no light input. Thus the mean array for those cases will be a study of the thermally generated dark current at each pixel.

Random Noise

The "random noise" at one pixel is the variation from the mean value which one obtains when a particular pixel is repeatedly sampled. This may be presented in the form of a pulse height distribution which describes the random noise at each pixel. For the presently planned system, the discriminator levels are not adjusted to a new value for each pixel. To study such a system, a pulse height distribution

in which the data is combined over the entire array is more relevant. In order to obtain this information we shall subtract from a single frame of sampled pixel values the mean frame discussed in the previous paragraph. The pulse height distributions which will now be discussed are obtained by sorting the values of these differences.

More specifically, in this paper we will average ten frames to obtain the "mean frame". The use of a value as small as ten has several implications:

- i. the random noise determined from the pulse height distribution (PHD) is somewhat smaller than the value which would be obtained for a very large number of frames.
- ii. the standard deviation of the fixed pattern noise is contaminated by the addition of about 30% of the standard deviation of the random noise.

For the present, these corrections will be ignored.

PHYSICAL NOISE SOURCES

In this section, we relate the instrumental effects defined in the previous section to various physical mechanisms.

Thermal Leakage Current

This "dark current" or thermal leakage current is due to thermally generated charge pairs which are created within the active silicon. The leakage current is parameterized by the average number of electrons which collect at a given pixel during the integration interval (the thermal leakage charge). This integration interval is usually the scan or frame time. The value of the thermal leakage charge varies across the frame from pixel to pixel. It also decreases by a factor of two for every 6 or 7° that the temperature of the CCD is reduced and decreases linearly as the integration time is decreased. The average leakage charge across the frame does not significantly affect the ICCD operation but its variation across the frame may create a problem in that the discriminator levels would have to be changed for each pixel. The variation of the thermal leakage charge from frame to frame (Poisson noise) would properly be a component of the random noise,

but its value is negligible for the normal ICCD operation.

Thermal Leakage Noise

The thermal leakage noise is the variation of the thermal leakage charge across the array. This will be parameterized by the standard deviation of the thermal leakage charge across the array (i.e., the fixed pattern noise). More precisely, it is the variation of the mean (over many frames) thermal leakage charge across the array. This latter form of the definition removes the random noise as a component of the thermal leakage noise. The temperature and frame rate dependence of the thermal leakage noise is the same as that of the thermal leakage charge. In order to permit single photoelectron discrimination without a change of discriminator level for each pixel, this noise should be reduced to a value of about 100 electrons. This may be accomplished by cooling the CCD to approximately 0°C.

Random Noise

The dominant source of random noise is the input noise of the on-chip preamplifier. This behaves as if dominated by the capacitive input of the preamplifier. It is relatively independent of temperature over the range of interest for ICCD operation. The shot noise due to electrons in the charge packet should also contribute, but for the small charge packets which occur in normal ICCD operation, the preamplifiers noise dominates.

MEASUREMENTS

An important characteristic of the data recording system for this discussion is the level of system noise of the recording system. This noise consists of the contributions due to the analog-to-digital conversion, the data transfer, and the analysis procedure. By injecting a constant voltage as the input of the sample and hold amplifier on the "Special I/O Card" of Figure 2, one may obtain data to characterize the recording system.

Random Noise

Figure 3 is a pulse height distribution (PHD) of the random noise. The units on the abscissa are the least significant bits of the Analog-to-Digital Converter (ADU). These are 10 millivolts, which, with an amplifier gain of 87.5, represent 0.114 milli-

volts at the CCD. This in turn represents about 570 electrons on the chip. The latter conversion has been made using data obtained from R. H. Dyck of the Fairchild Corporation⁹ and has been confirmed by measurements at the University of Maryland. The first curve (denoted by x) is representative of the noise in the data recording system. As might be expected, this has a width of about one quantization unit (one ADU). The second curve (denoted o) consists of data taken on a standard CCD201. The noise level for the CCD is significantly larger than that of the recording system. However, as may be seen in Figure 2, this data also includes the random noise and external pick-up contributed by the electronics in the camera head (i.e., the Video Processor Card) and any ground loops which may occur in the overall system. Since direct qualitative measurements of the CCD noise yields values in the range of 300 to 400 e⁻, it would appear that there are some system contributions to curve 2 and curve 3. The third curve (denoted *) shows the random noise of the CCD in the ICCD. Figure 3 shows that there is a definite excess random noise (about 0.45 mv) in the ICCD. The cause of this is under investigation at the present time.

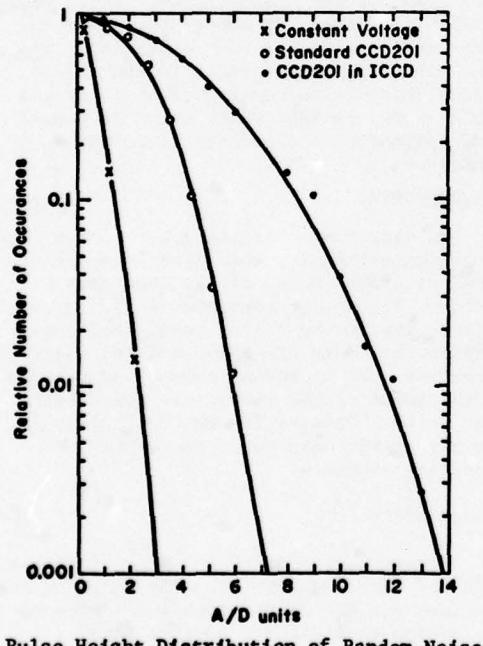
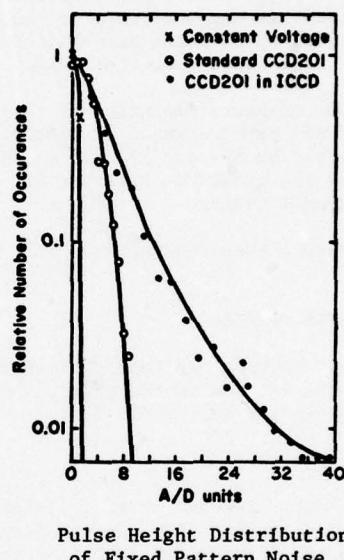


Figure 3

An additional stage of amplification is being added and future tests will include data taken with a well shielded discriminator located within the camera head. The latter should eliminate the problem of external interference and ground loops.

Fixed Pattern Noise

Since we do not intend to change the discriminator level for each pixel, an important parameter for single photoelectron discrimination is the variation of the mean array.



Pulse Height Distribution of Fixed Pattern Noise

Figure 4

The ordinate and abscissa are the same as in Figure 3. The first curve (denoted by x) is the system noise. Most of this width is assumed to be the contamination due to random noise. The second curve (denoted by o) is a standard CCD201. The relative narrowness of this PHD indicates that the variation is relatively small (approximately 3 mv). The third curve (denoted *) is obtained from the CCD201 in the ICCD. The similarity of the upper portions of curve 2 and curve 3 indicates that the background is about as uniform as the previous CCD. The wide skirt indicates that there are regions of increased leakage current. These regions were also visible on the monitor display as relatively broad

localized areas. They might have been on the CCD before processing, or they might be nucleation centers formed while processing the ICCD. The CCD's to be used in future ICCD's will have data packages taken before and after processing.

The width of these curves may be made as narrow as required for single photoelectron discrimination by cooling the CCD.

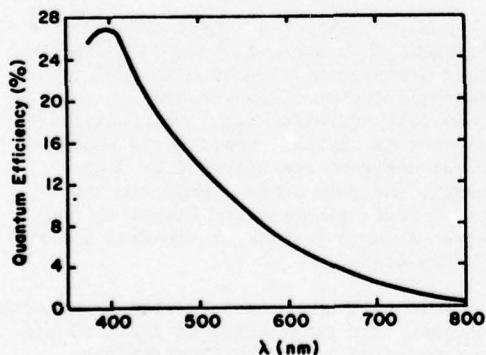
INTENSIFICATION

ROLE OF NOISE SOURCES

As has been discussed by Dyck, the expected r.m.s. random noise is about 300 e⁻ and this is dominated by the capacitive input of the preamplifier.¹⁰ At the nominal operating voltage of 15 KV, the calculated gain is about 2,000. The pulse height distribution which is then expected will permit single and multiple photoelectron discrimination¹.

PHOTOCATHODE

Since some groups have had significant contamination problems when forming photocathodes with alkali vapors in the presence of silicon devices, the photocathode of the ICCD is processed in a region well removed from the CCD⁴. A very high performance photocathode and elimination of alkali metal "vapors" are achieved by using a molecular beam technique. The response of the photocathode (roughly of S-20 type) of the ICCD used in these measurements is indicated in Figure 5.



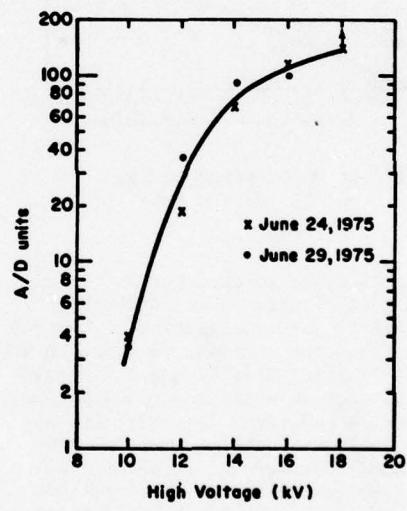
Quantum Efficiency of ICCD Photocathodes

Figure 5

DESCRIPTION OF TEST ICCD

The remaining tests were conducted on an ICCD of slightly different design than indicated in Figure 1. The device tested (denoted as ICCD-1) had no focus cone and relied on proximity focusing. It has about the same dimensions as the device in Figure 1. The measurements on this device were terminated after the second test sequence due to ion bombardment of the photocathode because the tube became gassy. This fabrication problem has apparently now been solved and another ICCD has been fabricated.

The electron gain may be studied by varying the accelerating voltage while maintaining a fixed light input. The tests conducted on 24 June 1975 were run using a light pulse from the LED which has a length of 10 milliseconds and a Neutral Density 2 filter. The tests conducted on 29 June 1975 were run with a 0.1 ms pulse and no filter in front of the LED. This data appears in Figure 6. The 18 KV point is low due to saturation of the A/D converter.



Relative Electron Gain

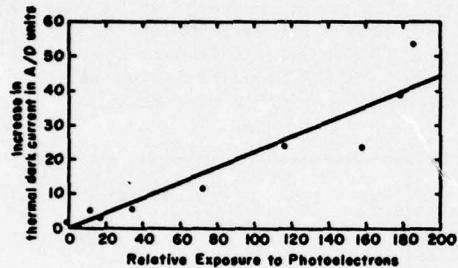
Figure 6

The nominal operating voltage of 15 KV was determined to prevent a photoelectron which is focused on the transfer registers from either entering the active silicon or the last insulation layer. By sufficiently increasing the accelerating voltage, one expects that the photoelectrons will pene-

trate the active silicon and produce a signal. However, this has not yet been observed even up to 18 KV.

DAMAGE

A preliminary test of the effect of extended exposure was used to study the operational lifetime. In this test, the light input was increased in one area until there was an observable increase in the dark current. This increase in thermal leakage was measured by a comparison of the magnitude of the dark current before and after the exposure to light. No re-adjustment of the drive voltages was made. The resultant enhancement of the dark current as a function of the exposure to photoelectrons is shown in Figure 7.



Effect of Electron Damage
on CCD Dark Current

Figure 7

The increase in dark current is expressed in A/D Units, each of which is equivalent to 0.114 millivolts at the CCD output. Thus the increase is about 40 ADU or 5 millivolts. This is somewhat above the fixed pattern noise due to variations in thermally generated dark current, and is less than 5% of CCD saturation. The light input consisted of repeated flashes with a duration of 0.1 ms repeated 1000 times a second. Assuming a gain of 2000, this is equivalent to an input of 0.4×10^6 photoelectrons per pixel in the brighter region.

Measurements on similar devices¹¹ indicates that this damage mechanism saturates. The effect on single photoelectron operation would be to require additional cooling (perhaps -20°C) in order to assure

that the increased dark current will not affect the single photoelectron discrimination operation. More extensive tests are planned on the later ICCD's to explore other damage mechanisms which may occur at higher light doses. In addition, several methods of annealing the damage, which have worked in similar devices, will be tested.

CONCLUSIONS AND PROJECTIONS

An Intensified Charge Coupled Device has been designed and fabricated. The first unit, after being sealed off, had a good photocathode and the CCD operated properly after the bakeout procedure. Successful measurements of video noise, electron gain, penetration of the transfer registers and damage to the CCD were conducted. It performed acceptably as an intensified array for the low light level work. For several reasons, the first device did not meet the performance criteria which are required for reliable single photoelectron discrimination. These problems were a gas leak in the tube and the excess random noise. However, the results of these tests are in general agreement with predictions, which indicate that such a device will be able to do single photoelectron discrimination. In addition, the ICCD showed no transfer noise, even at elevated voltages.

The gas leakage problem seems to have been solved and another ICCD, which is electrostatically focused, has been fabricated.

ACKNOWLEDGEMENTS

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This work has been supported by several agencies. The fabrication of the ICCD has been supported by Goddard Space Flight Center, and by the Space and Missile Systems Organization through Science Applications, Inc. The specialized electronics for the

operation of the CCD at single photoelectron sensitivity has been supported by the National Science Foundation. The data handling and recording electronics, which may be used on any rapid scan photon counting detector, has been supported by the Advanced Research Projects Agency through the Office of Naval Research. The program development and data reduction were largely carried out at the University of Maryland Computer Science Center with the support of NASA grant NSG 398.

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CCD DYNAMICALLY FOCUSED LENSES FOR ULTRASONIC IMAGING SYSTEMS

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ABSTRACT. Charge coupled device (CCD) delay lines offer many useful features when incorporated into multi-piezoelectric-element electronically focussed successors to the single element ultrasonic imaging systems currently in clinical use on humans and in non-destructive testing use on materials.

Two such electronically focussed systems are presented: (1) a microprocessor controlled delay line system and (2) a single chip C3D lens system.

INTRODUCTION

Ultrasonic imaging systems are currently in use: (1) on humans in a variety of medical imaging applications and (2) on materials in non-destructive testing applications. Single element piezoelectric transducers are used in these commercial instruments to obtain cross section scans using mechanical scanners and storage CRTs. Charge coupled device (CCD) delay lines offer many useful features when incorporated in multi-piezoelectric-element electronically focussed successor to these single transducer systems. Briefly stated the CCD acts as an electronically adjustable delay line performing the required delay-sum operation on the 1-5 MHz ultrasonic signals. This CCD capability makes economically feasible an ultrasonic imaging system with the following features:

1. High resolution
2. Dynamic focussing
3. Adjustable field of view

CCD ULTRASONIC IMAGING

The basic acoustic imaging problem being considered is shown in Fig. 1 along with a simple signal processing architecture. In operation a burst of ultrasound is transmitted from the "array" of piezoelectric transducers. Reflections from the "target" return to the array, arriving at the elements with a spherical time delay distribution associated with the target range (the farther away the target the smaller the

time delay between elements in the spherical distribution). The basic signal processing task to be performed by the delay lines is to equalize the total propagation time from the target through the medium, piezoelectric transducers and individual channel electronics to the common signal output summing node. It is accomplished by spacing the input taps of the CCD delay line in a quadratic arrangement and dynamically sweeping the clock frequency to control the curvature of the quadratic delays to complement the curvature of the spherical wavefronts from targets T_1 through T_2 and beyond. It permits significant improvements in resolution at ranges less than ten times the aperture of the system.

One may consider a system as shown in Fig. 2 which utilizes a linear delay distribution (in cascade with the quadratic distribution) to steer the "focussed" beam providing two-dimensional display information. This is a simple steering technique which allows deflection of the formed beam in one direction from the perpendicular. Typical systems may be designed for thirty to forty-five degrees deflection. In operation the linear array of delay lines "electronically rotates" the piezoelectric array thereby providing the quadratic delay line with focus task similar to the "on-axis" focussing just discussed. One minor difference in focussing is that the apparent range for focussing is larger than the range to the midline of the array due to the "elec-

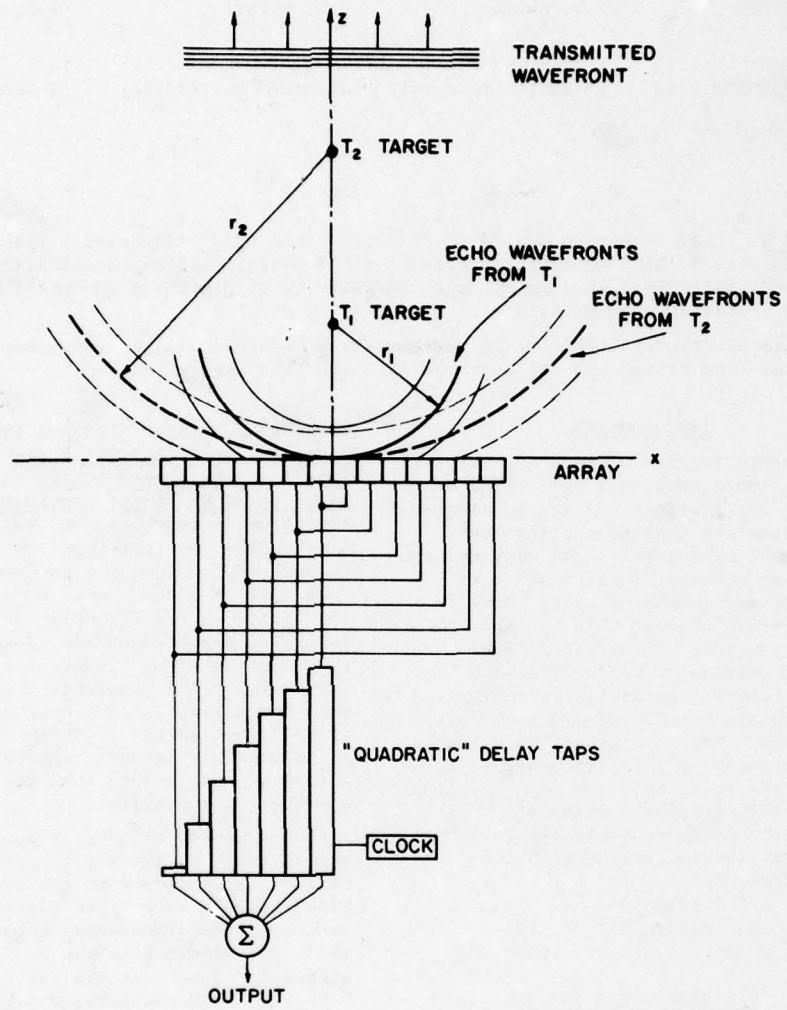


Fig. 1. Dynamic Focussing with Quadratically Tapped Variable Delay Line.

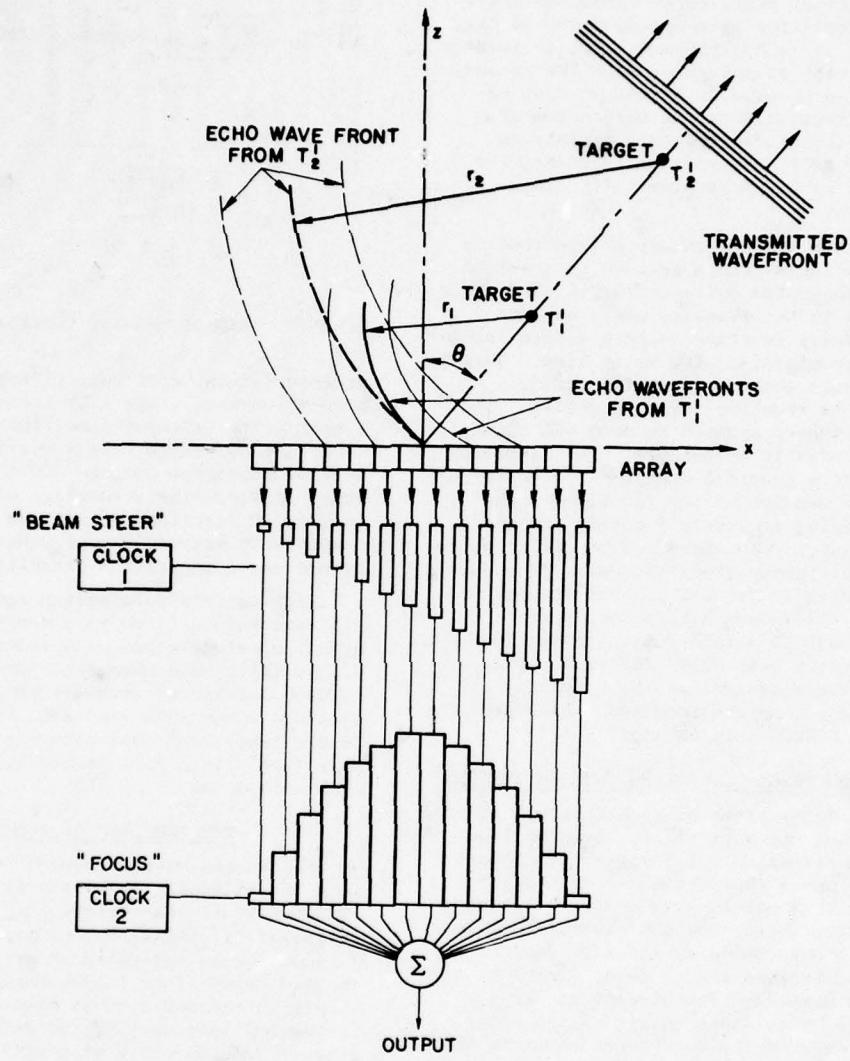


Fig. 2. Dynamic Focussing and Beam Steering with Variable Delay Lines.

tronic rotation" being about the point of zero (beam steer) time delay (i.e. the far end of the piezoelectric array from the target).

In actual practice two problems exist with implementing this system shown in Fig. 2. First it is desirable to have as large a field of view as possible, thus the formed beam should be capable of being swept in either direction from the perpendicular. Secondly the clock frequency variations should be kept to a minimum to reduce the variation of CCD parameters with clock rate.

The two systems concepts described in the following sections achieve this set of goals through two quite different approaches. The first to be discussed achieves each channel delay function using a single serial-in-serial-out (SISO) CCD delay line. Thirty-one channels (one for each transducer element) is required for this system. The clock frequency applied to each CCD channel is independently adjustable. The frequency applied to a specific channel is a multiplicative product of two functions: the beam steering frequency function and the focus frequency function. Each CCD clock is applied uniformly along the delay line but is time-varying in frequency. The second approach utilizes a single specially-designed C3D lens integrated circuit for the entire system time delay function. This single chip approach has the potential of realizing a complete focussed ultrasound probe in a hand held package.

A MICROPROCESSOR-CONTROLLED IMAGING SYSTEM

The delay lines of an ultrasonic imaging system thus may perform two forms of time delay equalization: (1) parabolic (focus) and (2) linear (beam steer). An experimental ultrasonic imaging system has been built using thirty-one 200 element serial-in-serial-out CCD delay lines to perform the quadratic and linear delay functions of a single piezoelectric element in one device [6]. As shown in Fig. 3 the delay time of each of the thirty-one channels is determined by the digital rate multiplier assigned to each channel.

A voltage controlled oscillator (VCO) and a sweep generator are used to dynamically control the time delay for focussing, and an 8080 microprocessor is used to control a rate multiplier for beam steering. This system is capable of ± 30 degrees deflection and

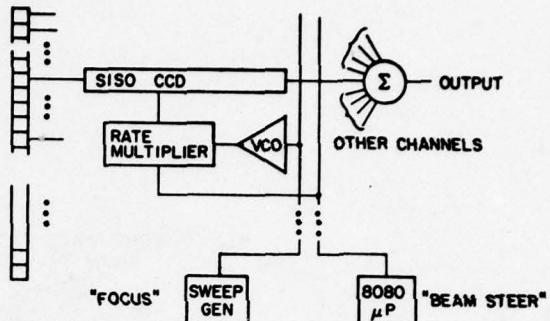


Fig. 3. Microprocessor Controlled System.

dynamic focussing of echoes from ranges of 2 to 40 cm when using a 31 element 3.1 cm linear array (element dimensions are .1 x 1 cm). This system uses a multiplicative control algorithm for the CCD time delays which provides the separation of focus and beam steer functions into tasks which are amenable to microprocessor control and simple sweep generation circuitry.

Unfortunately this system requires significant volume (1 cu.yd.) due to the large amount of electronics associated with each of the thirty-one channels. Over seven hundred integrated circuits and six thousand discrete components are used. There is little likelihood that with present technology this system will be configured in a hand-held probe.

THE C3D LENS ON A CHIP

The cascade charge coupled device (C3D) is a recent invention of the Stanford Integrated Circuits Laboratory [4] that has the potential of realizing a compact focus unit. This device is basically an array of charge coupled delay lines interconnected on a single integrated circuit substrate and having multiple sections of delay each clocked independently at a different frequency giving flexibility in design which can be utilized to realize sophisticated signal processing functions. Multiple input taps (first demonstrated in the Stanford Razorback CCD [5]) combined with multiple sections experiencing different clock rates yield devices capable of performing the high speed spatial Fourier transform

required for the imaging task.

A simple form of C3D lens is a device which incorporates all of the delay electronics in Fig. 1b on one silicon chip. Signal charges injected by the transducers in the piezoelectric array undergo time delays determined by the frequency of clock 1, clock 2, and the number of bits transferred in the sections controlled by these two clocks.

The acoustic imaging system shown in Fig. 2 may be considered to have an optical equivalent of a wedge shaped lens for linear delay closely spaced with a spherically shaped lens for quadratic delay. The "thickness" of both lenses may be electronically varied to steer and focus the lens system on different target points.

Thus the C3D lens realizing this delay function may be considered as having two lens elements in one group on a single silicon chip. There is significant advantage in optics as well as in C3D lenses to have more than just two lens elements in an imaging system. The single parabolically shaped lens in Fig. 2, for instance, actually can be realized to advantage using multiple elements to correct for imaging and electronic aberrations. Fig. 4 shows photomicrographs of two element and three element

C3D lens versions designed and fabricated at Stanford to perform the parabolic lens function shown in Fig. 2.

The device on the right of this figure is the two element parabolic lens. This two element device uses the first element to increase the curvature of the arriving wavefront by a large constant amount (large in comparison to the curvature of the typical wavefronts being imaged). The second element in this two element lens focusses the highly curved wavefronts, i.e. decreases the curvature to a linear wavefront. The total curvature function focussed by the second element is a large constant curvature added to the curvature of the acoustic waves impinging upon the piezoelectric array. Thus the variations in the second element "thickness" (clock frequency) with changes in focussed range are small in comparison to the total second element thickness. This two element C3D lens requires significantly less clock frequency variation with focus range variation than single element equivalents. For an imaging system designed at Stanford this two element lens requires the 2 MHz variation of a 5 MHz clock while a single equivalent lens would require a 45 MHz variation (45 MHz variation is impractical for present day C3D lenses).

The three element lens shown on the left side of Fig. 4 can be used in several modes. The simplest is to simulate a two element lens by clocking the first two elements at an identical, time invariant frequency, and the third element at a frequency in keeping with the focus requirements. Since this two element lens has a first element with twice the number of sample storage positions as the previously described lens, this allows the clock frequency of this element to be twice that of the previously described two element lens. This design technique of allowing choice of clock frequencies provides a method for designing difference frequencies (cross modulation products) of the two clocks to be outside the passband of the ultrasonic channels used.

The goal of this C3D development program is to realize a device as shown in Fig. 5 which incorporates both the focus and beam steer functions on a single chip. As can be seen in this figure two wedge shaped "lens elements" are used to realize this beam steer function. Thus if clocks 1 and 2 are equal in frequency, there is no delay differ-

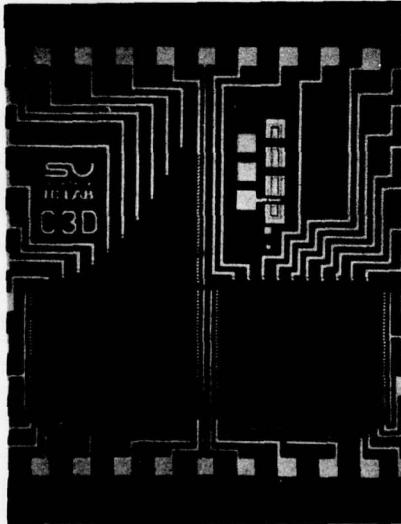


Fig. 4. C3D Prototype Devices.

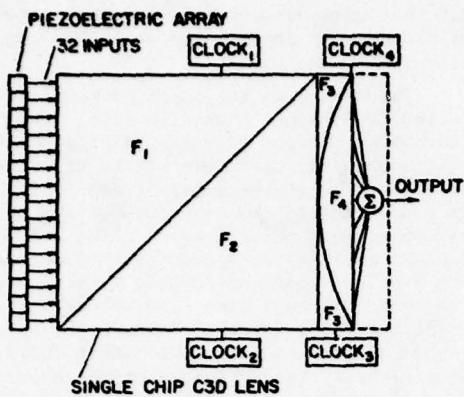


Fig. 5. C3D Lens with Beam Steer and Focus Elements.

ence between channels introduced by the two wedge-shaped delay functions. Beam steering off axis may then be accomplished by clocking the two lens elements at different clock frequencies (the larger the difference frequency the larger the formed beam deflection off axis).

Thus the C3D shown in Fig. 4 is comprised of isolated channels of delay (32 shown in the figure) experiencing different zones (F_1 , F_2 , F_3 and F_4) of signal propagation velocity determined by the clock frequency of the respective zone. Different channels experience different quantities of delay determined by the number of elements that channel has in each of the zones and the clock frequency of those zones.

There are three classes of focus aberrations associated with the C3D lens which must be considered in any practical system design. These are

1. Dynamic focus aberrations
2. Focus approximation aberrations
3. Electronic distortion aberrations

Dynamic focus aberrations result from "moving the lens" before all elements in the array have received a given wavefront. In the C3D lens design shown in Fig. 5 it is assumed that the lens will focus only at one depth during operation. In practice, the focus range is scanned in synchronism with the returning echoes. Initially after a transmit burst the lens is focussed close to the array to focus nearby targets, then is dynamically scanned in synchronism with the returning echoes from target at greater

depths. Unfortunately the lens must be moved before the entire wavefront from a given depth arrives to every element in the array. The outer elements in the array are therefore focussed farther from the array than they should to be exactly focussed on the arriving wavefront. This focus error is called dynamic focus aberration. In the microprocessor controlled system shown in Fig. 3 there is no dynamic focus error for on-axis imaging. This system has the design flexibility to focus the outer elements at different depths than the inner elements due to the separate focus oscillator on each channel. In the C3D lens, however, extra lens elements (clock zones) may be added to connect for this form of aberration.

These are aberrations due to the focus approximation used in the device design shown in Fig. 5. This device uses parabolic delay equalization for a spherical wavefront. While a C3D lens could easily be designed to exactly equalize (except for truncation error) the delay for a specific spherical wavefront, it could not be scanned by varying the clock rate to equalize other spherical wavefronts. Thus the parabolic approximation which is fairly accurate at ranges greater than the aperture of the array is used to accomplish a generally useful focus function in a single device. As in the case of dynamic focus aberration, additional lens elements may be used to advantage in reducing this form of aberration.

Electronic aberrations encompass all of the imaging distortions due to the non-ideal parameters of the C3D lens. Two significant sources of electronic aberrations in the C3D lens are (1) charge transfer efficiency (2) cross modulation distortion. The efficiency of charge transfer between storage electrodes determines the total number of storage elements permissible between device input and output. Large charge transfer losses result in a reduced delay line bandwidth. Typically transfer loss considerations limit the total number of storage elements in a channel to five hundred and the maximum clock frequency to fifteen megahertz. Intermodulation distortion results from the interaction of the four clock frequencies shown in Fig. 5 with nonlinearities at the C3D inputs, output and lens element interfaces. While the input and output cross modulation distortions may be eliminated in principal by shielding these points from the clocks, the lens element interface cross modulation distortion is

primarily a function of the design of the lens interface and the respective clock frequencies of the lens elements on each side of the interface. This interface cross modulation distortion is the result of the asynchronous partitioning of charge packets which arrive at an interface with a propagation velocity different from the packets leaving the other side. In this case the packets are regrouped resulting in a difference frequency being generated. From a spectral point of view one may consider the signal packet as being resampled at each interface by a special type of sampler. If the resampling is not performed at frequencies large enough to encompass twice the highest frequency sampled, some aliasing will occur.

Unfortunately the spectrum to be sampled is very rich in harmonics so insuring twice that the largest frequency component be sampled is impractical. Fortunately some averaging (low pass filtering) occurs at the interface reducing the magnitudes of some of the aliased components. In a practical system design using C3D lenses the spectrum and magnitude of these difference frequencies relative to the desired signal passband should be considered. A detailed analysis of electronic distortion aberrations is beyond the scope of this paper.

SUMMARY

Two electronically focussed ultrasound imaging systems have been presented. Both systems offer significant improvement in resolution compared with single element systems for ranges from one to ten times the system aperture. The microprocessor controlled system offers fewer sources of imaging aberrations while the single chip C3D lens offers high performance in an extremely compact and potentially economical system configuration.

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CCD-TV CAMERAS UTILIZING INTERLINE-TRANSFER AREA IMAGE SENSORS

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ABSTRACT

A recently developed Fairchild CCD area array image sensor of 190 x 244 elements, described in a paper by Kim, Steffe, and Walsh at this conference, and a 380 x 488 element device currently being developed have design features which simplify application of these sensors in compact, highly ruggedized solid-state TV cameras. Sensor characteristics are reviewed with emphasis on the reduction of camera circuit complexity resulting from the use of two-phase charge transport principles in combination with interline-transfer device organization.

Several camera designs using the 244 and 488 devices are described including a 488 LLLTV camera and a 244 camera pair which effectively doubles the image format pixel density along the row direction. Experimental results demonstrating low-light-level and multiplexed camera pair operation are presented.

The MV201, Fairchild's commercial camera product is described. The design employs the 190 x 244 element image sensor. The electronic circuit blocks comprising the camera are described as well as the techniques employed for miniaturization.

Variations on the basic MV201 design are discussed. These include a two-piece camera with a 1-1/2 inch diameter 3/8-inch thick sensing head, a "G" hardened version designed to withstand howitzer shell launch conditions, and a version for use in borehole applications where the output is converted to slow-scan video for transmission over several miles of cable.

INTRODUCTION

The interline transfer (ILT) organization has been adopted for a family of charge coupled image sensors, including designs with 100 x 100, 190 x 244, and 380 x 488 elements^{1,2,3}. Each design employs two-phase (2ϕ) charge transport principles which, in combination with the ILT organization, minimizes the number and complexity of gate drive waveforms necessary for device operation. In addition, each design employs buried channel principles which eliminate the surface channel device requirement for bias charge or "fat-zero" insertion. For the 190 x 244 sensor, buried channel operation is combined with an on-chip low noise distributed floating gate amplifier (DFGA) with a resultant significant increase in low light sensitivity^{3,6}. Threshold signal packets of a few tens of electrons can be efficiently transferred and detected.

As shown in Figure 1, the total number of gate drives or forcing-functions for ILT operation is significantly less than for a typical 3ϕ frame-transfer design-simplifying the utilization of ILT sensors in compact, all solid state TV camera equipment. The 3ϕ design requires the generation of 3 different waveforms for each of the 3 sets of vertical (V) and horizontal (H) transport gates. Only two V and H transport waveforms are required for the 2ϕ ILT since the inputs for each H and V pair are complementary.

Figure 2 illustrates the ILT organization and the forcing-function inputs required for self-scan operation as a TV image sensor. The unit cells contain one photosensor site and an adjacent light-shielded site which is one-half stage of a 2ϕ vertical-transport register. Cell dimensions are defined by comb channel stop boundaries on three

sides of the photosite. Alternate cell rows are uniquely assigned to each of the two fields comprising a TV frame resulting in higher vertical MTF than for beam-scanned or frame-transfer type image sensors. An implanted potential barrier at the photosite/transfer site interface inhibits transfers to the vertical column register, except when the photogate (ϕ_p) is LOW and the adjacent transfer gate (ϕ_{V1} or ϕ_{V2}) is HIGH. Thus, 2/1 interlace readout is achieved by pulsing ϕ_p LOW during each vertical blanking interval and applying complementary ϕ_{V1} , ϕ_{V2} waveforms with HIGH states during alternate V-blanking periods.

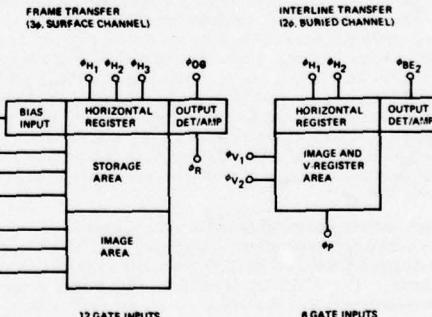


FIGURE 1. GATE DRIVE INPUTS FOR CCD-TV IMAGE SENSORS

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At the start of the ODD field readout, elements corresponding to odd number rows are first shifted in unison into adjacent ϕ_{V1} sites for row transport along the column registers to the output register. The EVEN field sequence is similar except the initial shift is into ϕ_{V2} sites. Row transfers at the output register interface (for both ODD and EVEN rows) are effected by holding ϕ_{V1} LOW and ϕ_{H1} HIGH during the horizontal blanking interval. Complementary square wave pulses at element rate are applied to the ϕ_{H1}, ϕ_{H2} transport gates to serially shift packets to the output detector.

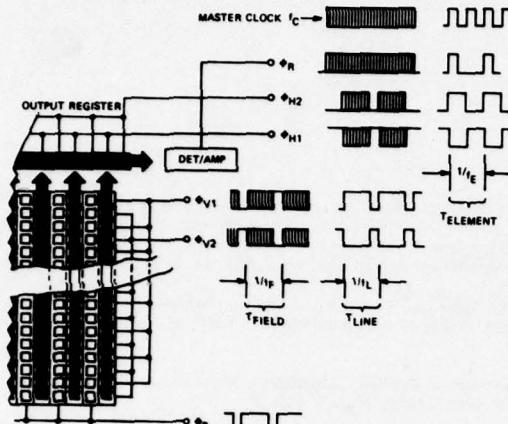


FIGURE 2. INTERLINE TRANSFER CCD ORGANIZATION AND DRIVE INPUT WAVEFORMS

CAMERA DESIGN FOR 525 LINE TELEVISION

Circuit functions for a TV camera using interline-transfer image sensors are illustrated in the block diagram, Figure 3. With the exception of the CCD and its associated gate drive waveforms, similar functions (plus horizontal and vertical scanning) are necessary for conventional camera designs using beam-scanned image sensors. A typical ILT-CCD camera logic design employs a crystal clock at frequency $f_C = 2f_E$, where f_E is the element readout rate, to provide decoding edges for pulses shorter than an element period. All CCD gate waveforms, and the display sync and blanking signals are derived from f_C by divide-down counters and combinational logic circuits.

A beam-scanned camera design requires relatively complex logic circuits to conform with 525 line TV system specifications such as EIA RS-170. In this case, the function of the logic is to synthesize synchronization and blanking waveforms with timing edges defined from the output of a master clock operating at a high multiple of the line scan frequency f_L . A typical single-chip MOS-LSI TV signal generator, such as the Fairchild type 3262, is controlled by a crystal clock operating at 910 f_L , facilitating the generation of a synchronous NTSC color subcarrier output at the nominal US Standard 3.58 MHz rate⁴. Decoding edges for either monochrome or color system outputs are derived from an on-chip square wave clock at 130 f_L .

Although existing waveform generators such as the 3262 do not provide CCD gate signal outputs, a modified CCD/RS-170 compatible design is feasible if the CCD design conforms to system specifications. For CCD imaging sensors, conformance implies a precisely defined number of readout lines per field. Also, if the CCD sensor element counts per line are properly defined, a simplified camera logic design using a single master clock input is possible.

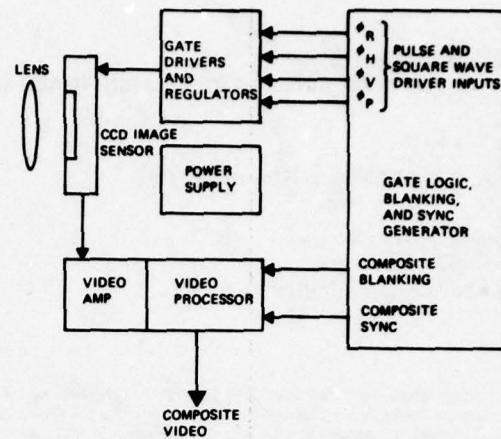


FIGURE 3. FUNCTIONAL REQUIREMENTS FOR A CCD-TV CAMERA UTILIZING AN ILT AREA IMAGE SENSOR

In accordance with 525-line monochrome system specifications the nominal values required for readout scan parameters are: line rate $f_L = 15,750$ Hz; field rate $f_F = 60$ Hz; and frame rate $f_R = 30$ Hz (with 2/1 field/frame interlace). The RS-170/3262 vertical blanking interval is (20 + 22/130) line periods/field, defining a minimum of (525-40) = 485 active scan lines, hence sensor element rows per frame.

Horizontal blanking is defined as (22/130) horizontal line periods, which is equivalent to: (22/130) ($n_A + n_B$) = (22/130) n_T where n_A , n_B and n_T define the active, blanked, and total number of element periods/line period, respectively. If n_T is selected to be 910/2 = 455, a single master clock can be used to satisfy the requirements for both RS-170 and CCD gate-drive waveform synthesis. For this condition, $n_B = (22/130) 455 = 77$, and $n_A = (n_T - n_B) = 378$. The CCAID-488B sensor currently being developed has 380 elements/row, and 488 rows, hence a few terminal rows and columns can be blanked off when blanking signal edges are properly centered with respect to the active format region.

CAMERA DESIGN USING 190 X 244 ELEMENT SENSORS

Semiconductor industry economic considerations clearly indicate a power function relationship between device cost and silicon chip size.² In addition, there are a number of TV camera applications which can be satisfied by sensors with fewer pixels/frame than required for 525 line broadcast-TV systems. These applications are being addressed by utilizing the small format (0.44 cm x 0.57 cm) 190 x 244 element sensor, as described below.

OPERATING MODES

The 190 x 244 element counts of exactly half the full format 380 x 488 design were selected to facilitate modes which are interface-compatible with existing TV system equipment including VTR's, display monitors, and TV receivers. These modes include:

FORMAT INSET MODE — All camera waveforms are identical to those required for operation of a 380 x 488 sensor, except for an extension of the horizontal and vertical blanking intervals. Thus, an NTSC compatible video signal can be generated over a portion of the full display format equal to $\frac{1}{2}$ the active height and

width. The outputs from up to four cameras can be displayed on a single monitor by appropriate phasing of the active and blanking signal intervals prior to composite signal mixing.

FULL FORMAT, SYNTHETIC INTERLACE-MODE—By modifying the camera timing generator to enable counting an integral number of lines/field near the normal 262·1/2 line value, a non-interlaced display raster can be generated with horizontal and vertical scanning rates within a few percent of industry standards. A raster thus generated is "synthetically" interlaced by alternatively addressing the display with video lines of normal sensor and blanking signal followed by an artificially generated line signal with 100% blanking. During an ODD field sensor readout, lines 1, 3, 5, ..., N_{odd} of the active format contain sensor video signal while 2, 4, 6, ..., N_{even} are blanked off, with the video/blank line sequence reversing for the following EVEN field readout.

FULL FORMAT, FAST FRAME MODE—Camera timing logic, including display synchronization and vertical-blanking signals, are altered to generate a true 2/1 interlaced display with approximately half the usual number of active scan lines per field. VTR compatibility is achieved by selecting a 120-Hz vertical rate, which is an even multiple of the standard rate. Display circuit modifications are required, however, these modifications can be limited to the vertical scan generator if the horizontal scan frequency is selected to be within a few percent of 15,750 Hz. Advantages of the fast-frame mode include the elimination of interline display flicker, enhanced resolution for rapidly moving scene information, and reduction of dark signal effects limiting dynamic range at high operating temperatures.

MULTIPLEX MODES—Other system compatible modes are possible if two (or more) 190 x 244 element sensors are arranged to view identical scene information; by utilizing optical beam splitters and a single lens, or by employing matched individual lenses in a boresight configuration. The outputs of each sensor can then be combined, i.e., multiplexed, into a single video information channel. Thus a pair of ILT sensors with 190 elements/row and 244 rows/frame can be used to generate multiplexed video for a display with twice the pixel information content. Sensor outputs can be combined to yield 380 pixels/line with 244 lines/frame or 380 pixels/line pair with 488 lines/frame. A camera utilizing one of these modes is described in the next section.

THE BORESIGHT-244 CAMERA

Interline transfer image sensors can be operated in a unique element multiplexed-pair (E-MUX) mode which doubles the pixel density in the row direction⁵. The combined E-MUX video has characteristics similar to the video from an ideal single sensor with 380 contiguous pixels/line and 244 lines/frame. This effectively doubles the sampling density in the horizontal direction while maintaining the high MTF in the horizontal direction. Implementation principles are based on two characteristics of the ILT sensor organization:

- 1) element aperture response in the row direction is defined by a photosensing site width ≤ 0.5 cell width, and,

- 2) the readout signal interval corresponding to each sensing element is approximately 1/2 the element transfer period.

A camera pair, known as the Boresight-244 System, has been constructed to evaluate multiplexing principles. This system, as shown in Figure 4, consists of two identical cameras each employing the 190 x 244 sensor. A third assembly, the Multiplex Control Unit (MCU) allows the two cameras to interact in a variety of ways. Each camera can be operated as a stand-alone unit. As such, the element readout rate is 3.75 MHz, with a frame rate of 60 Hz. With both cameras and the MCU interconnected,

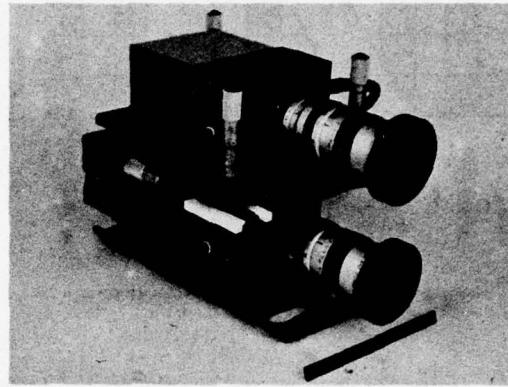


FIGURE 4. BORESIGHT-244 CAMERA SYSTEM

the cameras run synchronously in a master/slave relationship and the combined video signals can be displayed on a single monitor. After rough image alignment adjustment, the MCU is switched to the align mode. In this mode the signals from each camera are subtracted, thus an ideally boresighted pair results in a blank video display. Micrometer adjustments on one of the cameras are used to achieve alignment; once boresighted the adjustments are locked in position.

Following boresight alignment, the MCU can be switched to one of two operating modes. For resolution enhancement the MCU gates the video from each camera so that there are 380 (190 x 2) pixels per display line. In this mode the boresight alignment is modified to result in a 1/2 cell pitch offset between the image information viewed by the master and slave cameras, as indicated in Figure 5. The resolution in this mode is twice as much in the horizontal direction as for either of the contributing cameras. Vertical resolution is unchanged.

Figure 6 shows an enlarged portion of the displayed video output for the boresighted pair operating in the E-MUX mode. Horizontal resolution equivalent to the 285 TVL/PH Nyquist limit condition is obtained with both cameras operating. Applying identical techniques to a camera pair using 380 x 488 image sensors would yield a composite video output with 760 TV elements per format width; i.e., 570 TVL/PH horizontal resolution.

The other operating mode, known as the E-SUM mode, is concerned with signal-to-noise ratio enhancement. By boresighting the system and then summing the two outputs, the combined signal is twice that of a single camera viewing the same scene with the same lens T-value. Since the on-chip amplifier noise of each camera is uncorrelated, the SNR of a camera pair will be enhanced by a $\sqrt{2}$ factor.

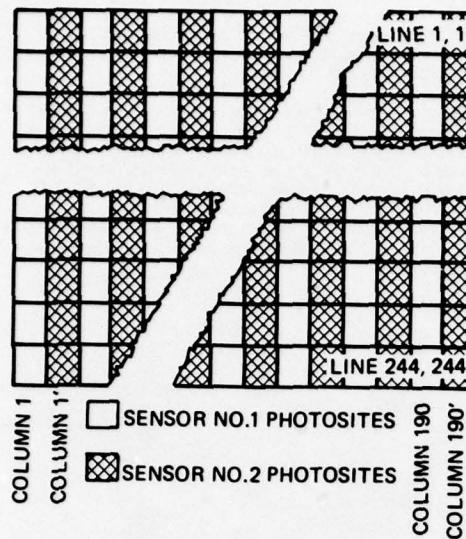
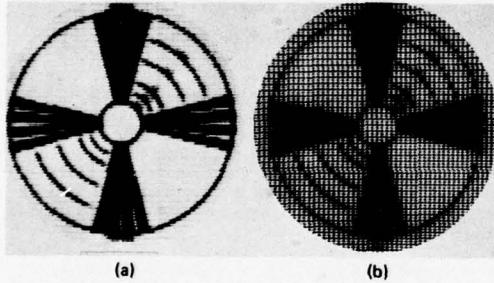


FIGURE 5. E-MUX SPATIAL ALIGNMENT FOR 244 X 190 SENSOR PAIR



(a) Enlarged portion of multiplexed-pair video display; (b) same as (a), except lens of one camera is capped. Resolution wedge calibration is 470 TVL/PH at center circle. 1st to 4th arc markings denote wedge resolutions of 312, 235, 156 and 117 TVL/PH, respectively.

FIGURE 6. BORESIGHT-244 CAMERA SYSTEM IMAGING

THE MV201 CCD-TV CAMERA

The Fairchild MV201 is a recently introduced TV Camera product utilizing the 190 x 244 element CCD-211 image sensor. Circuit design features have been included which permit packaging in a variety of compact camera configurations for specific application requirements.

The standard MV201 is housed in a near-cylindrical case, 2-½ inches in diameter and 3-½ inches long (approximately 17 cubic inches), as shown in Figure 7. It is a lightweight and rugged assembly requiring less than 4 watts from an external ±12 volt



FIGURE 7. FAIRCHILD MV201 CCD-TV CAMERA

power supply. The lens bushing is a 16mm C-mount type, however, a number of small format TV and camera lenses can be used, including Super-8mm types.

The camera electronic circuits are arranged in three major functional groups: Logic Control, Gate Drivers and Video Processing. The logic is a crystal-controlled CMOS system which provides clocking at the nominal element rate of 3.766 MHz. A choice of frame rates is available, depending on user preference. The standard camera operates at 30 frames/second using the synthetic interlace mode; a 60/second fast-frame mode is available as an option. The line rate for either mode is 16.02 KHz.

Hybrid circuits are used for both Logic and Gate Driver functions. A total of six clock signals are applied to the CCD, however, these are derived from only three input waveforms due to the inherent simplicity of drive requirements for the two-phase interline-transfer CCD.

The Video Processor contains sample and hold, gamma compensation, and automatic gain control (AGC) circuits. The AGC feature extends the operating range to sensor highlight levels of less than 10^{-3} fc (2854° K). Camera output is a composite video, sync, and blanking signal suitable for driving up to 500 feet of coaxial cable. A typical camera output image is shown in Figure 8.

MV201 VARIATIONS

Due to its small size and low power, the basic MV201 design has been used as the basis for a number of interesting applications.

In environments where space is at an absolute minimum, the MV201 can be operated as a two-piece system comprised of the camera body, containing the electronics, and a remotely located sensor. The length of the cable may be two feet or longer, depending on the availability of space for electronics at the sensor location. A cable containing less than 20 wires connects the sensor to the electronics. The applications for such a system, where in the sensor head (excluding optics) can be 1-½ inches in diameter and less than $\frac{1}{4}$ -inch thick are widespread. The remote head may be substituted directly for the standard camera-housed sensor. One such application for this type of system is in aircraft with limited windshield space, where a camera is required to view the forward scene, as well as the heads-up-display superimposed

thereupon. Any obstruction to the pilot's view is undesirable, so a 1-1/2 inch diameter sensor head represents a near-ideal solution.



FIGURE 8. MV201 CCD-TV CAMERA IMAGE

The MV201 is being incorporated in a camera system to be used for underground inspection in the event of a mine disaster. In this situation a hole is first bored into the earth to reach the site. A long 2-1/2 inch diameter cylinder containing the camera, coupled to a scan converter, is then dropped into the borehole at the end of a connecting cable which can be up to 24,000' long. Single frame slow scan video is then transmitted to a receiving site at ground level. Due to the possibility of explosions in this type of environment, a standard vidicon system, with its associated high voltage, cannot be used without a large diameter explosion proof housing. The CCD approach overcomes these limitations.

The objective of a recently initiated development program is to incorporate the MV201 concept into an artillery-launched system. This system will provide real-time observation of preselected areas using a parachute-deployed TV camera and RF link. The system makes use of the major components of the XM485 illuminating round for the 155 mm howitzer, in which the illuminant is replaced with a ballistically matched package comprising the CCD TV camera, battery, RF transmitter, and antenna. The TV pictures are received and displayed in real time on a monitor and simultaneously recorded on video tape. During the launch of the shell, the camera system must endure accelerations of 14,000 G's. A completely solid state image sensor is clearly needed for such an environment.

A two-camera system, similar to the previously mentioned Bore-sight Pair, can be used to generate video corresponding to two different views of the same object suitable for reconstruction as three-dimensional stereo display images. The applications for stereo TV are numerous, including the inspection and control of objects or vehicles in remote or hazardous areas. The additional circuit requirements for paired-camera operation are relatively modest; over 75% of the electronics can be shared.

LLLTV CAMERA DEVELOPMENT

An all solid state TV camera is being developed with features designed to extend the illumination-sensitivity threshold to sensor highlight levels of 2×10^{-5} fc (10^{-5} W/m², 2854°K). Camera design parameters are based on utilization of a 380 x 488 element image sensor. The element clock rate is 7.16 MHz, with a 30 frame/second rate. The composite video output signal is designed to be fully compatible with 525 line TV display and VTR equipment.

Preliminary evaluations of camera circuit concepts and LLLTV performance have been made using the 190 x 244 image sensor, which incorporates the same design principles as the larger 380 x 488 version.

The images of figures 9 and 10 were obtained by processing and displaying the output signal from the on-chip 12-stage distributed floating gate amplifier (DFGA)⁶. Output imaging was observed for an 8000/1 range of sensor highlight illumination. The sensor readout rate was 30 frames/second, simulating 380 x 488 operation. Figure 9 illustrates imaging of a high-contrast pattern consisting of test bar groups at 1/4 and 1/2 Nyquist-limit horizontal resolution. Pictorial scene imaging for the same device, at similar highlight signal levels, is shown in Figure 10. The image sensor highlight level equivalent to the 25 electrons/pixel/frame threshold condition is approximately 2×10^{-5} fc -2854°K.

Figure 11 illustrates the camera configuration to be employed. The sensor is enclosed in a hermetically-sealed region containing a thermoelectric cooling module. The cooling feature has been included to minimize the dark current and dark current noise effects which can limit image detectability at very low signal levels.

CONCLUSIONS

CCD area image sensors of the interline transfer type are being utilized in all solid-state TV cameras for applications where very small size, low power/low voltage operation, high sensitivity, and extreme ruggedness, are either desirable or mandatory system requirements.

The CCD-ILT sensors, particularly the 190 x 244 and 380 x 488 designs, have features which make these devices useful for many operating modes not feasible with other types of solid-state and beam-scanned image sensors. Operation at very high frame rates is feasible, since the line transfer rate is never required to exceed line readout rate. Low light level operation has been demonstrated at threshold levels corresponding to signal packets of the order of tens of electrons. The ILT organization is adaptable to multiplexed operating modes, one of which demonstrates image resolution element densities in excess of 66 pixels/mm; comparable with silicon-target beam-scanned image sensor performance. Also, these ILT sensors have a unique capability for accepting information from an electrical input register. These features, when fully exploited, may be expected to result in significant new applications for solid-state TV cameras.

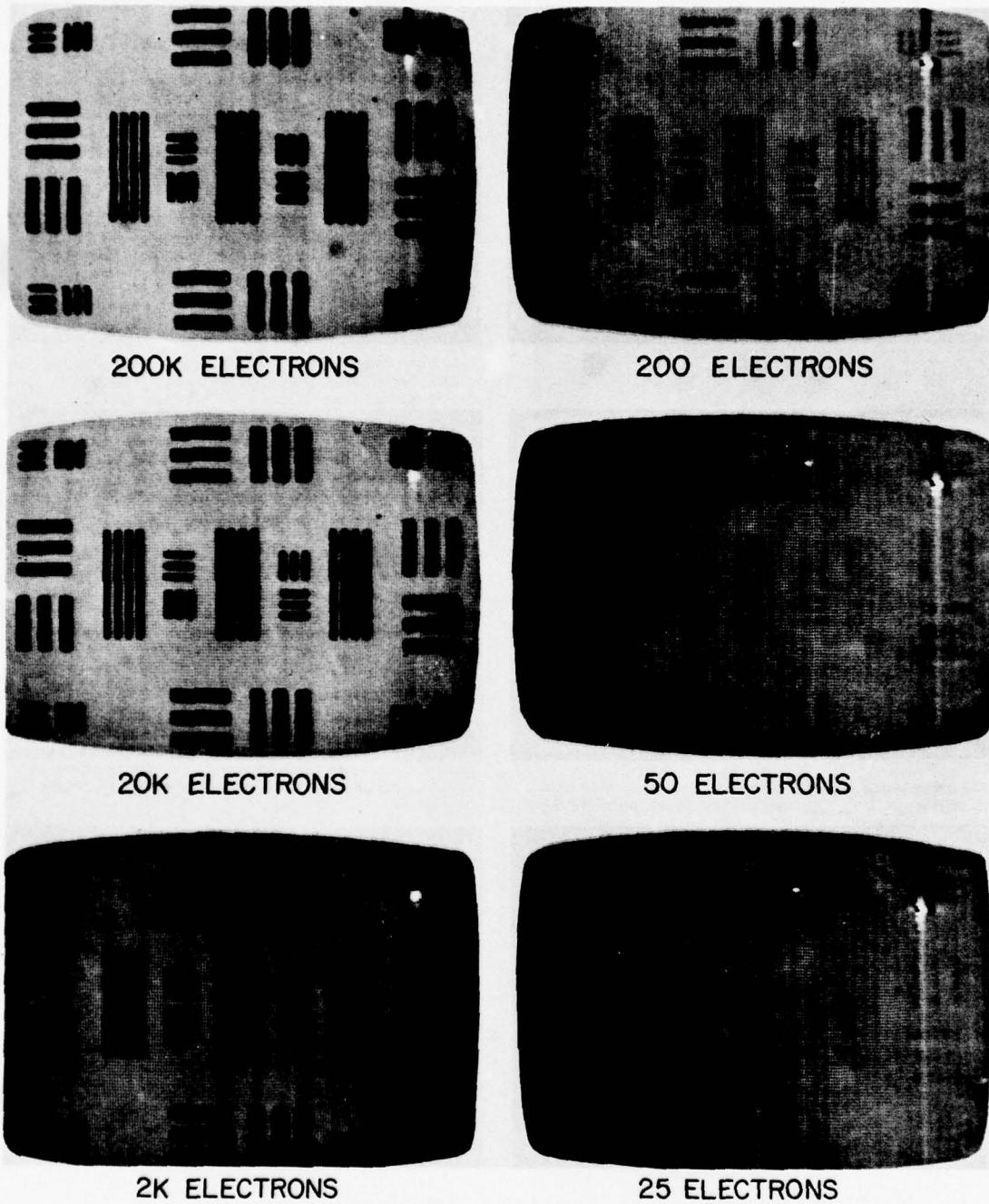


FIGURE 9. TEST BAR IMAGING WITH THE DFGA OUTPUT OF A 190 x 244 SENSOR
EXPOSURE TIME: 0.1 SECOND, TEMPERATURE: 0°C, 30 FRAMES/SECOND
ELECTRON COUNTS REPRESENT ELECTRONS/PIXEL/FRAME IN
IMAGE HIGHLIGHT REGIONS

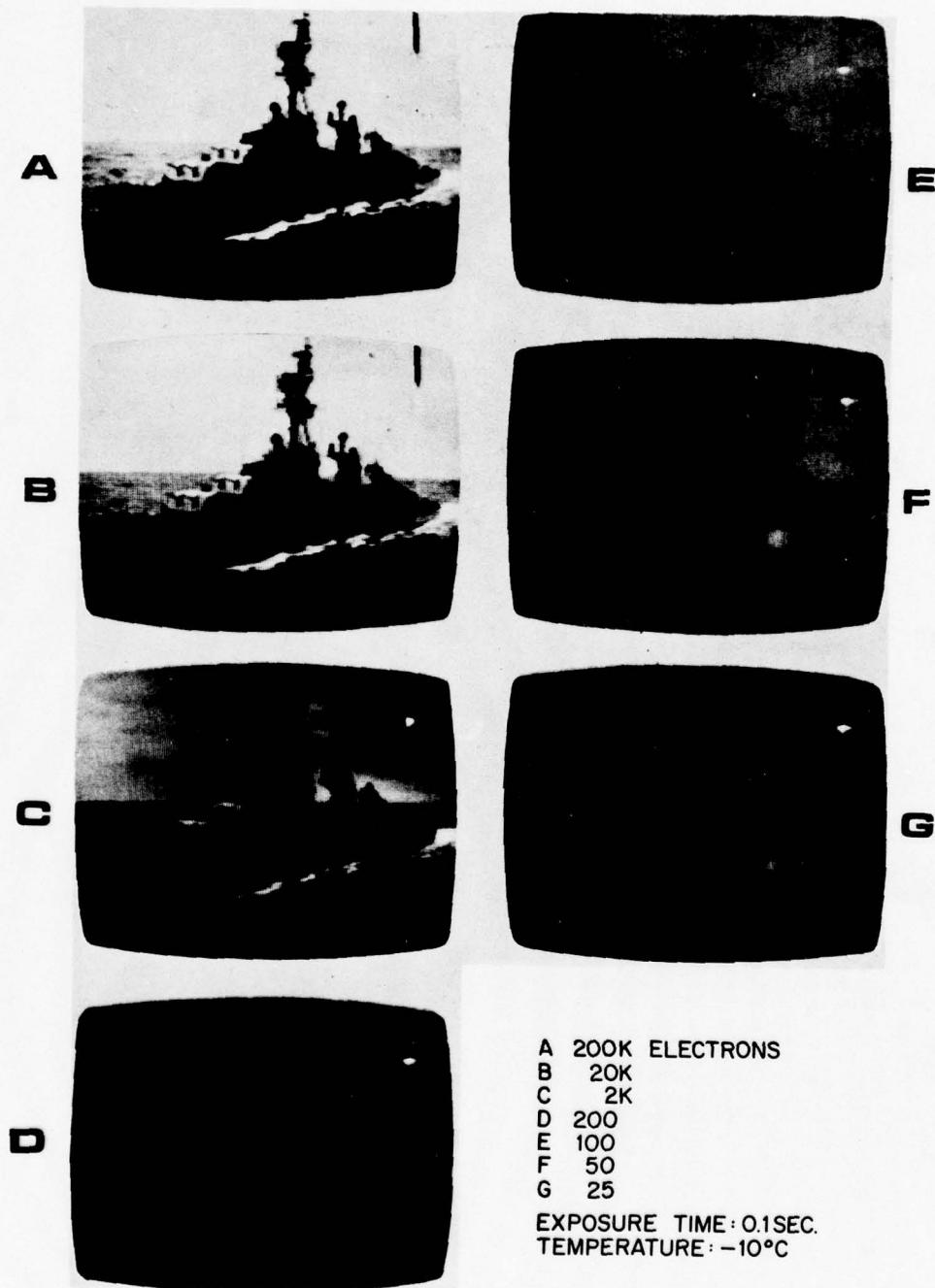


FIGURE 10. PICTORIAL SCENE IMAGING WITH THE DFGA OUTPUT OF A 190 X 244 SENSOR
ELECTRON COUNTS REPRESENT ELECTRONS/PIXEL/FRAME IN IMAGE HIGHLIGHT REGIONS

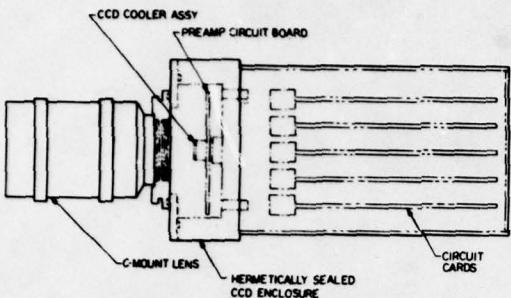


FIGURE 11. LLL-TV CAMERA CONFIGURATION

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DIVERSE ELECTRONIC IMAGING APPLICATIONS FOR CCD LINE IMAGE SENSORS

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ABSTRACT

The performance and operating characteristics of a family of Fairchild CCD line image sensors provides the basis for a variety of electronic imaging applications. Multi-chip, long line, and integrating mode line image sensor configurations are well suited to such diverse applications as high resolution aerial reconnaissance, facsimile page reading, mail sack label bar-code reading and low light level periscope scanning.

CCD line image sensors used in experimental imaging configurations for these applications were 1×500 , 1×1000 , 1×1728 , and 128×128 element devices. The 128×128 area device, included in this line image sensor category, is operated in a time delay and integrating mode (TDI). Results are presented of imaging performance for experimental configurations.

The real time aerial reconnaissance test configuration described consists of three 1×500 element devices using beam-splitting optics to achieve long line, gapless coverage of scene information. A nine-chip electronic imaging system using 1×1728 CCD devices and a low distortion, wide angle lens is also discussed.

The experimental page reading scanner employs a single 1×1728 array and lens to cover an $8\frac{1}{2}$ " page width format at a limiting resolution of 200 lines per inch. An automatic hand-held reader with a single 1×1000 element array rapidly scans and reads mail sack labels.

Experimental results are presented for a 128×128 multi-row TDI charge-coupled device in a moving image system. An experimental configuration for low light level periscope scanning is described and an example of reconstructed low light level imagery is presented.

INTRODUCTION

Newer forms of CCD buried channel line image sensors, i.e., long line and multi-row integrating arrays are enhancing performance of many all-solid state electronic line image applications. Specifically, a 1×1728 element long line device provides a substantial number of picture elements in a single chip at a resolution density approaching 2000 elements/inch. These features are essential in applications where high resolution performance is required in single-chip configurations or in higher resolution multi-chip configurations where high density, long line sensors minimize both the number of chips and the image format size required in the sensor system.

Another interesting CCD line image sensor, a 128×128 element multi-row device, provides additional signal integration compared to a conventional single-row sensor when a scene is scanned across its 128 integrating rows. This mode of operation, also called time delay and integration (TDI)¹, provides the signal-to-noise performance improvement to make it useful in low light level applications. Although the size of this initial device is only 128×128 in its present form, it can undoubtedly increase in the near future consistent with the 380×488 format sizes achieved in CCD area image device technology in development².

Several diverse electronic imaging applications are currently being investigated which use CCD long line and multi-row line image sensors to advantage:

- a wide angle aerial reconnaissance system where a large number of picture elements, e.g., 15,000, are required across the image format for high resolution performance.
- a page scanning system where a single-chip system configuration is required for 200 line per inch performance using $8\frac{1}{2}$ " inch page widths.
- a bar-code reading system where a single-chip configuration automatically reads a mail sack label code when positioned over a 2.3 inch long format.
- a submarine periscope viewing system where operation is required in both daylight and night sky environments.

This paper describes the laboratory test configurations and imaging results related to these applications. These projects were executed at the Fairchild Imaging Systems facility at Syosset, New York and were sponsored by various government agencies.

1 X 1728 LONG LINE IMAGE SENSOR

The 1728-element CCD line image array, described recently in the literature³, is a two-phase buried channel device with read-out registers and video amplifiers included on the chip. The element-to-element pitch is 13 μm , the element width is 16 μm , and all 1728 elements form a continuous unstaggered photo-responsive line.

The 1 x 1728 element CCD line image sensor consists of five functional elements, illustrated in the block diagram of Figure 1. These elements are:

- A row of 1728 image sensor elements, separated by diffused channel stops and covered by a polysilicon photoelectrode. The photoelements are shown at the center of the diagram.
- Two aluminum transfer gate structures, one on each side of the row of 1728 photoelements.
- Two 864-element, 2 phase, analog transport registers, one on each side of the line of photosensors. The transport registers are separated from the photosensors by the transfer gate.
- A charge detector and gated preamplifier⁴ which detect the charges delivered by the transport registers and convert them to a voltage output signal (video).
- A compensation amplifier which provides the capability of suppressing reset clock transients through an external differential amplifier.

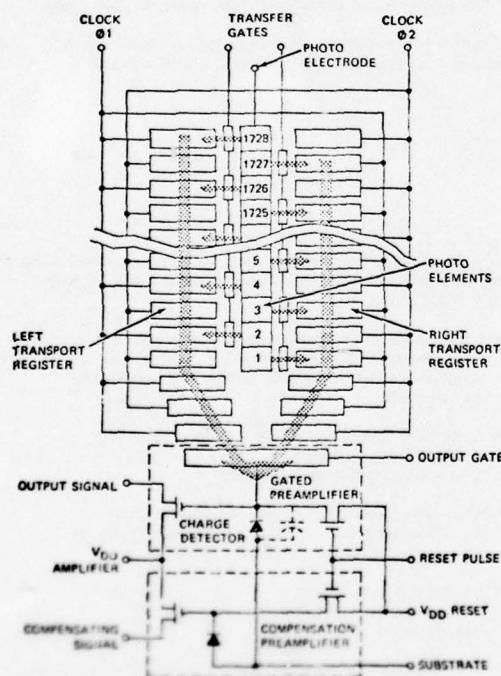


FIGURE 1. 1 X 1728 SINGLE-ROW (LINE) SENSOR

128 X 128 MULTI-ROW IMAGE SENSOR

The 128 x 128 element line image device is composed of an area-imaging array, an output register, and an amplifier section that incorporates two amplifiers. The central feature of the sensor is the area-imaging array which consists of 16,384 individual photosensor elements arranged in a 128 x 128 element format. The photosensor elements are also the unit cells of 128 vertical, 128-bit CCD registers as shown in Figure 2. Each 20 $\mu\text{m} \times 20 \mu\text{m}$ photosensor element is composed of two charge storage areas, two barriers, and a channel stop region.

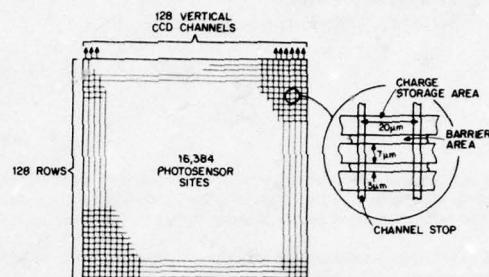


FIGURE 2. 128 X 128 MULTI-ROW SENSOR

The single-line output register receives charge from the area array via an output transfer gate. Two amplifiers, a gated charge integrator (GCI) and a low noise threshold floating gate amplifier (FGA)⁵, are located at the end of an extension of the output register.

The multi-row integrating array is used in a moving image mode⁶ where one direction of scan is provided by sensor or object motion. As shown in Figure 3 when the image is moved across the array (from Row A to Row B, etc.) charges developed in one row of potential wells (A_1, A_2, A_3 , etc.) are transferred in synchronism with the image motion so that at the end of the array rows (Σ) a substantial signal has been accumulated. The signal is transferred to the output register and is read out in the same manner as a conventional single-row (line) imaging array. The output register readout rate is greater than 128 times the column transfer rate to clear the output register before the next input of row data.

The multi-row array is analogous to a mechanical slit in a moving film camera. The electronic "slit" of 128 rows is 128 times greater than with a conventional single-row array thereby achieving an increase in exposure time, by a factor of 128 under the same system operating conditions.

AN ELECTRONIC WIDE ANGLE CAMERA SYSTEM

A multi-chip breadboard scanner and display unit was designed and fabricated to study optical butting when using simple beam splitter techniques to produce "seamless" pictures.

The breadboard arrangement used three CCD 1 x 500 line image sensors⁷, which have 1.2 mil center-to-center spacings, and a mirror arrangement to scan a scene across the array. The eventual electronic wide angle camera system (EWACS)⁸, to which the study was directed, may use nine or more 1 x 1728 line sensors operating in a pushbroom or panoramic mode to provide an approximate 15,000 line resolution performance.

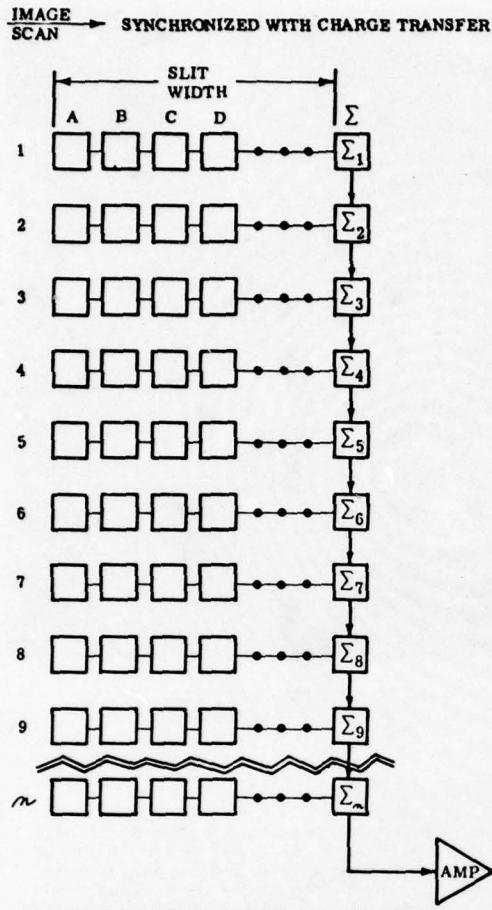


FIGURE 3. MULTI-ROW INTEGRATING LINEAR ARRAY SCHEMATIC

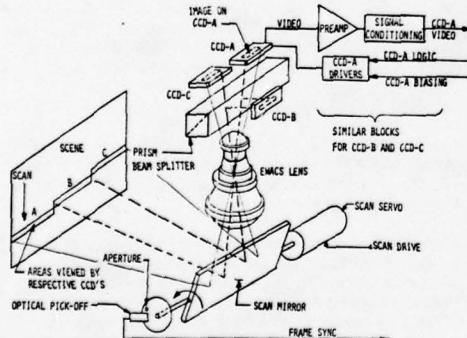


FIGURE 4. BREADBOARD SENSOR CONFIGURATION (EWACS)

SYSTEM DESCRIPTION

The EWACS laboratory demonstration sensor configuration shown in Figure 4, primarily consists of a special-design EWACS lens, a scan mirror, a beamsplitting prism, three optically butted 1 x 500 element linear CCD arrays, and associated electronics. A separate control and display unit provides logic, control functions, video processing, sweep generators and a CRT display. An additional commercial lens was also used for many of the breadboard tests.

A CCD channel selection control permits viewing imagery produced by either the 500 elements of one CCD or the beginning 250 elements and the end 250 elements of adjacent pairs of CCD's. The latter mode of operation permits viewing the optical butted sector, between the line image sensors, in the center of the CRT display.

A photograph of the optical butting section is shown in Figure 5. Major components of this unit are a beamsplitting prism, the CCD arrays, prism mount, and front end electronic components.

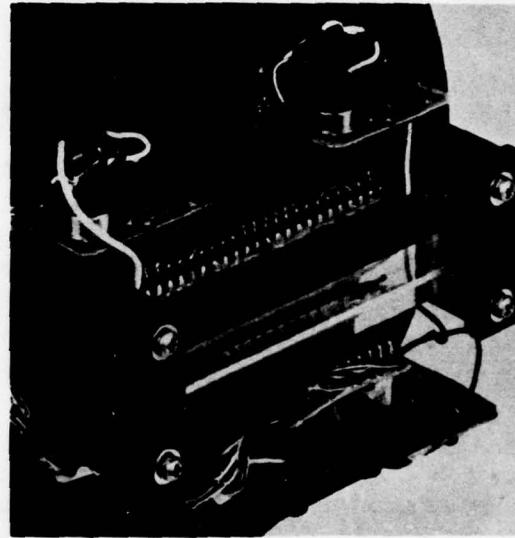


FIGURE 5. OPTICAL BUTTING ASSEMBLY (EWACS)

Multi-Chip Alignment

To facilitate accurate chip positioning, adjustments are incorporated into the breadboard optics. These adjustments enable focusing and butting alignments to be made while viewing the chips through the beamsplitter using a high power microscope. The three line arrays, cemented to individual base plates, form part of a six-degree-of-freedom adjustable mount. The chips are visually focused and butted to better than $\frac{1}{4}$ sensor element width. Adjusting screws for the two outboard chips are accessible from the rear so that final butting alignments can be made with the breadboard installed on the objective. The final adjustments are performed while viewing an oscilloscope and the system display monitor.

MULTI-CHIP IMAGING RESULTS

Figure 6 shows the results of combining the video signals of CCD arrays B and C on the display CRT. Photograph B represents the end 250 elements of the B array alone and photograph C shows the beginning 250 elements of the C array alone. The combined B and C photograph was taken with both arrays operating simultaneously.

The system limiting resolution, limited by the sensor geometry, corresponds to 16 line pairs per millimeter for the 1 x 500 element sensor.

The region of the displayed image where the array butt occurs is not readily detectable by viewing the Polaroid photograph of the displayed image.

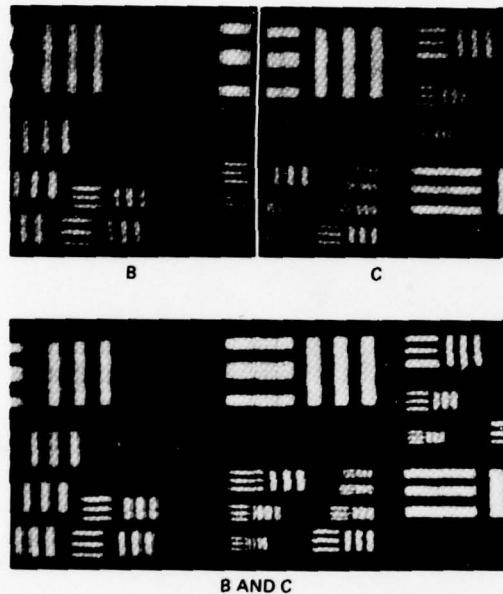


FIGURE 6. EWACS BREADBOARD PERFORMANCE (1 x 500 MULTI-CHIP SENSORS)

An example of aerial imagery using a single 1 x 1728 line image sensor is shown in Figure 7. The imagery was scanned from a film sample and reconstructed on a CRT monitor display. The maximum of 800 lines available on the CRT monitor display limits the output recording to approximately one-half of the 1 x 1728 sensor's resolution capability.

A PAGE SCANNING SYSTEM

A page scanning breadboard was designed and fabricated to demonstrate CCD linear array performance under conditions encountered in page reading and facsimile applications⁸. The initial breadboard scanned two 1 x 1000 arrays using twin lenses to achieve high resolution performance. The 1 x 1728 was subsequently developed to achieve the 8-1/2 inch page width coverage and the 200 line per inch resolution in a single-chip configuration thereby eliminating the need for the multiple lens arrangement and its associated alignment requirements.



FIGURE 7. MONITOR DISPLAY OF AERIAL SCENE (1 x 1728 SENSOR)

SYSTEM DESCRIPTION

In the test arrangement the scanned 8-1/2 inch width page was mounted on a carriage that was transported across the field of view of the array. The page is illuminated by a row of lamps that direct a uniform light band to the field of view of the array. The array and its relay lens are mounted on a separate carriage above the paper carriage.

A rotating cylinder test arrangement was also used for page scanning tests. The rotating cylinder, with a standard IEEE Facsimile Test Chart wrapped around it, inputs the image across the array's field of view. The video signals developed are amplified and reconstructed on a CRT display. The video readout rate was 1 MHz.

PAGE SCANNER IMAGING RESULTS

The limiting resolution for the array in the system coverage of an 8-1/2 inch page was 200 lines per inch which corresponds to the results of other investigators⁹. Figure 8 was taken with an expanded sweep CRT monitor.

Non-uniformity of response, largely determined in local areas by array aperture geometry control and from one end to the other (gradual variations) by non-uniformities in the polysilicon layer thickness, was approximately 5% of the mean output for the 1 x 1728 array when tested with uniform light input and without a lens. With the relay lens of the scanner included, the array response fell off gradually at the two ends of the line due to lens vignetting. The gradual variation in brightness of the recorded images, however, was found to be unobjectionable to the eye as compared to any sharp element-to-element variations.

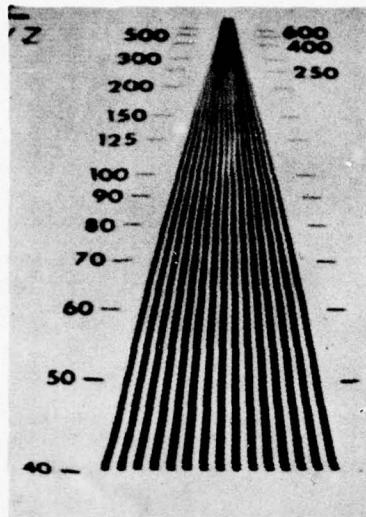


FIGURE 8. MONITOR DISPLAY OF RESOLUTION WEDGE (EXPANDED SWEEP)

Dynamic range of the 1 x 1728 page scanner sensor was measured to be 1000:1. A facsimile test chart recording from an 800 line CRT display screen is shown in Figure 9.



FIGURE 9. MONITOR DISPLAY OF IEEE FACSIMILE TEST CHART (1 x 1728 SENSOR)

A BAR-CODE READER SYSTEM

A developmental model automatic label reader was designed and fabricated to read destination bar codes on mail sack labels. The reading requires only that the operator position the hand-held scan head over the 2.3 inch long mail sack label instead of performing a manual scan as required with earlier reader equipment. The digital code read is transmitted to a computer which controls the sorting mechanism of a mail sack conveyor line.

SYSTEM DESCRIPTION

As shown in Figure 10, the developmental mail sack label reader is configured in a housing with a "pistol grip" handle. The reader system contains both a scan head assembly and an electronic interface assembly. Light source imaging optics, a 1 x 1000 CCD line array, array logic and driver circuits and video amplifier are in the hand-held scanhead assembly. The same scanhead is used for both stencil and computer code labels. The electronic interface assembly consists of an analog to digital converter, shift register memory and recognition logic. The output of the label reader connects compatibly with a decoder interface.

Indicator lamps mounted on the scanning unit are activated by logic circuits to alert the operator when the label is read successfully.



FIGURE 10. DEVELOPMENT MODEL MAIL SACK LABEL READER

SINGLE-CHIP IMAGING RESULTS

The analog output signal of the scanhead, when reading a barcode sample, is shown in the upper trace of Figure 11. This variable space code is converted to the digital signal shown in the lower trace of the photograph. The logic "0" correspond to the wide space and the logic "1" to the narrow space reading. Different samples of labels, i.e., using colored paper stock, stencil codes, computer codes, skewed patterns and degraded patterns (voids, ink variations) were successfully tested to an engineering specification. The throughput rate, i.e., the rate at which mail sack labels are picked up from a table, successfully read by the reader, and replaced on the table was measured at greater than 20 labels per minute.

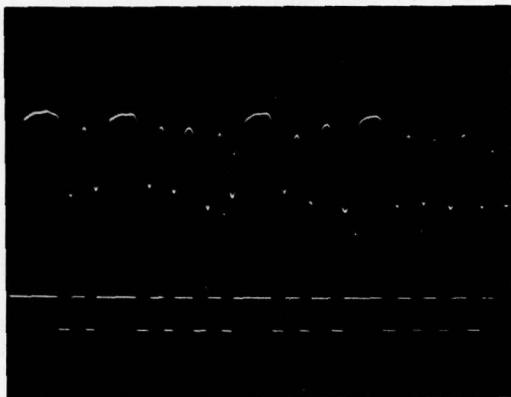


FIGURE 11. BAR-CODE VIDEO SIGNALS
(1 x 1000 SENSOR)

AN ELECTRO-OPTICAL DAY/NIGHT PERISCOPE SYSTEM

A breadboard periscope scanner, currently being designed and fabricated uses both a long line 1 x 1728 and a 128 x 128 multi-row integrating CCD sensor to demonstrate simulated day/night periscope electronic imaging performance. Table 1 lists the test instrumentation operating parameters.

TABLE 1
TEST INSTRUMENTATION PARAMETERS
TDI/HIGH RESOLUTION ARRAYS

Array	128 x 128	1 x 1728
Number of Elements	128	1728
Element Pitch	20 μm (.00079")	13 μm (.00051")
Focal Length	1"	3"
Vertical Angle	5.86°	16.77°
Scan Rate	18°/sec	37.3°/sec
Exposure Time	325 ms	260 μs
Lines per 180° Scan	3932	18547
Data Rate	10^6 elem/sec	6.9×10^6 elem/sec
Scene Irradiance/Brightness	3×10^{-9} W/cm ²	100 ft. lamberts

SYSTEM DESCRIPTION

The test instrumentation for demonstrating system sensor performance for the periscope application is shown in the block diagram of Figure 12. It includes a rotating table to simulate periscope scanning, controllable light source, lens, array sensors, array logic and drive circuits, signal processing amplifiers and image display equipment. The display equipment consists of both a direct CRT display with polaroid camera recorder and a scan converter for single frame storage and TV monitor display of the image at 30 frames per second. Each sensor, with its lens and control electronics, is interchangeable on the rotating table.

Clocking voltages used to transfer signal charges from row-to-row in synchronism with the image motion at the array plane of the 128 x 128 line sensor are derived from a shaft encoder coupled to the rotating table. Temperature control of the array, required to reduce dark current under low light input conditions, is provided by cooled dry nitrogen.

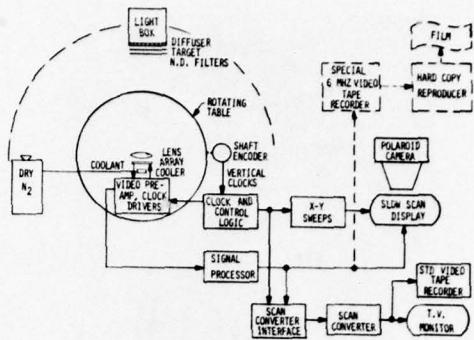


FIGURE 12. LABORATORY TEST ARRANGEMENT FOR PERISCOPE SYSTEM

A future version of the display and recording arrangements is designed to include a 6 MHz video tape recorder and a hard copy reproducer to reconstruct the images on high quality film.

MULTI-ROW SENSOR IMAGING RESULTS

Figure 13 shows a CRT polaroid recording of a high contrast tri-bar image made with a linear moving image target test configuration using a 128 x 128 multi-row image sensor. The tri-bar image easily resolved both orientations of tri-bars corresponding to the array's Nyquist limit.

The orientation and direction of the moving image as it traverses across the array to create charge summing is shown in Figure 14.

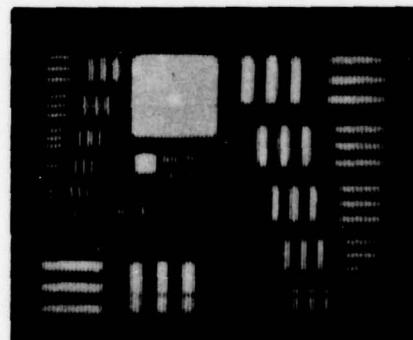


FIGURE 13. MONITOR DISPLAY OF TRI-BAR TARGET (128 x 128 SENSOR)

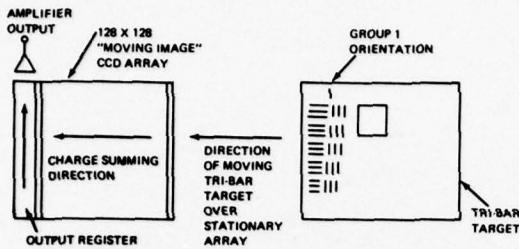


FIGURE 14. TARGET/SCENE ORIENTATION FOR MULTI-ROW SENSOR

Low Light Level Performance

The results of a low level test where the input highlight irradiance is 0.5% of the saturation irradiance is shown in Figure 15. The highlight signal level was equivalent to 1000 electrons and the noise level was 90 electrons rms. The highlight irradiance was measured as $16 \times 10^{-9} \text{ W/cm}^2$ at a 43 millisecond integration time where the source approximated a 2854°K black body radiator.

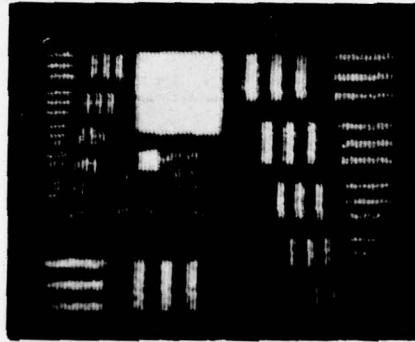


FIGURE 15. MONITOR DISPLAY OF TRI-BAR TARGET AT 0.5% OF SATURATION LEVEL

CONCLUSIONS

Although line image sensing systems have the drawback of requiring sensor or object motion to provide one direction of scan in electronic imaging configurations, they have an important role in many electronic imaging applications. Page reading and character reading¹⁰ have long been identified as major applications for line sensors but a review of the use of line sensors in different configurations, i.e., multi-chip, multi-row and long line single-chip arrangements shows that they can also address other high performance electronic imaging applications.

The four examples discussed are believed to be only a small sample of the potential areas of use for CCD line imagers. Development, for example, of very small, lightweight (less than one pound) remote surveillance systems and high speed facsimile (7 MHz data rate) are applications made possible by recent performance improvements made in CCD long line sensor arrays. Other new features recently added to versions of the long line arrays, i.e., electrical input registers, low noise floating gate amplifiers and electronic exposure controls are expected to expand their applications to a scope limited only by the creativity of the system designer. The future expansion of the multi-row sensor to larger-sized configurations with smaller sized photosensor cells is expected to increase its suitability to newer diverse line imaging applications.

ACKNOWLEDGEMENTS

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Charge Coupled Device (CCD) Analog Signal Processing*

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ABSTRACT

CCD basic building blocks provide a flexible approach to analog signal processing in systems. The Serial In/Serial Out (SI/SO) block provides time-base translation through electrically alterable time delay and recursive, programmable, filter-banks may be realized with the addition of PROM's or EAROM's (adaptive programming) to determine filter center frequency, bandwidth, and gain. The Parallel In/Serial Out (PI/SO) block may be used for time-division-multiplexing (TDM) of signals from a number of parallel channels into a serial data stream; and through the "delay and add" mode of operation, the PI/SO block permits sensor array beam forming and steering as well as convolution. The Serial In/Parallel Out (SI/PO) block provides variable tapped delay lines and transversal filters/correlators. Electrically reprogrammable analog weights combined with these building blocks offer adaptive filtering for communications. Combinations of the above linear or one-dimension blocks may be employed for Fourier transforming, filter banks and multiple correlators. Applications of CCD's are discussed for Radar, Sonar and Communication Systems.

1.0 Introduction

A simplification of the charge-coupled (CCD) analog shift register is shown in Figure 1. The timing is arranged so the switch toggling frequency is one half of the four-phase clock frequency. Thus, the input sampling switch, S_1 , alternately samples data and zero reference. At the output, switch S_2 clamps during zero reference, samples during data, and holds when it is not actually sampling. The output holding capacitor, therefore, contains only the "time-stretched" data samples. In a shift register having N pairs of stages, there will be N signal samples and N zero reference samples, each of duration $T/2$.

Figure 2 illustrates some key waveforms which are applied to the CCD analog shift register. The waveforms θ_1 through θ_4 are the four-phase clocks whose function is to propagate charges down the line without dispersion. Waveform S_1 demonstrates the switch functions; data is sampled in the up

position and zero reference is sampled in the down position. V_1 demonstrates the appearance of the delay line output voltage with the alternate data and zero reference outputs confined to $3/8T$. S_2 demonstrates the output processing functions: the data is sampled in the up position, the zero is clamped in the down position, and the data is held when it is not sampled (center). The interval from data sample to data sample is T and the total transport time is NT where N is the number of CCD analog delay line data stages. Thus, the signal delay for a serial in/serial out (SI/SO) CCD analog shift register is,

$$\tau = NT = N/f_c \quad (1)$$

which illustrates the electrically alterable delay feature of the CCD delay line.

* Sponsored in part by Naval Research Labs., Washington, D.C.

Since the Shannon Sampling Theorem requires the analog signal to be sampled at least twice during its period we may write,

$$f_s \leq 1/2T = f_s(\max) \quad (2)$$

and the time-delay signal bandwidth product becomes,

$$\tau f_s \leq N/2 \quad (3)$$

The low frequency limit is set by the thermal leakage current which accumulates in each stage, and the upper frequency limit is determined by input injection limitations and transfer efficiency.

Figure 3 illustrates a cross-section of a four-phase electrode CCD with transfer and storage electrode dimensions. The CCD is fabricated with PMOS silicon-gate technology and the insulator is a dual dielectric comprised of silicon nitride (Si_3N_4) over thermal silicon dioxide (SiO_2). The electrodes are fabricated with polycrystalline silicon and aluminum, to give coplanar but overlapping electrodes. The overlapping electrode feature provides a "sealed" CCD surface and stable operation over temperature-bias excursions.

2.0 Signal Transport in a CCD

The CCD delay line^{2,3} provides a unidirectional transfer of signal charge $q_s(x,t)$ from one storage cell to another adjacent cell. The signal charge is designated in cell x at time t , where x and t assume integer values; i.e., the unit of distance is the cell-to-cell separation X_0 (center-to-center), and the unit of time is the stepping interval T (clock period).

The frequency response of the CCD delay line may be calculated from a discrete frequency expression for the signal charge:

$$q_s(x,t) = \epsilon q_s(x,t-1) + (1-\epsilon) q_s(x-1,t-1) \quad (4)$$

where ϵ is the transfer inefficiency per stage delay with typical values of $\epsilon \leq 10^{-4}$ for $f < 1 \text{ MHz}$. Since equation (4) is a discrete set of signal values in the time domain, we may transform the signal charge to the Z-domain:

$$Q_s(x, Z) = Z^{-1}[\epsilon Q_s(x, Z) + (1-\epsilon) Q_s(x-1, Z)] \quad (5)$$

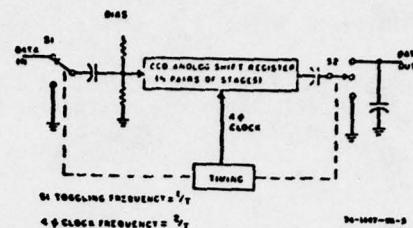


Figure 1. Charge Coupled (CCD) Analog Shift Register

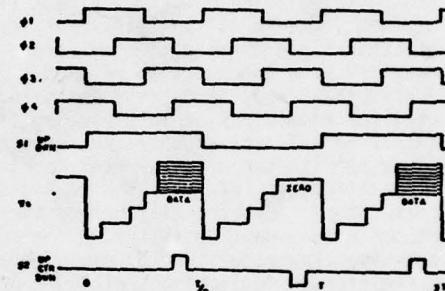


Figure 2. Basic CCD Four-Phase Clock Timing

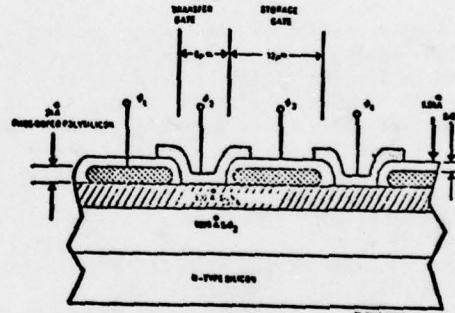


Figure 3. Cross-section of Four-Phase CCD Stage Delay

The transfer function of a N-stage CCD delay line becomes

$$H(z) = \frac{V_{out}(z)}{V'_{in}(z)} = \frac{\epsilon_m R_F C_{in}}{C_{out}} \left[\frac{1-\epsilon}{1-\epsilon z^{-1}} \right]^N z^{-N} \quad (6)$$

and the substitution of $Z = e^{j\omega t} = e^{j2\pi f_s/f_c}$ into equation (6) yields the amplitude and phase characteristics shown in Figures 4 and 5, respectively, for various values of $N\epsilon$. The signal frequency, $f_s \leq 0.5f_c$, as restricted by the Shannon Sampling Theorem, which states that a band-limited signal, f_s , may be reconstructed from samples taken at time intervals $T = 1/f_c$. The phase deviation $\Delta\phi(f_s)$ is the departure from linear phase shift. The insertion loss of the CCD delay line is less than 2 dB at the Nyquist limit ($f_s = 0.5f_c$) if $N\epsilon < 0.10$ and the maximum phase deviation at $f_s = 0.25f_c$ is less than 3°.

2.1 Frequency Dispersion

This dispersion can be viewed in the frequency domain as a shift in the filter response frequency with the maximum shift at one-half the clock frequency.

$$f'_s = f_s + \frac{\epsilon f_c}{2\pi} \left[\sin \frac{2\pi f_s}{f_c} - j(1 - \cos \frac{2\pi f_s}{f_c}) \right] \quad (7)$$

2.2 Amplitude Dispersion

The signal is "dispersed" or spread-out in time as a result of the finite transfer inefficiency ϵ and the number of cells, N . The dispersion of a single data sample of unit height (i.e., one propagating storage cell through the delay line) may be determined by the binomial expansion theorem:

$$[(1-\epsilon) + \epsilon]^N = \sum_{t=0}^N \binom{N}{t} (1-\epsilon)^{N-t} \epsilon^t \quad (8)$$

$$= \sum_{t=0}^N q_s(N, t)$$

$$\binom{N}{t} = \frac{N!}{t!(N-t)!} \quad (9)$$

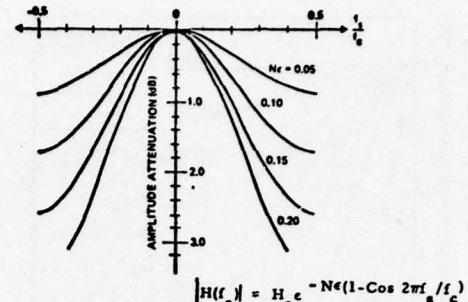


Figure 4. Amplitude attenuation characteristics as a function of f_s/f_c for various values of $N\epsilon$.

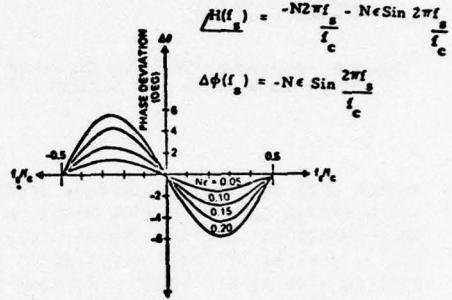


Figure 5. Phase Deviation as a function of f_s/f_c for various values of $N\epsilon$.

Figure 6 illustrates the effect of $N\epsilon$ product on the shape of a single data sample of unit height. The total area under the output waveforms is identical to the area under a single sample at $\epsilon = 0$. The peak of the signal lags by one clock period when $N \approx 1/\epsilon$ and dispersion is minimal for $N\epsilon \leq 0.10$.

3.0 CCD Basic Building Blocks for Discrete Analog Signal Processing (DASP)

Any signal processing system that involves the linear transformation of analog signals such as correlation, discrete Fourier transformation (DFT), filter banks, matched filters, multiplexing/demultiplexing, array scanning, orthogonal scan transformation, time base translation, etc., can be realized with combinations of CCD basic building blocks. In discrete analog signal processing (DASP),

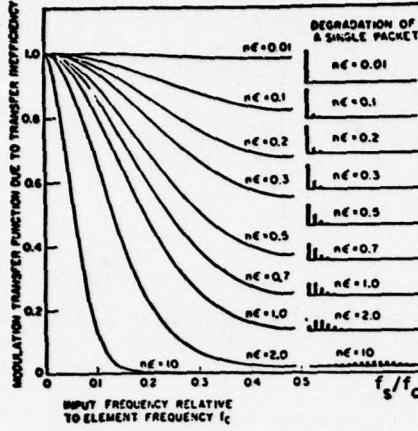


Figure 6. Degradation (Amplitude Dispersion)⁶ of a Single Charge Packet as a function of Ne .

analog data samples are stored, transferred, and operated upon by analog means, whereas in conventional digital signal processing (DSP), digital or quantized samples are handled with binary logic. A major advantage of DSP is retained by DASP, namely the precise transport delay, particularly in relation to coherent signal processing. The dynamic range of an analog bit in DASP may be thought of as composed of 6-dB equivalent DSP digital bits. Thus, a typical example of 100 Stage ($N = 100$) CCD delay line with 60-dB dynamic range and transfer inefficiencies of $\epsilon \sim 10\%$ at 1-to-2 MHz clock rates will have an overall signal degradation of 1 percent (i.e., less than 0.1-dB insertion loss) without the need of A/D conversion.

One-dimensional basic building blocks⁷ (linear arrays) may be classified according to the characteristic information flow patterns:

- (1) Serial in/Serial out (SI/SO)
- (2) Parallel in/Serial out (PI/SO)
- (3) Serial in/parallel out (SI/PO)

These fundamental linear arrays may be combined to form area arrays (2-dimensional matrices) with increased signal processing

capabilities. Table 1 provides a partial listing of applications for these basic building blocks.

Table 1

Basic Information Flow	
Serial In:	Parallel Out (SI/PO)
Serial In: Serial Out (SI/SO)	Parallel In: -Nondestructive Sensing Taps - Weighted Unweighted
Pure Delay: Time Base Interchange	Transversal Filtering; Correlation/Convolution; Adaptive Filtering; Sampled Data Smoothing or Interpolation [Scan Format Converter]
Array Configuration	Beam Focusing; Focus Scanning Multiple Beam Forming; Beam Steering
Linear	Corner Turn (Orthogonal Scan Trans- formation)
2-d Matrix (Area)	Built Serial Analog Storage*
	Built Serial-Parallel Serial (SPS) Analog Storage*

*As For Video Refresh Memories

3.1 Serial In/Serial Out (SI/SO)

The SI/SO block is a simple CCD shift-register with the characteristics discussed in sections 1 and 2. In a linear array configuration the SI/SO block provides pure analog signal delay with the ability to provide time base translation. Typical dynamic range for present-day SI/SO blocks is 60-80dB with ± 1 percent linearity and clock frequencies from 1KHz-1.0MHz for a 64 analog bit delay line. The clock requirement may vary from device to device with voltages varying from TTL to MOS compatible. In general, MOS-type voltage swings are needed to obtain dynamic range and frequency response. The capacitance loading for the drivers is typically $0.2\text{pF}/\text{mil}^2$ of active bit area; for bit areas of 1.5 mil^2 we have $0.3\text{pF}/\text{analog bit}$. Thus, a 64 bit delay line will offer a loading of $\sim 20\text{pF}/\text{driver}$. In general, CCD

structures have not been built with interface/buffer circuits on the chip because of the advanced development nature of the work; however, CCD chips can be fabricated with MOS, CMOS, or bipolar interface circuits. In order to test SI/SO blocks without on-chip buffer circuits, a so-called "open collector" driver may be employed. This driver is relatively inexpensive and provides clock voltage swings of 30V up to 2 MHz clock frequencies. Clock shaping may be accomplished if desired by the use of a series resistor, which also protects the drivers in the pull-down transient. A CCD chip should have protective resistor/diode combinations, similar to MOS-type circuits, to limit the displacement current and prevent shorting of the input electrodes.

For analog signal processing, as discussed in the introduction, a desirable feature is the incorporation of an a-c zero reference between successive signal samples, particularly for PI/SO and SI/PO blocks. In addition, sample and hold techniques are required for analog signal reconstruction which attenuates the response with a

$\frac{\sin \pi f_s / f_c}{\pi f_s / f_c}$ shape factor. The input to a

CCD may also be filtered with a $\frac{\sin \pi / \Delta t f_c}{\pi / \Delta t f_c}$

roll-off where Δt is the sampling window aperture. The output after sample and hold requires filtering with a low-pass filter with ideal "brick-wall" cut-off at $f_c / 2$, the Nyquist limit. Figure 7 illustrates an analog output swept frequency response of a CCD SI/SO block with sample/hold and a 7-pole Butterworth filter (-3dB @ 750 KHz) to filter the clock and limit the aliasing of frequencies higher than $f_c / 2$. Thus, in a properly designed CCD Analog Delay Line the frequency response is limited by the sample/hold and low-pass filter characteristics.

A time multiplexed CCD filter bank¹ which used SI/SO blocks is shown in the block diagram of Figure 8. The Filter-Bank Characteristics are illustrated in Figure 9 for the case of uniform filter spacing. Storage and sequencing of the constants is accomplished digitally using programmable read only memories (PROM) or electrically alterable ROM's (EAROM's). Weighting of the analog signals by the filter constants

is accomplished by means of multiplying digital-to-analog converters. The serial output data is multiplexed onto N lines by the output sampler which stretches each sample to a width, $T = NT$. Timing circuitry provides the CCD clock waveforms, the PROM addresses, and the sampler address. Applications of this filter bank include Doppler spectrum processing in radar, sonar and communications systems with advantage of low total part count combined with variable filter parameters.

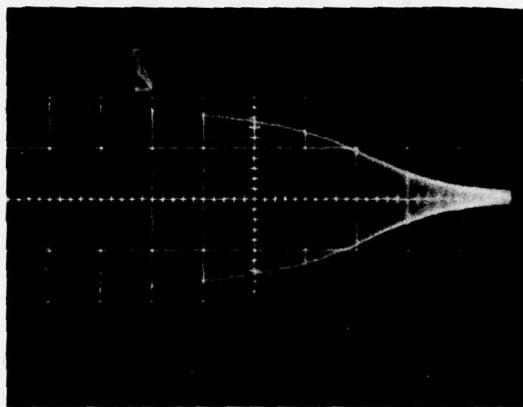


Figure 7. Frequency Response of Sampled Data CCD Analog Delay Line. 100 KHz/Div. Horizontal, $f_c = 2.0$ MHz. Transfer efficiency $e(f_c = 2.0$ MHz) = 2×10^{-3} for $L = 12\mu m$ electrodes. Sample/Hold and Filter Responses are included in the overall response.

The main signal processing function in a moving target indicator (MTI) radar is the main beam clutter (MBC) canceller. A three pulse canceller using CCD's is illustrated in Figure 10. Each delay line contains a number of range cells (or bins) adequate for the required resolution and range coverage. Low pulse repetition frequencies (PRF's) with interpulse periods (IPP) of 0.5 to 5 milliseconds are used to provide unambiguous range detection. The delay in each CCD shift register for a given range cell is one IPP. In MTI radars with more than 500 to 1000 range cells, the CCD shift register may be arranged in the serial-parallel-serial (SPS) configuration to minimize the effects of charge transfer inefficiency. The dual sampling scheme of figures 1 and 2, then automatically

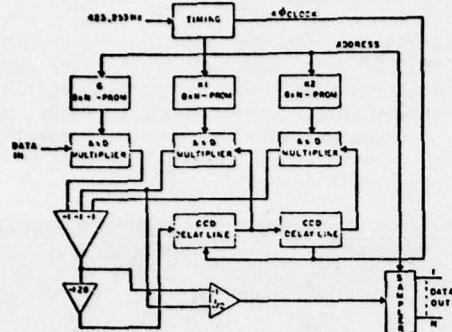


Figure 8. Block Diagram of N-channel CCD Filter Bank¹

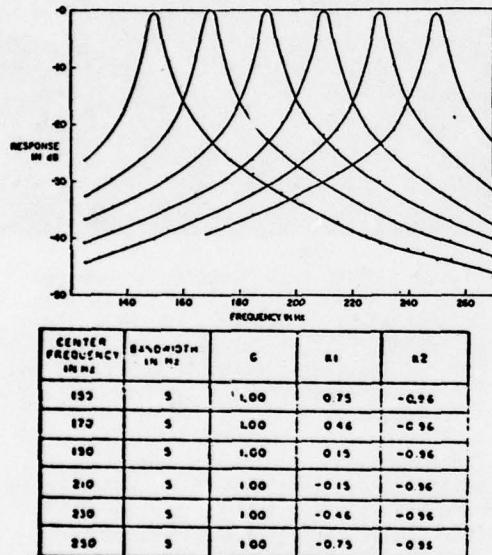


Figure 9. Uniform Filter Characteristics¹

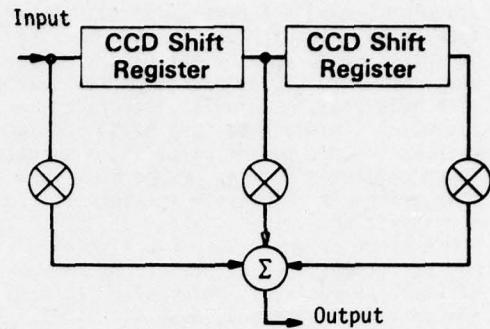


Figure 10. CCD Clutter Canceller for a Moving Target Indicator (MTI) Radar

eliminate most effects of leakage current nonuniformities since both "signal with reference" and "reference only" samples follow identical paths.

3.2 Parallel In/Serial Out (PI/SO)⁸

The PI/SO block may be used to time division multiplex a number of low data rate signal channels into a higher date rate output channel. The variations in electrical input may be minimized with the use of a stabilized charge injection circuit. An N-channel multiplexer converts N parallel input channels into a single-channel pulse amplitude modulated (PAM) signal. The input signals are synchronously sampled and the sampler information is entered into a unique spatial and temporal position in the CCD delay line. Applications include the multiplexing of many sensor input channels (e.g. electro-optical sensors, acoustical sensors) into a single video output channel. Figure 11 illustrates a photomicrograph of a PI/SO CCD chip with stabilized charge injection and parallel injection of alternate stage delays along the CCD delay line to minimize interchannel cross-talk and provide for the injection of an a-c reference for threshold voltage cancellation. Figure 12 illustrates the response of a PI/SO block with N = 20 and a simultaneous unit impulse at each parallel input. The injection of a reference and a signal and reference permits subsequent subtraction at the CCD output to remove input variations. Voltage variations, referenced to the input, not exceeding 100 μ V

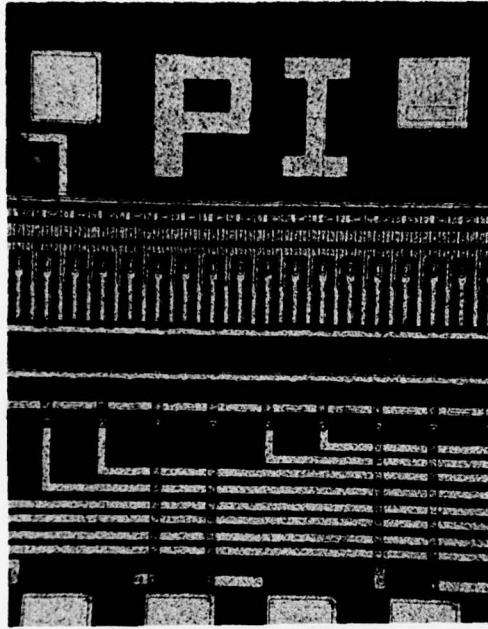


Figure 11. Photomicrograph of PI/SO CCD Basic Building Block.

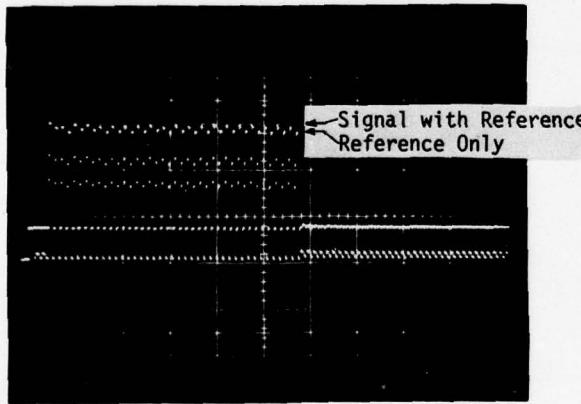


Figure 12. Impulse Response for Uniform Weighting Prior to Subtraction of Signal and Reference and Reference Inputs.

have been obtained to remove fixed pattern noise and place the limitation on noise with the charge injection uncertainty associated with the input capacitance.

The PI/SO block may also be operated in the time delay and add or integrate (TDI) mode to give such signal processing functions as sonar beam forming and steering or convolution. Formation of sonar or any acoustic beams using an array of transducers is illustrated in Figure 13.

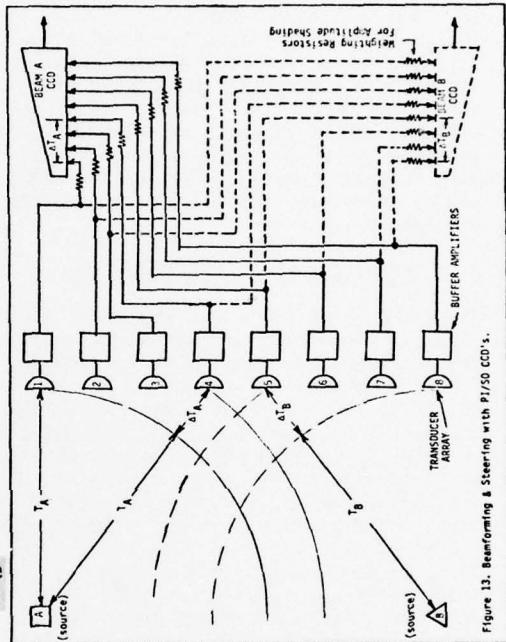


Figure 13. Beamforming & Steering with PI/SO CCD's.

Transducer "1" is first to receive the signal from source A which is suitably weighted and injected into the "Beam A" CCD, where it is delayed. The signal next arrives at transducer "2" and is weighted accordingly. When it is injected into "Beam A" CCD, the weighted signal from transducer "2" is added to the weighted signal from transducer "1". As the signal from source A arrives at each transducer in turn, it is weighted, injected into the "Beam A" CCD, and added to the previously accumulated signals that were injected and delayed from the closer transducers. The output charge integrated in any charge packet during transit through the "Beam A"

CCD may be written

$$Q_{out}(t) = \sum_{k=1}^N V_k(t-kT) \cdot W_k \cdot C_k \quad (10)$$

where W_k = k^{TH} weighting coefficient, C_k = k^{TH} input capacitance, $V_k(t)$ = signal from k^{TH} transducer, T = CCD clock time.

[Note: A common signal source applied to all weighting resistors, i.e., $V_k(t) \equiv V(t)$ for all k , gives a convolution of the signal $V(t)$ with an impulse response function determined by the quantities $(W_k \cdot C_k)$.] Although the use of the PI/SO block in the TDI mode typically involves a progressively larger charge packet as the packet propagates from the initial input to the final output, such an approach has some advantages over the use of the SI/PO block for the same functions: ease of fabrication and yield, interface simplicity, and lower power dissipation.

3.3 Serial In/Parallel Out (SI/PO)

The SI/PO block features INDEPENDENT nondestructive, low-impedance voltage readouts of the analog signals at specified locations or taps corresponding to various delays through the CCD shift register. In general, the signal voltage at each tap may be multiplicatively weighted by conductance to give a current proportional to the PRODUCT of the signal voltage by the weighting conductance. Summation of the product currents provides such functions as transversal filtering, correlation, or sampled data smoothing/interpolation for line arrays. Two dimensional weighting matrices driven by the independent low-impedance taps of the SI/PO block can give discrete Fourier transformers, filter banks, or multiple cross correlators. Figure 14 illustrates a photomicrograph of a SI/PO block ($N = 20$ outputs) which uses a floating clock electrode sensor at alternate stage delays along the CCD delay line. This permits the use of a "reference-only" and "signal and reference" to compensate for nonuniformities in the SI/PO structure. Figure 15 shows the tapped output signal from the SI/PO block. Numerous taps with multiplicative analog weighting can be accommodated without signal amplitude degradation due to stray parasitic capacitance, by paralleling SI/PO blocks of feasible size due to the summation of product currents. Furthermore, the independent nondestructive

voltage taps of the SI/PO block can provide the analog voltage signals needed by multipliers to give CCD real-time analog correlation. Use of programmable conductances such as the nonvolatile MNOS type or conventional MOS type permit such device applications as adaptive transversal line equalizer or programmable matched filter (or correlation detector) for secure voice/data communications systems

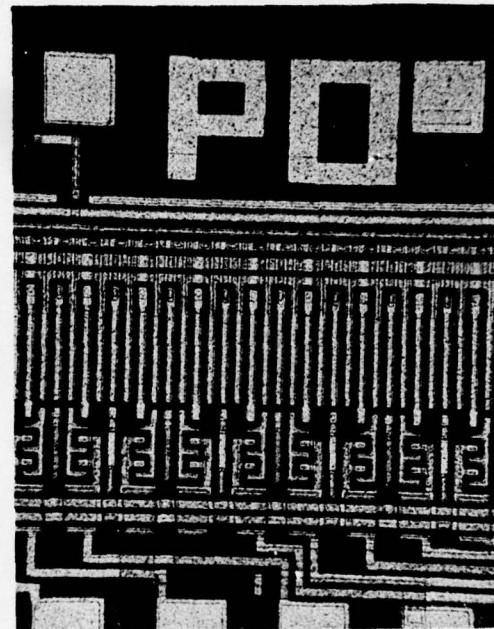


Figure 14. Photomicrograph of SI/PO CCD Basic Building Block

4.0 Conclusions

Many signal processing systems which involve the linear transformation of analog signals, such as matched filters or multiplexing/demultiplexing, can be realized with a finite number of CCD basic building blocks. To impact future electronic systems, the CCD basic building blocks should be flexible in the sense that systems design engineers can use them in a variety of applications. Thus independent unweighted taps keep the active device relatively simple yet require the use of external resistors and output buffer/reconstruction circuitry for trans-

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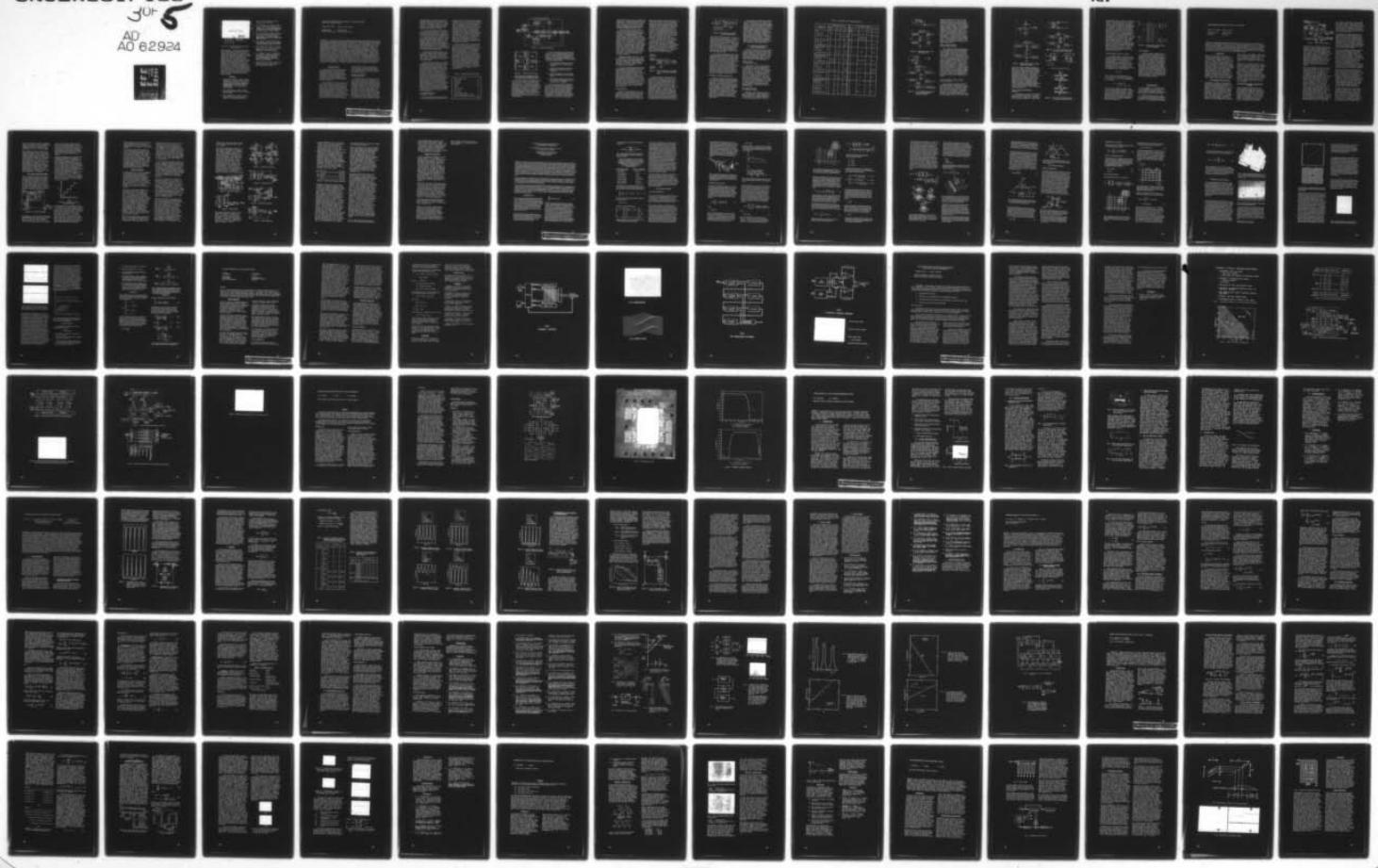
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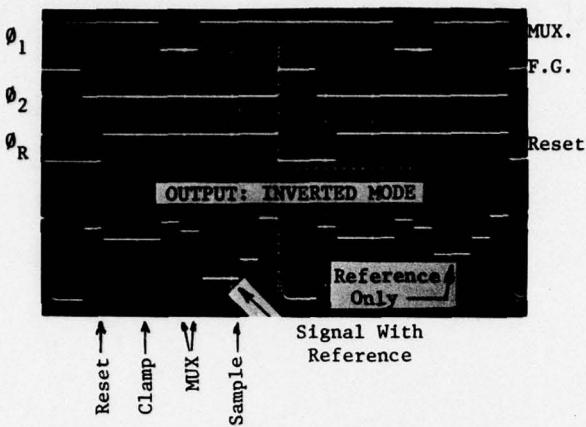


Figure 15. Floating Clock Electrode Sensor for SI/PO Block

form operations. But the main advantage is that a single device design may be used to satisfy many applications requirements. In systems where the external resistors are too clumsy, but tap weight adjustment is desired, electrically alterable tap weights are appropriate. This is clearly the most powerful method of tap weighting, which can lead to real-time analog correlators and/or adaptive filtering as well as tap error compensation. Devices having electrically alterable taps are substantially more complicated than fixed tap or unweighted devices but can be used as universal filter/correlator building blocks. Such universal blocks can benefit from the economics of high volume production and find diverse applications ranging from one-of-a-kind R and D to production systems.

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APPLYING THE CONCEPT OF A DIGITAL CHARGE COUPLED DEVICE ARITHMETIC UNIT

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ABSTRACT — Recent discussions have highlighted some of the computational potential of CCD implementations in the digital domain, and some note has been taken of the possibility of applying this potential to a few specific situations.⁽¹⁾ This paper explores the concept and application of a digital CCD arithmetic unit consisting of an arithmetic chip which is electronically reprogrammable to allow the chip to perform a variety of functions. The arithmetic chip contains four multipliers, three adder/subtractors, and a variety of selectable delays and signal routing paths. In discussing the configuration of this chip, the importance of technology items such as yield and general producibility as well as practical items such as pin count and package size is considered. The use of this arithmetic unit in any system is totally dependent on the proper interfacing. As part of this concern, the proper timing of input signals (such as data and multiplier coefficients) and output signals is treated, and it is shown that the internal chip timing requirements can generally be made compatible with anticipated system usage. A detailed discussion is given of the arithmetic unit configuration needed to realize a single-pole recursive filter, a nonrecursive digital filter, a single zero digital filter, and two filter sections useful for voice processing systems. This work has been supported in part by the Naval Research Laboratory, Naval Electronics System Command, Contract No. N000-14-74-C-0068.

INTRODUCTION

The use of charge coupled devices in the digital domain has been receiving increased attention. The digital characteristics of high noise immunity and independence from individual device parameters and parameter variations in combination with the high density implementation capabilities of CCD's make an attractive concept.

In this paper we first discuss a few of the basic constraints that are important in any realistic attempt to employ this concept. Next, we give a brief review of the makeup of a reprogrammable arithmetic unit chip that is capable of being electronically reconfigured so as to perform a number of useful functions. The following section describes the nontrivial considerations associated with properly programming such an arithmetic unit and shows how maximum use can be made of the inherent

CCD features. The final section illustrates the wide range of capabilities of this arithmetic unit chip by discussing in some detail several of the functional forms the chip can assume.

SOME FUNDAMENTAL CONSIDERATIONS

Before discussing any particular CCD chip configuration, it is worthwhile to reflect on some of the basic limitations and constraints that appear to exist with today's technology. First, CCD's operate not as wideband amplifiers like conventional MOS or bipolar circuits but on a charge transfer principle. To form a digital adder, several charge transfers must occur before the carry from the least significant bit is available as an input to the next most significant bit. In a 16-bit adder, for example, this operation must be repeated 16 times. To compensate for this, pipelining is used to provide an acceptable speed of operation.

The addends are stored in parallel shift registers with the delay increasing from the least significant bit to the most significant bit. This allows additions to be performed at a rate determined by the delay through 1 bit of addition rather than the delay through the total of 16 bits.

The need to operate CCD arithmetic circuits in a pipeline fashion to attain good speed performance imposes a constraint on the functions which can be realized with CCD LSI. Functions which inherently are of a streaming nature (e.g., the FFT) are best suited to the pipeline approach. Pipelining also implies that a number of shift register stages must be included in the implementation of arithmetic functions to equalize the delay between least significant and most significant bits. Fortunately, shift registers are one of the most efficient functions in terms of chip real estate which can be implemented with CCD's.

The maximum producible size of an LSI chip presents a fundamental limitation to the CCD configuration. With present technology, a square chip 150 mils on a side would be considered small to medium size, while a chip 300 mils on a side is considered large.

One of the most important constraints in configuring CCD chips is the limited number of package pins available. The pin limitation constraint is acutely felt when partitioning the digital functions for implementation with CCD's. Every effort is made to make the digital function or functions complete on a single chip. If the function is split between two chips so that two input and two output lines are needed with 16-bit parallel arithmetic, all of the 64 pins available with standard packages would be used for interconnections with none left for power and ground or control signals. One solution to the pin limitation problem is to time multiplex the input/output signals on the same set of pins. The chip timing must be carefully designed from an overall system viewpoint to assure that all of the time multiplexed signals from several chips appear in the correct sequence.

A REPROGRAMMABLE ARITHMETIC UNIT

By incorporating the characteristic of reprogrammability in an arithmetic unit,

a large number of useful signal processing functions can be performed with a relatively small number of computational functions. This is particularly true when it is possible to rearrange the interconnection of these few functions at will. One such situation has been studied recently and has resulted in a concept for a digital CCD arithmetic chip. This concept allocates to a single chip some important arithmetic functions such as addition/subtraction and multiplication. In fact, it can be shown that, by including three such adders/subtractors, four multipliers, and a few delay stages and signal routing gates, an impressive list of signal processing functions can be performed.

Figures 1 and 2 show the interconnection of these functions and the proposed layout for such an arithmetic unit. Note that the chip combines the multipliers and adders with the necessary control gates, inverters, and delays. The estimated overall chip dimensions are 350 x 300 mils. The total active area of the chip is considerably less, and it is probable that this design could be produced with reasonable yield. (This size estimate is based on 7.5 micron photolithography, two-level metal interconnections, and a standard two-phase overlapping gate CCD design.) Table 1 lists the pin usage for the chip, and shows that 64 pins are required for the configuration of Figure 1. The details of programming the arithmetic unit are discussed next.

Table 1. Arithmetic Unit Pin Usage

Power and ground	5
Data input	16
Multiplier	16
Output	16
Clock	1
Clock inhibit	1
Sync (+5)	1
Accumulator clear	2
Control functions (e.g., FFT add or accumulate filter modes)	6
	64

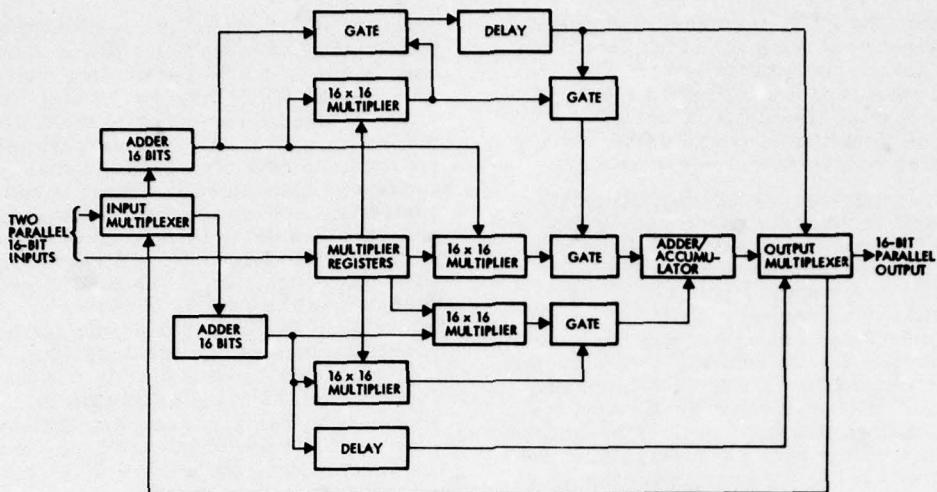


Figure 1. Arithmetic Functions

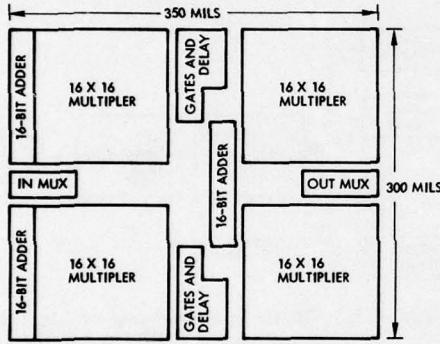


Figure 2. Arithmetic Unit Layout

PROGRAMMING CONSIDERATIONS FOR THE CCD ARITHMETIC UNIT

The utility of the CCD arithmetic unit depends on our ability to reconfigure the chip to perform various functions under program control. Compared to present microprocessors, the CCD arithmetic unit packs five to ten times the computational capability in a single chip. However, due to the fixed layout and the input/output (I/O) limitations imposed by packaging, the CCD arithmetic unit provides less programming flexibility than an array of microprocessor chips with equal computational capacity.

The reconfiguration of the CCD arithmetic unit is accomplished either by activating on-chip controls or by adjusting the inputs so that only the desired function is realized. With reference to Figure 1, the following on-chip functions can be controlled by external binary inputs:

- The two adders at the input can be independently set to either add or subtract
- A delay can be inserted following either the top adder or the top multiplier
- The output adder can be connected either as an adder or as an accumulator
- The internal feedback path from the output back to the input can either be connected or disabled.

It can be seen from Figure 1 that the inputs to the final adder/accumulator are provided by the outputs of two multipliers. This serves to cross-couple the outputs of the two input adder/subtractors which, after multiplication, are summed or differenced, thus completing the complex multiplication required in the FFT kernel or "butterfly" computation. When the CCD arithmetic unit is used for computations

other than the FFT, the cross-coupling can be disabled by making the multiplier coefficient zero. Since there are four multipliers, there are four different (useful) ways of making the interconnections by means of disabling unwanted paths with multiplier coefficients equal to zero.

The programming of the CCD arithmetic unit is strongly influenced by the necessity to time-multiplex the input/output data on the limited number of pins available on a standard package. The charge transfer nature of CCD arithmetic using multiphase clocks requires 2.5 clock intervals for a 1-bit addition or subtraction and five clock intervals for a 1-bit multiplication. It is convenient to arrange the data format so that four clock intervals are used for both the data input/output and the multiplier coefficient input, with the fifth clock interval a "do nothing" state which can be used to synchronize the CCD arithmetic unit with a memory or other external devices. The timing sequences for the various types of computations are indicated in Table 2.

Assuming a 5 MHz clock rate, 1 μ sec is required for the five clock intervals in the data format. By the use of pipelining, operations requiring multiplication can be done at a 1 MHz rate. If only addition/subtraction is required, then a 2 MHz throughput can be attained.

It is to be emphasized that these rates are achieved only with pipeline operation. The total delay through the two 16-bit adder/subtractors and the 16x16 multipliers in the signal path amounts to 32 μ sec at an assumed 5 MHz clock rate. This factor of 32 represents the difference between pipeline operation and a recursive operation where the output must be available before the next input can be processed. For this reason, computations which are inherently of a streaming nature (e.g., the FFT, correlation, etc.) are particularly well suited to the operation of the CCD arithmetic unit.

INTERLEAVING

When the CCD arithmetic unit is set to operate as a recursive filter, the relatively long propagation delay through the arithmetic functions necessitates the reduction of the sampling rate to below 30 kHz. If only a single filter is being com-

puted, the arithmetic unit is operating very inefficiently because valid inputs appear only in one of the 32 1- μ sec intervals constituting the delay through the chip. This situation can be remedied by multiplexing the inputs so that inputs from parallel sources can be interleaved in time. The concept is illustrated in Figure 3 and is basically a conventional time division approach. The delay through the CCD arithmetic unit is divided into 32 1- μ sec intervals. The signal from the first source is accepted on the 1st, 33rd, 65th, ..., intervals. The signal from the second source is accepted on the 2nd, 34th, 66th, ..., intervals, and so on. In this way, signals from as many as 32 different sources can be processed simultaneously with one CCD arithmetic unit. By changing the on-chip controls and the multiplier coefficients in synchronism with the inputs, different computations (e.g., single zero filter, double-pole filter, etc.) can be performed on the different inputs.

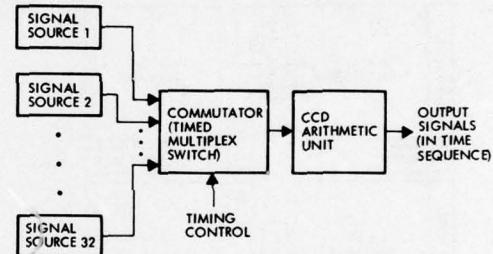


Figure 3. Time Interleaving of Multiple Inputs to the CCD Arithmetic Unit

Another method of obtaining the full computational potential of the CCD arithmetic unit is to use time interleaving to realize a cascade of digital filter sections. This is a very practical procedure because complex digital filters are usually implemented as a cascade of first and second order sections in order to minimize quantization effects. In this case, it is necessary to add an external register as indicated in Figure 4. The external register provides an additional 1 μ sec delay needed to apply the output at the n th time interval to the input at the $(n+1)$ th interval. For example, assuming the computation is running continuously and the first section of a digital filter is computed in the first of

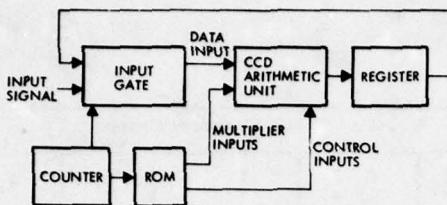


Figure 4. Realization of Cascade by Time Interleaving

32 time intervals, the outputs would appear at the 1st, 33rd, 65th, ..., intervals. The one interval delay provided by the external register allows these values to be applied to the input of a second filter section at the 2nd, 34th, 66th, ..., intervals. Proceeding in this way, a cascade digital filter of 32 different sections can be computed with a single CCD arithmetic unit plus a source of multiplier coefficients and control levels which operates in sync with the arithmetic unit.

From the preceding discussion of processing multiple input signals either from independent sources or as a cascade operation on a single signal, it is obvious that a mixture of the two types of operation is possible. For example, the 32 time intervals could be used to compute eight 4-section filters, four 8-section filters, or any other combination of sources and multiple sections provided the total does not exceed the 32 time intervals available. All that is required is that the timing be carefully controlled and synchronized so that each operation is performed periodically in its assigned time interval.

GENERAL PURPOSE PROGRAMS

Before proceeding with the examples of the different signal processing functions which may be realized with the CCD arithmetic unit, a few comments should be made about operation as a general purpose microprocessor. The primary limitation is the relatively long (32 μ sec) propagation delay through the CCD arithmetic unit. This means that programs with many branching points may result in a long execution time. As with the special purpose signal processing functions, programs which can be organized to operate in a pipeline fashion will have the lowest execution time.

The powerful computational capability of the CCD arithmetic unit should not be ignored in general purpose program applications. For example, the parallel adders at the input allow the arithmetic operations and the program instructions to be overlapped in time so that the arithmetic result and its storage location, for example, would appear essentially simultaneously at the output. The adder/subtractor, multiplier, adder/accumulator sequence in the chip layout allows great versatility in computing jump instructions. This combination of powerful arithmetic capability with the unfortunately long propagation delay presents a challenge to the programmer in general purpose applications.

EXAMPLES OF ARITHMETIC UNIT CHIP USAGE

This section discusses several specific configurations of the arithmetic unit chip. A block diagram is shown for each function desired, and this is then compared to the functional realization as achieved by reprogramming the arithmetic chip. The required signal paths and multiplier coefficients are shown where appropriate.

SINGLE ZERO RECURSIVE FILTER

The arithmetic chip can be operated as a single zero recursive digital filter. The block diagram of the single zero recursive filter and the corresponding equations are shown in Figure 5a. A control level is applied to the chip to inhibit the input on the even clock periods (i.e., T_2 and T_4). As shown in Table 2, the data input is accepted during T_1 , and a zero value is inserted during T_3 . At the multiplier inputs, the sequence is K, 0, 1, and 0. The zero serves to disable the unwanted paths as shown in Figure 5b. The 1 and K multiplier values cause the two single paths to be combined to form the desired output.

TWO SINGLE-POLE RECURSIVE FILTERS

Operation of the arithmetic chip as a pair of single-pole recursive filters is shown in Figure 6a. The organization of the chip allows two independent filters to be computed simultaneously. The two

Table 2. Arithmetic Unit Timing Sequences

Programmable Configuration	Clock Period - Input					Clock Period - Output				
	T ₅	T ₄	T ₃	T ₂	T ₁	T ₅	T ₄	T ₃	T ₂	T ₁
FFT										
Data input	Y ₂	X ₂	Y ₁	X ₂		CY ₂ +ST ₁	CT ₁ -ST ₁	Y ₁ +Y ₂	X ₁ +X ₂	
Multiplier input	-	-	sin θ	cos θ		-	(T ₁ =X ₁ -X ₂) (T ₂ =Y ₁ -Y ₂)	-	-	
Single zero filter										
Data input	-	0	-	X _{in}		-	-	-	-	Y _{out}
Multiplier input	0	1	0	K		-	-	-	-	-
Two single-pole filters										
Data input	-	U _{in}	-	X _{in}		-	V _{out}	-	-	Y _{out}
Multiplier input	0	K ₂	0	K ₁		-	-	-	-	-
Single-pole filter with scaled output										
Data input	K _{scale}	0	0	X _{in}		-	K _{scale} Y _{out}	-	-	Y _{out}
Multiplier input	K _{scale}	0	0	K ₁		-	-	-	-	-
Two-pole resonator										
Data input	-	-	-	X _{in}		-	Y _{out}	-	-	K _{scale}
Multiplier input	K _{scale}	K ₁	0	K ₂		-	-	-	-	Y _{out}
Itakura analyzer										
Data input	-	B _{n-1}	-	A _{n-1}		-	B _n	-	-	A _n
Multiplier input	1	K	K	1		-	-	-	-	-
Itakura synthesizer (First pass)										
Data input	-	B _m	-	A _{m+1}		-	S ₂	-	-	S ₁
Multiplier input	1	K	0	1		-	-	-	-	-
(Second pass)										
Data input	-	S ₂	-	S ₁		-	B _{m+1}	-	-	A _m
Multiplier input	1	0	K	1		-	-	-	-	-

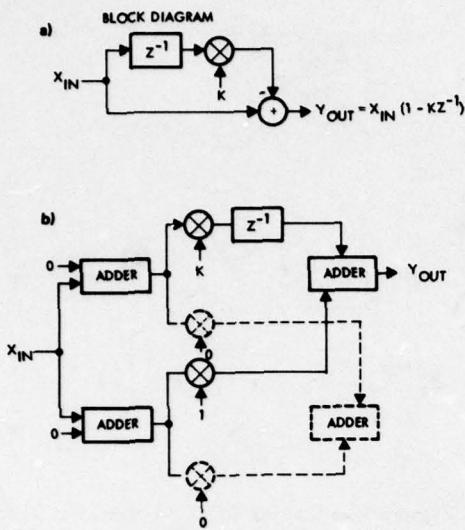


Figure 5. Data Inputs to the CCD Arithmetic Unit

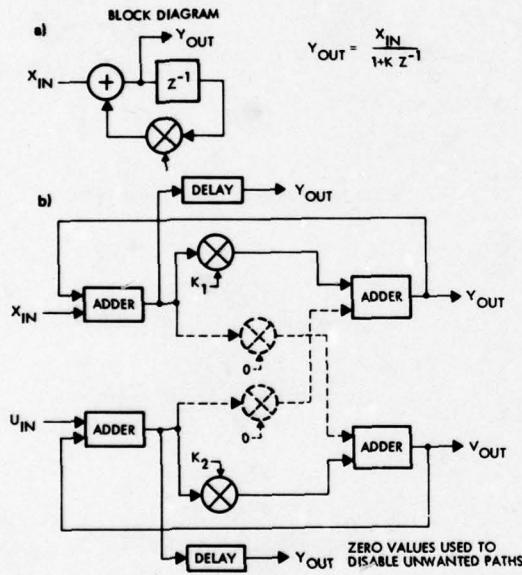


Figure 6. Use of CCD Arithmetic Unit as Parallel Single-Pole Recursive Filters

inputs are applied on the first and third clock pulse intervals. A control level disables the inputs during the even intervals when the outputs are fed back internally to the adder inputs. The multiplier inputs K_1 and K_2 adjust the time constants of the two filters. Zeros are provided to disable the unwanted paths. The delay required for the recursive filter is provided by the propagation through the multiplier. The subtraction of the output from the input is performed twice by the input adder. After the first subtraction, the difference is applied to the multiplier where it is multiplied by the filter coefficient. After the second subtraction, the difference is delayed one clock period as shown in Figure 6b.

SINGLE-POLE FILTER WITH SCALED OUTPUT

For complex recursive digital filters, it is often desired to provide a weighting or scale factor between adjacent stages. The arithmetic chips can be used to provide a single-pole recursive filter with a scaled output. In this configuration, it is very similar to the one previously described for the two multiplexed single-pole filters with the exception that, in this case, the scaling operation is substituted for the second filtering operation. The operation may be described with the aid of Figure 7. The top half of Figure 7 is identical to Figure 6a and represents a single-pole recursive digital filter. To obtain a scaled output, the same values that were applied to the top adder are also applied to the bottom adder. In this case, the difference formed by the adder is multiplied by the scale factor K_{scale} and is supplied as an output.

LATTICE FILTER - THE ITAKURA ANALYZER SECTION

Linear predictive coding (LPC) is a bandwidth reduction method used for secure voice systems. The linear predictive coder reduces the data rate from a nominal input rate of 60 kilobits to an output rate of less than 5 kilobits. The Itakura procedure is a streaming approach to implement the linear predictive coder with recursive digital filters. The lattice filter

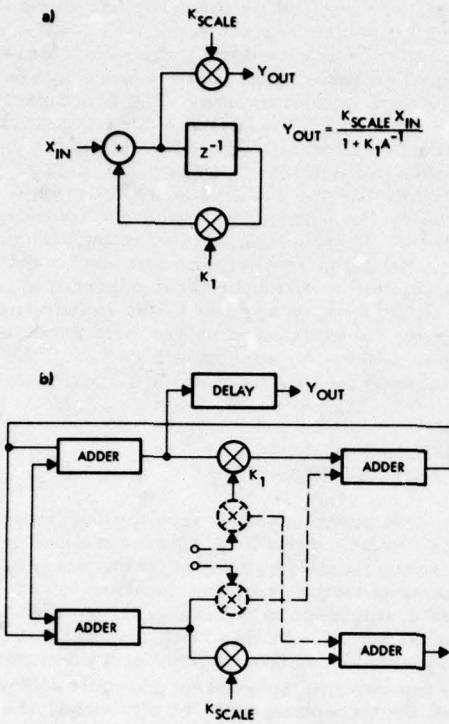


Figure 7. Single-Pole Recursive Filter with Scaled Output

used in the Itakura analyzer is shown in Figure 8a. Inputs to the CCD arithmetic chip are provided during the first and third clock pulses. These correspond to the A and B input in Figure 8a. The multiplier inputs are unity or K, where K is the PARCOR(2) coefficient. In Figure 8b, it is seen that the two outputs, A and B, are obtained by combining the direct (multiplied by unity) and the weighted (multiplied by K) values. Operation of the arithmetic chip in the Itakura analyzer section is particularly straightforward due to the similarity between the complex rotation used in the FFT and the structure of the lattice filter.

THE ITAKURA SYNTHESIZER SECTION

The synthesizer section for the Itakura linear predictive coder employs a lattice filter as shown in Figure 9a. This filter is somewhat more difficult to realize with

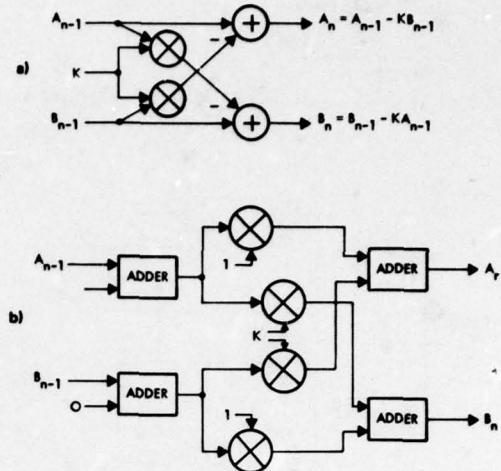
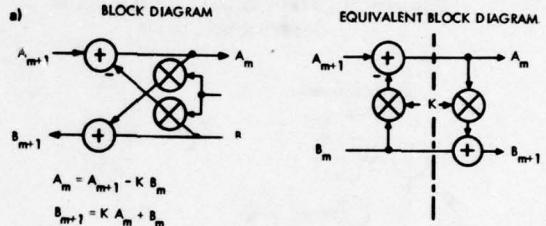


Figure 8. Use of CCD Arithmetic Unit as Lattice Filter (Analyzer)



TWO PASSES THROUGH ARITHMETIC CHIP REQUIRED

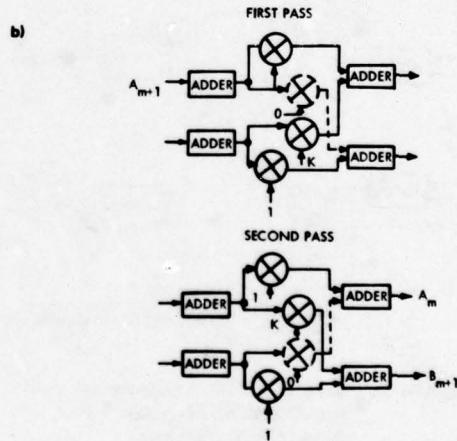


Figure 9. Use of CCD Arithmetic Unit as Lattice Filter (Synthesizer)

the arithmetic chip because two multiplications are required in order to obtain the output. To accomplish this, the lattice filter operation is split into two segments, and two passes through the arithmetic chip are required. Alternatively, two chips can be used — one chip for the first pass and the second chip for the second pass. Referring to Figure 9b, on the first pass, the two inputs A_{m+1} and B_m are applied to the input adder. A_{m+1} is multiplied by unity, and B_m is multiplied by K. The two are added in the top output adder. B_m also appears at the output adder after having been multiplied by unity. In the second pass through the arithmetic chip, the order of the multipliers is changed so that the top input passes through the multiplier, after having been multiplied by unity, and appears at the output as A_m . The lower input is combined with the upper input multiplied by K and appears at the lower adder output as B_{m+1} .

NONRECURSIVE DIGITAL FILTER

As a final example, consider the use of the arithmetic unit in conjunction with a correlator chip, which we described in a previous paper.⁽¹⁾ To use these two chips together, it is necessary to consider the techniques that allow achieving, say, 8-bit accuracy. To achieve 8-bit coefficient accuracy, the signal, s, and the reference, r, consisting of 8-bit words, are partitioned into 4-bit segments

$$\begin{aligned}s &= a + b \\r &= c + d\end{aligned}$$

with a and c the 4 most significant bits (i.e., ≥ 16) and b and d the 4 least significant bits (i.e., < 16). The multiplication $s \cdot r$ becomes

$$\begin{aligned}s \cdot r &= (a+b)(c+d) \\&= ac + bc + ad + bd\end{aligned}$$

Thus, four CCD digital correlator chips would be used to form the product comprising a 32-sample signal segment. In addition, three arithmetic unit chips would be needed to sum the four products. Nonrecursive filters with lengths equal to multiples of 32 can be formed by cascading 32-sample sections in a manner similar to that shown in Figure 10.

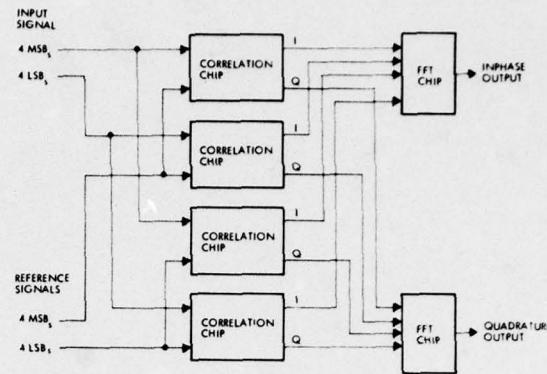


Figure 10. Nonrecursive Digital Filter — 8-Bit Quantization

CONCLUSIONS

The advantages of digital signal processing for most applications are well known and relate to greater accuracy, flexibility, and environmental reliability. However, the growth of digital signal processing has to date been hampered by cost and power limitations even with the use of LSI. The advent of CCD digital processing techniques, as discussed in this paper, has the potential for greatly alleviating these problems and thereby allowing more effective digital signal processing hardware implementations to be achieved in the future. CCD allows high density, low power LSI operation in a full pipelined signal processing architecture. Circuit techniques are now under development towards this objective.

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SIGNAL PROCESSING CAPABILITIES OF A 100 x 100 CCD ARRAY

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ABSTRACT A prototype camera and signal processing unit has been built using three identical 100 x 100 interline transfer CCD arrays. Each CCD organization is in a SPS (series, parallel, series) format. A unique electrical interface allows the output to be compatible with standard EIA RS170 format monitors and recorders operating at 30 television frames per second. The system operation features both frame-to-frame subtraction and long-term recirculation of stored data. Details of implementation are presented along with suggested areas of application, particularly as a moving target indicator.

INTRODUCTION

Efficient analog signal processing in charge coupled devices is predicated upon the existence of compatible CCDs with electrical input capabilities for temporary storage and delay of the live signal. The number and variety of commercially available CCDs, especially those with electrical input capabilities, are still quite limited. Exclusion of those CCDs intended for digital applications further limits the number of devices available. This paper presents design experience with one commercially available device which is useful for both imaging and analog signal processing: Fairchild's CCD201. The use of interline transfer devices, such as the 201, necessitates special signal handling techniques.

CCD ORGANIZATION AND STRUCTURE

The CCD201 is a 2-phase, 10,000-element self-scanning image sensor, using buried channels with ion-implanted barriers. The active light sensitive portion of each element is 1.2 mils horizontal by 0.8 mils vertical. To allow for interline analog shift registers, the elements are center spaced at 1.2 mils vertical by 1.6 mils horizontal. Thus, 50 percent of the chip area is photosensitive and a 4 X 3 image aspect ratio is provided. One-hundred columns of 2-phase vertical analog shift registers are inter-digitated in the photo-

sensor array. A 102-element, 2-phase horizontal analog shift register permits clocking of successive horizontal lines to an output detector/preamplifier which is balanced with a compensation output amplifier.

Additionally, the CCD201 includes a 100-element, 2-phase analog input shift register which, when properly clocked, will accept electrical signals through an input diode on the device. The actual input function involves applying a signal-modulated DC level to the input diode and gating the signal in by clocking the input gate at the proper time within the horizontal cycle. A 2-phase horizontal input clock is incorporated to shift charge through the register. The input register includes an output drain to prevent charge build-up in case of overclocking.

FULL FRAME MOVING TARGET INDICATOR (MTI) SYSTEM

Figure 1 shows the functional blocks of a full-frame MTI system using an interline transfer CCD imager and two matching CCD analog shift registers. Generalizing from the specific case of the 100 x 100 array discussed earlier, the CCD array is assumed to be composed of "N" rows by "M" columns of photosensitive cells. Readout, in the usual interline transfer manner, is accomplished by shifting

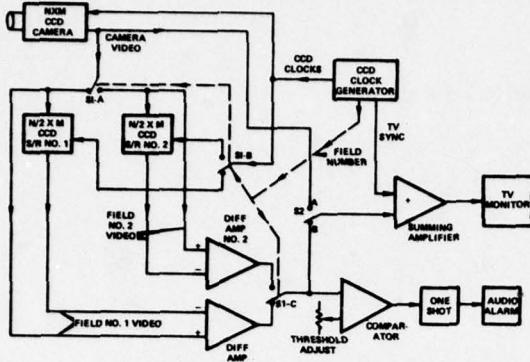


Figure 1. CCD MTI Block Diagram

alternate rows of photosite charge accumulations into the adjacent vertical shift-registers. Discrete charges are then clocked through the shift register array to the output. This inter-digitated format, necessary to give the camera its interlace feature, reduces the effective size of the shift register array to $N/2 \times M$. Although this is generally of little importance in imaging systems, it directly impacts the scheme for using identical interline CCDs as shift registers. The effective storage capability has been reduced by 50 percent from that of the imager.

The CCD clock generator section of Figure 1 produces horizontal and vertical clock signals for the CCD. In addition, TV sync pulses and a signal referred to as "field number," which changes states on alternate fields, are generated. The system operation proceeds by initially assuming both shift-registers (S/R) are empty and the field number is such that information in field #1 is being read out of the camera. Switches S1-A and S1-B are connected to S/R #1 so that camera video is input to this device. At the end of field #1, the information stored in S/R #1 is identical, on a cell-by-cell basis, with that transferred out of the imager's shift-register. Once the field transfer has finished, the field number signal changes state, causing S1-A and S1-B to be connected to S/R #2. This second memory is now loaded with field #2 information. It is important to realize that the information stored in one shift-register remains static while the other is being loaded and read out. After field

#2 is loaded and the field number changes state again, field #1 video is again read out from the camera. Simultaneously, S/R #1 video is read out and the "old" and "new" field #1 video is subtracted in differential amplifier #1. This subtraction occurs on a cell-by-cell basis in real time with the "new" field #1 video.

If the amount of charge collected on any individual pixel of the imaging CCD has changed from one frame to the next, there will be an output from differential amplifier #1 when the cell is simultaneously clocked out of the two devices. Otherwise, the amplifier has zero output throughout the entire field. An identical subtraction function is performed by differential amplifier #2 and the shift register #2 during the alternate field of video.

If S1-C is alternately switched between the two amplifiers, the wiper of S1-C will contain one entire frame of MTI video, which can be used in several ways, two of which are shown in Figure 1. With single-pole, double-throw switch S-2 in position B, TV sync pulses are added to the MTI video for display on a standard television monitor. Motion in any portion of the scene will be displayed, while all stationary scene components will cancel on a cell-by-cell basis with the stored field. Therefore, not only the presence of motion, but the location of the motion is derived.

The second (though less sophisticated) output which could be used in conjunction with, or in place of, the TV system is also shown. The MTI video is compared to a reference voltage and, when threshold is exceeded, a one-shot multi-vibrator is triggered to sound an audio alarm for some time period. While the TV compatible mode limits the system to standard 30 frame/second comparison times, the audio alarm could be used at frame rates from three to three hundred frames per second, allowing greater system versatility.

The modular design of the system allows considerable flexibility. Use of only one shift register and one differential amplifier degrades vertical resolution by 50 percent. For some applications where resolution is of secondary importance, this may be a desirable trade. Switch S₂ placed in position A, equivalent to a removal of all memory functions, returns the system to a normal, camera

only, mode capable of driving a standard monitor. The system in this configuration requires less than 20 square inches of breadboard circuitry for operation and easily fits in a $2 \times 3 \times 5$ inch package.

This approach to motion detection has several advantages over others, the most important of which is exact registration. Since the imager and shift registers are operated from a common clock, there is no chance of improper timing causing imperfect subtraction. Also, this is the only feasible method of obtaining a true analog delay of $1/30$ second. The alternative would be a complex and costly pseudo-analog approach using A/D and D/A converters with large numbers of digital shift-registers. Added to this is the inherent low power and small volume characteristics of CCDs and the low-light level capability of CCD imagers.

FULL FRAME RECIRCULATING MEMORY

Figure 2 represents the basic elements of a full-frame recirculating memory using the same interline transfer CCD imager and matching CCD analog shift resistors. Its operation is related to the state of the field number signal from the clock generator which, again, multiplexes the two CCDs on alternate fields. As before, the CCD clock generator produces all clock signals for the CCD and TV sync pulses.

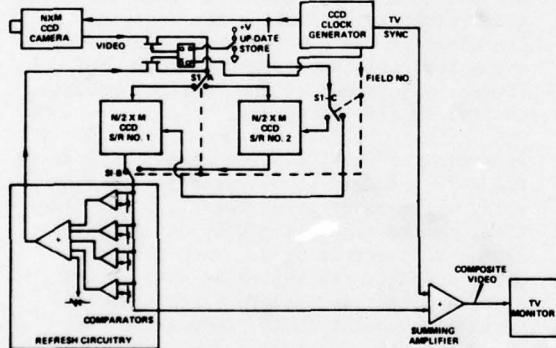


Figure 2. Recirculating Memory

The operation of the system begins when the UPDATE/STORE switch is placed in the UPDATE position. This allows the succeeding frames of video to be loaded into S/R #1 on the first field and S/R #2 on the second

field. Since the CCD clocks are also switched on alternate fields, via contact S1-C, the video read into each CCD is stored for one field before being read out. Multiplexing of these outputs through switch S1-B provides exactly a one-frame delay between video being readout of the camera and that being displayed on the monitor.

Continuous recirculation of a given frame of data is initiated by returning the UPDATE/STORE switch to the STORE position. The D flip-flop signals the end of a complete frame of video stored in the two CCDs. Camera video is then disconnected from the shift register inputs and replaced with the output of the refresh circuitry. As shown, this circuit is composed of a group of comparators and a summing amplifier. The comparator thresholds are set to quantize analog outputs into several (five in this case) levels. For example, if the thresholds are set at 1, 2, 3, and 4 volts and the fixed offset into the summing amp is set at 0.5 volt, then the transfer function of the refresh circuitry would be as shown in Figure 3.

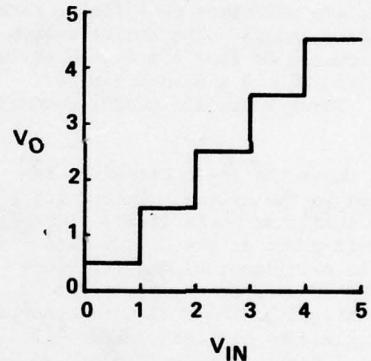


Figure 3. Transfer Function of Refresh Circuitry

The requirement for the refresh circuitry is a result of the finite transfer efficiency of the CCD as well as noise considerations. As an example, Fairchild's 100×100 element CCD201 with a transfer efficiency of 0.9995 will displace 50 percent of its charge after about 1380 shifts, or 9.2 cycles through the device. For a 30 frame per second system, this corresponds to a hold time of less than $1/3$ second. In practice, dark current accumulation in the CCD and random noise associated with the input and output mechanisms further degrade the

signal. Addition of the refresh circuitry to the feedback loop corrects signal degradations of up to $\pm 1/2$ volt (in this example) before the signal is fed back into the CCD.

By routing the multiplexed CCD outputs to the summing amplifier and/hence, the monitor, an image having perfect registration and five quantized grey shades can be continuously displayed. Obviously, there is a limit to the number of comparators that can be used effectively. Each quantized bin must be sufficiently wide to correct for degradations due to transfer inefficiencies and noise variations. A thermo-electric cooler to lower the operating temperature of the memory CCD would be expected to provide additional grey shade storage capability.

PROTOTYPE OPERATION

A modified version of the system described in the previous two sections was built for laboratory tests and evaluation. The principal change involved using only one CCD for each function. Therefore, both MTI and the recirculating memory functions are performed on a field, rather than a frame, basis. The entire system was constructed on four 4 x 6 inch circuit boards plus a 2 x 3 x 5 inch camera housing. Three Fairchild CCD201 devices are used.

Figure 4 shows the logic circuitry incorporated in the system. Except for a few modifications, it is identical to the circuit given in the CCD201 data sheet. An oscillator with a frequency of 3.6 MHz is used as the clock for U2 and U3, which form the horizontal counting chain by dividing the oscillator by 224. Since the 1.8 MHz horizontal clock ϕ_H is derived by dividing the oscillator by 2, U3's carry output occurs each 112 horizontal clock pulses, corresponding to one horizontal line. This output is 7 ϕ_H periods wide and is used for horizontal blanking. The remaining 105 periods are used to clock the output register of the CCD. ϕ_R is active during the first quarter of ϕ_H , while ϕ_S occurs during the last quarter.

The vertical counting chain consists of U4 and U5. With single pole, double throw switch S1 in position A as shown, U8 and the associated 3-input AND gate are not

involved in the active circuitry and the vertical clock is at the line rate. Fifty-one lines are counted before the load command at Q2 of U5 is generated. This command, vertical blanking #1, exists for one line. U6 is loaded at the same time as the vertical counting chain. This interrupts the clock to U4 for 13 lines, forming vertical blanking #2. Total blanking period is the sum of vertical blanking #1 and #2, or 14 lines. When added to the 51 active lines, a total field length of 65 lines results.

U7 is a multiplexer designed to produce ϕ_p and ϕ_V . ϕ_p goes low for the first half of vertical blanking #1 and then low for the whole of vertical blanking #1 on the alternate field. ϕ_V is basically horizontal blanking during the active field and high or low during vertical blanking on alternate fields. The relationship between ϕ_p and ϕ_V on the negative transition of ϕ_p determines which set of elements of the sensor is transferred into the vertical transport register.

Since each horizontal line requires 112 ϕ_H cycles, the line rate is 1.8 MHz \div 112 \approx 16 KHz, which is sufficiently close to 15.75 KHz (standard TV line rate) to be used with 525 line monitors. As mentioned before, a field is composed of 65 lines, resulting in a frame rate of 16 KHz \div 130 = 123 frames per second. Forcing a 30 frame per second monitor to sync to this increased rate requires paralleling the resistor in the wiper of the vertical hold control with a smaller resistor, typically 100 Ω . Of course, adjustment of the vertical height control is also necessary.

Operation of the 100 x 100 element CCD at the CCTV standard of 30 frame-per-second rate, while maintaining the 15,750 Hz line time, can be accomplished by using U8 to divide U3's output by 4. With double pole, double throw switch S1 in position B, U8's output is used to clock the vertical counting chain, increasing the field time by a factor of four. Since horizontal sync pulses to the monitor are not divided, the overall result is that only one vertical shift of ϕ_V in the CCD occurs for each four lines displayed on the monitor. The monitor will now run at 30 frames per second making it compatible with the requirements of EIA RS-170 standards. The CCD imager's inte-

gration time, being increased four times, allows operation at lower light levels (~ 2 f-stops).

The clocks, as generated in Figure 4, are used to drive both imager and storage CCDs; Figure 5 indicates the arrangement for driving the imager. Each of the T^2L level clocks needed is amplified and level shifted by one of the clock driver circuits of Figure 6. The normal state of the clock waveform at the CCD determines which circuit is used. These drivers offer the high speed operation necessary to clock the CCD at TV compatible rates and the low power dissipation desirable for a minimum system heat generation. Since ϕ_{V1} and ϕ_{V2} require identical voltage levels, some component reduction is accomplished by sharing power supply transistors (Q1 and Q3) between these two complementary signals. The same is true of ϕ_{H1} and ϕ_{H2} .

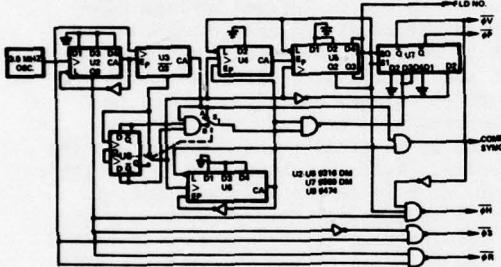


Figure 4. CCD Clock Generator

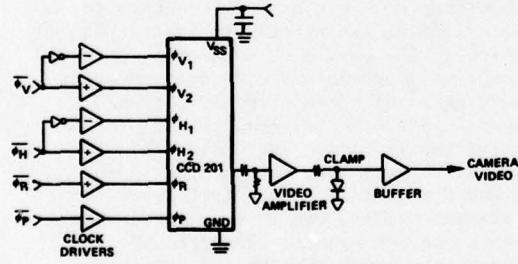


Figure 5. CCD201 Camera

The output signal level of about 75 mV is capacitively coupled to remove the DC offset. The signal is then amplified and clamped to a DC level near ground potential. A unity gain buffer offers a low output impedance for transmitting the camera video to three other functional blocks of Figures 7, 8 and 9.

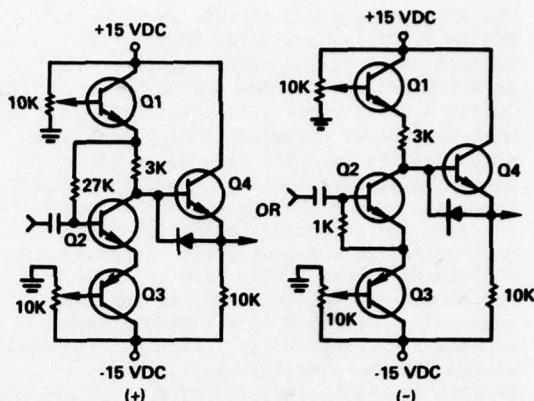


Figure 6. Clock Driver Circuits

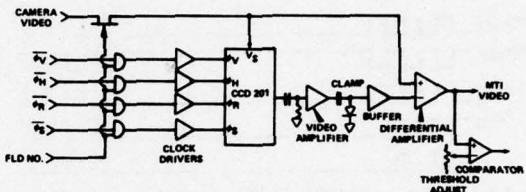


Figure 7. Single-Field MTI

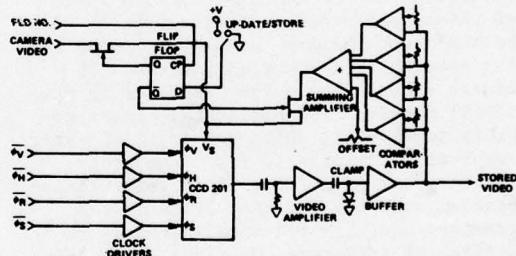


Figure 8. Single-Field Storage

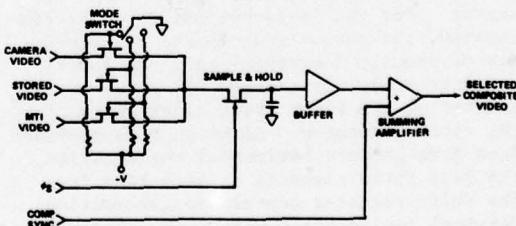


Figure 9. Video Processing

The single-field MTI circuit is shown in Figure 7. Here, a single CCD201 array is used as an analog shift register. It is worth noting that the device, when operated in this mode, is interfaced with peripheral circuitry in much the same manner as the imager. Both modes of operation require vertical, horizontal, and reset clocks. A photogate clock is not required for the memory mode since the photosites are not addressed. However, additional clocks in the form of input horizontal (ϕ_{H1-IN}) and sampling (ϕ_S) are required. Figure 10 is a timing diagram showing the relationships between horizontal clocks and the sampling clock. Input horizontal clocks (ϕ_{H1-IN} and ϕ_{H2-IN}) are held low during the vertical transfer. Otherwise, the input horizontal clocks are identical to the output clocks.

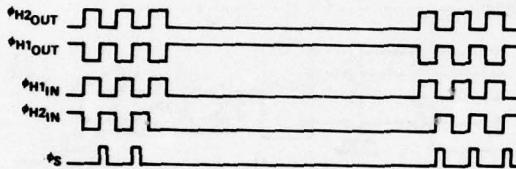


Figure 10. CCD201 Shift Register Waveforms

Although the waveforms of Figure 10 are sufficient for producing a delayed field of video, the problem of registration must be dealt with before the device can be used for element-by-element comparison with camera video. The output register on the CCD201 requires 102 horizontal clocks to empty completely, while the input register requires 100 clocks to fill completely. The simplest solution to this registration problem, and the one that leads to the greatest useful scene area, is to clock all horizontal registers 102 times. The input register will dump the overfill, resulting in each element holding the charge associated with the equivalent element on the sensor. For the prototype system under discussion, the sensor was clocked 105 times (as previously described), and the shift register array was clocked 102 times by inhibiting the first three clock pulses from the clock generator. Although this approach does give perfect horizontal registration, the last three elements of each line from the shift register contain no information. Vertical registration must also be considered. The 51 vertical shifts per field derived from the clock generator board is exactly

the number required to transfer data through the CCD 201 shift register.

Figure 7 showed that the clocks are applied to the shift register on alternate fields only. This provides same field comparison on odd numbered fields (for instance), and no MTI output video on even fields. The resulting resolution is 50 x 100 elements. Background suppression to 2 percent of white level has been demonstrated with the prototype system over the entire dynamic range of the imager. This type of performance is achieved only after careful clock level and amplifier adjustments. In the system being discussed, a comparator with its threshold set at 5 percent of white level was added to the differential amplifier's output. This completely eliminated stationary components of the viewed area from the displayed video.

The single-field storage (Figure 8) is similar to the full-frame storage discussed previously, except that only one CCD is employed, removing the requirement for the multiplexing circuitry. The prototype system uses from two to four comparators in the refresh circuitry, giving up to five levels of recirculating storage. Again, registration is important since each cycle through the CCD must result in the same element-time relationship. The same clocks are used in this scheme as those in the single field MTI. False alarms, defined for this discussion as a charge degradation of sufficient magnitude to cause the CCD's output to be quantized incorrectly in the refresh circuit, are very much a function of the number of comparators and their threshold settings. With two properly adjusted comparators, the false alarm rate (FAR) is virtually zero. Increasing this number to four comparators greatly increases the FAR for the first few recirculation cycles, but it then settles to about one per minute. This transient phenomenon can be attributed partly to charge-spreading in the CCD for large contrast changes between adjacent cells, and partly to electronic transients when the input of the CCD is switched between camera video and video from the refresh circuit.

Figure 9 shows the essential elements of the video processing electronics used in

the prototype system. Here, one of the three available videos (direct camera, stored, or MTI) is chosen for display. Due to the format of the CCD video output (see the CCD201 data sheet), a sample-and-hold is required to remove clock components. Finally, composite sync is added to the video in a summing amplifier before routing the composite video to the monitor.

SUMMARY AND CONCLUSIONS

A 100 x 100 CCD array, organized in a SPS (series, parallel, series) format, has shown itself to be a very versatile device. Although normal operation is a 2-phase, 10k element, self-scanning image sensor, the device design includes a 100 x 1 bit input register which may be used for electrical input. By using a common set of clock voltages to drive the electrical input register of the identical (storage only) devices in synchronization with the imaging chip, data has been shown stored in temporary memory and subsequently read out for frame-to-frame subtraction on succeeding fields. Or the output of the memory chip may be tied back to its own input and the information recirculated for an indefinite period if appropriately refreshed.

Operation in the frame-to-frame subtraction mode allows the detection of moving objects in the field of view. Operation in the recirculation mode, with refresh, increases the storage capability of the device since each bit now has several analog levels associated with it. Areas of application include security systems for detection of unauthorized entry, storage of the scene at the time of the alarm, and slow scan transmission to a remote monitoring point.

A prototype camera and signal processing unit, operating in the above described modes, has been built with one imaging chip and two storage CCDs.

Operation of the unit is simplified by a unique electrical interface allowing the output to be displayed on an unmodified 30 frame/second CCTV monitor. This allows the camera mode of operation to be compatible with EIA RS170 format monitors and recording devices. It is believed that the use of this smaller device in a CCTV compatible format offers cost advantages in those applications

where the higher resolution, and consequently higher cost, of larger devices is not necessary.

THE USE OF CHARGE COUPLED DEVICES IN ELECTROOPTICAL PROCESSING

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ABSTRACT. The use of coherent optical analog methods to perform matrix multiplications has been reported in the literature. Described in this paper are two incoherent optical systems in which the matrix multiplication represents a general linear transformation of one data vector into another. The input data vector is represented as a time sequence of N amplitude weighted electrical pulses which temporally modulate the light output of an LED. This modulated light field first passes through optical transparency and is then incident upon a charge coupled device (CCD). In one system the CCD is a 500×1 element line array and in the other it is a 100×100 area array. The transparency is arranged in a rectangular array of $M \times N$ elements, where the transmittance of each element is proportional to the m, n^{th} sample of the impulse response or kernel of the linear transformation. Finally, the output data vector is in the form of a time sequence of M electrical pulses, the amplitudes of which represent the values of the desired output data vector.

The linear transformation thus performed is one of broad application, the particular nature of the transformation depending upon the form of the impulse response encoded into the optical memory transparency. Examples of transformations which can be readily programmed into the device include convolutions; correlations; Fourier, Laplace, and Walsh-Hadamard transformations; and linear filtering.

An electrooptical system is particularly appropriate for such calculations in moderate-accuracy (6-8 bit) applications. A direct evaluation of this discrete matrix operation requires $M \times N$ analog multiplications to be performed in a sequential manner such that the elements of the output vector are produced one at a time. To significantly reduce the processing time relative to such a slow direct implementation, one must reduce the time required for each analog multiplication, process in parallel, or both. In the electrooptical systems described here, both of these processing advantages are inherently present.

INTRODUCTION

The use of coherent optical analog methods to perform matrix multiplications has been reported in the literature.¹⁻³ An electrooptical approach utilizing incoherent optical technology has recently been described in which a vidicon tube was used as the integrating element.⁴⁻⁶ Presented below is an extension of this latter work in which the vidicon is replaced by a line-array charge coupled device (CCD) in one system, and by an area-array CCD in another.^{7, 8}

We consider the electrooptical implementation of a general linear filter, illustrated in Fig. 1, which is characterized by an impulse response $h(u;v)$. The output of such a filter, $g(v)$, is related to the input, $f(u)$, through a general linear transformation

$$\int_{-\infty}^{\infty} f(u)h(u;v)du = g(v) \quad (1)$$

in which the impulse response appears as a weighting function. We shall not restrict our discussion to shift-invariant filters, for which Eq. (1) would reduce to a simple convolution, and will therefore be able to treat a larger class of useful linear transformations. The relation described by Eq. (1) is one of broad application, the particular nature of the transformation depending on the form of the impulse response. Table 1 lists a few examples of signal processing transformations together with the appropriate form of $h(u,v)$. Thus, a signal processing device for which the impulse response can be readily programmed, and which can subsequently perform the transformation of Eq. (1) with economy

of time and hardware, should find widespread and versatile use.



Fig. 1. General linear filter characterized by impulse $h(u,v)$. Input $f(u)$ is transformed into output $g(v)$ through a linear transformation integral.

TABLE I. EXAMPLES OF LINEAR TRANSFORMATIONS COMMONLY USED IN SIGNAL PROCESSING APPLICATIONS. EACH TRANSFORMATION IS OF THE FORM OF EQ. (1), WITH IMPULSE RESPONSE $h(u,v)$ AS SHOWN BELOW.

TRANSFORMATION	IMPULSE RESPONSE
Convolution	$h(v-u)$
Cross correlation	$h(u-v)$
Autocorrelation	$f(u-v)$
Cosine transform	$\cos(2\pi uv)$
Fourier transform	$\exp(-i2\pi uv)$
Laplace transform	$\exp(-uv)$
Hankel transform	$2\pi J_0(2\pi uv)u$

Anticipating the electrooptical implementations to be described below, which are basically sampled data systems, we consider the discrete finite version of Eq. (1).

$$\sum_{n=0}^{N-1} f_n h_{mn} = g_m \quad m = 0, 1, 2, \dots, M-1 \quad (2)$$

It is often useful to rewrite this equation in its equivalent matrix notation

$$[H][F] = [G].$$

Written in full this relation becomes

$$\begin{bmatrix} h_{00} & h_{01} & \dots & h_{0,N-1} \\ h_{10} & h_{11} & \dots & \vdots \\ \vdots & \vdots & \ddots & \vdots \\ h_{M-1,0} & h_{M-1,1} & \dots & h_{M-1,N-1} \end{bmatrix} \begin{bmatrix} f_0 \\ f_1 \\ \vdots \\ f_{N-1} \end{bmatrix} = \begin{bmatrix} f_0 h_{00} + f_1 h_{01} + \dots + f_{N-1} h_{0,N-1} \\ f_0 h_{10} + f_1 h_{11} + \dots + f_{N-1} h_{1,N-1} \\ \vdots \\ f_0 h_{M-1,0} + f_1 h_{M-1,1} + \dots + f_{N-1} h_{M-1,N-1} \end{bmatrix} = \begin{bmatrix} g_0 \\ g_1 \\ \vdots \\ g_{M-1} \end{bmatrix} \quad (3)$$

where each matrix has a direct interpretation in terms of the processors described in this paper.

At this point, it is appropriate to comment on why an electrooptical implementation of this fundamental matrix operation is being considered here. Note that a direct evaluation of Eq. (3) requires $M \times N$ analog multiplications to be performed in a sequential manner such that output values g_m are produced one at a time. In order to increase the rather slow processing rate associated with such a direct approach, one must reduce the time required for each multiplication, process in parallel, or both. In an optical system both of these processing advantages are inherently present. Although they must still be detected, analog multiplications take place as fast as light travels through an optical transparency (about 10^{-13} sec). Also, the two-dimensional nature of image transfer in an optical system provides the capability of performing many such multiplications simultaneously (up to about 10^6 in the systems described below). Therefore, in applications involving high-speed calculations of moderate accuracy (6-8 bit), an electrooptical system seems a particularly appropriate approach.

We describe in sections to follow two different electro-optical devices designed to implement the matrix multiply operation of Eq. (3). The first utilizes a scanning mirror to sweep the temporally modulated image of an optical memory transparency or mask across a line-array CCD. The second eliminates the need for a scanning mirror by replacing the line-array detector with an area-array CCD and electronically scanning the mask image within the detector itself.

LINE-ARRAY PROCESSOR

GENERAL DESCRIPTION

Fig. 2 depicts the incoherent electrooptical system used to evaluate the matrix multiplication of Eq. (3). The system consists of: (a) light emitting diode (LED), (b) condensing lens, (c) optical memory mask, (d) imaging lens, (e) scanning mirror, and (f) line-array CCD.

Given a temporal signal $f(t)$, for which some linear transformation must be performed according to Eq. (1), the input to the device is a time sequence of electrical pulses, f_n , which represent sampled values of $f(t)$. These samples are proportional to the elements of the column vector $[F]$ in Eq. (3), and appear as an intensity modulation of the LED. The condensing lens is chosen for uniformity of illumination upon the mask and to maximize the light throughput in the system by imaging the light source into the entrance pupil of the imaging lens. Directly behind the condenser is placed the optical mask in which is encoded the matrix operator

[H]. An image of the mask is then formed by the imaging lens, via a scanning mirror, on the face of the CCD. The scanning mirror is galvanometer driven in a sawtooth fashion such that an image of the mask is repetitively swept across the CCD face at a constant velocity in a direction perpendicular to the long dimension of the array. The CCD is then allowed to integrate the light falling on it during a single passage of the image, and a new output vector [G] is generated and clocked out of the CCD at the end of each minor sweep.

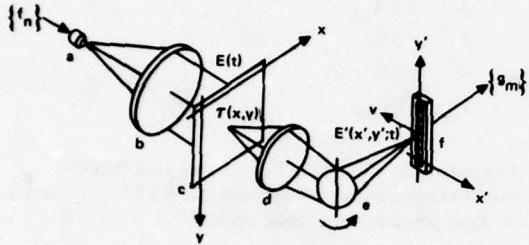


Figure 2. Incoherent electrooptical processor utilizing a mirror scan and line-array CCD. Components are: (a) light emitting diode (LED); (b) condensing lens; (c) optical memory mask; (d) imaging lens; (e) scanning mirror; and (f) line-array charge coupled device (CCD).

MATHEMATICAL ANALYSIS

Given that an analog temporal signal $f(t)$ must be sampled and then transformed according to Eq. (2) into a new discrete signal, we shall proceed by tracing $f(t)$ through the system from input to output. The first step in preparing the analog input signal for processing is to convert it to a time sequence of pulses by passing it through a form of sample-and-hold circuit. The discrete version of the signal, shown in Fig. 3, then becomes

$$f_s(t) = \sum_{n=0}^{N-1} f_n \operatorname{rect}\left(\frac{t-nT - d/2}{d}\right) \quad (4)$$

where

$$f_n \triangleq f(nT)$$

and T is the sampling period, d is the constant pulse duration, and the rectangle function (rect) is defined in Appendix A. The discrete signal $f_s(t)$ is then used to modulate the light emitted by the LED so that the spatially uniform irradiance distribution incident on the optical memory mask in the x, y plane is

$$E(t) = c_1 f_s(t) \quad (5)$$

where the constant c_1 is a scaling factor which depends on the design of the condensing optics and on the scale of the electrical-to-optical pulse conversion by the LED and its electronics.

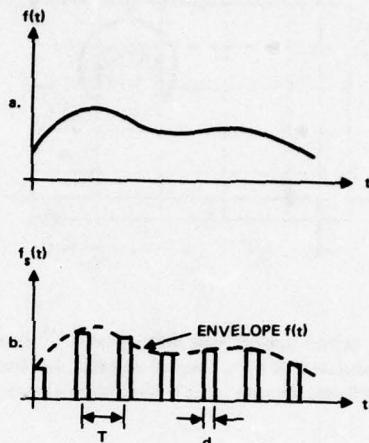


Fig. 3. The input signal (a) and its sampled version (b). Sample pulses of height $f_n \triangleq f(nT)$ and period T are all of same duration d .

The mask itself consists of a total of $M \times N$ rectangular apertures arranged in a rectangular array as shown in Fig. 4. Note that each element is the same size, $A \times B$, but that the clear area of each element, $a_{mk} \times W$, is modulated by varying the x -dimension while holding the y -dimension fixed. This design, which modifies the transmitted radiant flux by varying the area of an aperture, is considerably easier to fabricate than one which varies the transmission properties of some photographic or electrooptic material. From the diagram, then, the transmittance function of the optical mask is given by

$$\tau(x, y) = \sum_{m=0}^{M-1} \sum_{k=0}^{N-1} \operatorname{rect}\left(\frac{x-kA}{a_{mk}}\right) \operatorname{rect}\left(\frac{y-mB}{W}\right) \quad (6)$$

where

$$a_{mk} = c_2 h_{mk} \quad (7)$$

and c_2 is a scaling constant. Inspection of Eq. (6) shows that there is now a one-to-one correspondence between each element of the mask and the corresponding element of the matrix operator [H] in Eq. (3).

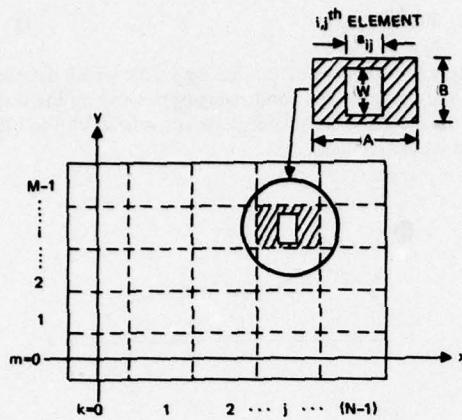


Fig. 4. Optical memory mask showing only i, j^{th} element. Mask consists of $M \times N$ rectangular elements, the clear portion of each having the same width W but a variable length a_{mk} .

The light field emerging from the optical mask is simply the product of the incident irradiance and the mask transmittance function. The resulting light distribution is then imaged onto the plane of the detector via a scanning mirror. The irradiance distribution in the x' , y' plane resulting from the temporally modulated mask image, moving at a speed v in the negative x' direction, is then

$$E'(x', y'; t) = c_3 E(t) r\left(\frac{x' + vt - x'_0}{\beta}, \frac{y'}{\beta}\right) \quad (8)$$

In this equation c_3 is a constant determined from radiometric considerations of the imaging system, x'_0 is an arbitrary spatial phase term associated with the scanning, and β is the lateral magnification associated with the mapping of the optical mask into its image.

Knowing the irradiance distribution in the detector plane, the quantity of interest in terms of the response of the CCD is the total exposure delivered to the x', y' plane during a single sweep of the mirror. This is given by

$$\xi(x', y') = \int_0^\infty E'(x', y'; t) dt. \quad (9)$$

Making the appropriate substitutions from Eq. (4) through (8), the total exposure becomes

$$\begin{aligned} \xi(x', y') &= c_1 c_3 \sum_{n=0}^{N-1} \sum_{m=0}^{M-1} \sum_{k=0}^{N-1} f_n \text{rect}\left(\frac{y' - mB'}{W}\right) \\ &\quad \int_0^\infty \text{rect}\left[\frac{t - (nT + d/2)}{d}\right] \text{rect}\left[\frac{t - (kA'/v + x'_0/v) + x'/v}{a'_{mk}/v}\right] dt \end{aligned} \quad (10)$$

where for convenience we have defined the magnification-scaled quantities

$$\begin{aligned} A' &= \beta A \\ B' &= \beta B \\ W' &= \beta W \\ a'_{mk} &= \beta a_{mk} \end{aligned}$$

Evaluating the integral in Eq. (10) we find that the m, k^{th} exposure element due to the n^{th} LED pulse is one of three possible trapezoidal solids.*

$$\begin{aligned} &\left(c_1 c_3 d f_n \text{rect}\left(\frac{y' - mB'}{W}\right) \text{trap}\left[\frac{x' - (k-n)A'}{a'_{mk}/v}; \frac{a'_{mk} + v}{a'_{mk}/v}\right] \right) & a'_{mk} > vd. \quad (11a) \\ \xi(x', y')_{nmk} &= \begin{cases} \frac{c_1 c_3}{v} f_n a'_{mk} \text{rect}\left(\frac{y' - mB'}{W}\right) \text{tri}\left[\frac{x' - (k-n)A'}{a'_{mk}}\right] & a'_{mk} = vd. \quad (11b) \\ \frac{c_1 c_3}{v} f_n a'_{mk} \text{rect}\left(\frac{y' - mB'}{W}\right) \text{trap}\left[\frac{vd - a'_{mk}}{2}; \frac{vd + a'_{mk}}{2}\right] & a'_{mk} < vd. \quad (11c) \end{cases} \end{aligned}$$

In arriving at the expressions of Eq. (11), several important requirements have been included. First, it is assumed that the moving mask image is in phase synchronization with the LED such that the first ($k=0$) column of the mask image is centered on the y' -axis half way through the first ($n=0$) LED pulse. This implies that

$$x'_0 = \frac{vd}{2}.$$

Second, the timing of the LED pulses must be such that the exposure pattern will be of the proper scale. That is, it will ensure that half way through the n^{th} light pulse the $k=n^{\text{th}}$ column of the mask image will also be centered on the y' -axis. This means that

$$A' = vT.$$

*See Appendix A for definitions of the rect, trap, and tri functions used here. Also see Appendix B for evaluation of the form of integral contained in Eq. (10).

The exposure elements described by Eq. (11) and their size relationships to a CCD element are illustrated in Fig. 5. The exposure element $\xi(x',y')_{nmk}$ describes the distribution of radiant energy per unit area delivered to the detector plane from the m,k th mask element during the n th LED pulse. As can be seen from the diagram, the size of a given exposure element relative to the size of a CCD element must be considered when computing the total radiant energy actually entering the CCD element. Of the five possible combinations described in Fig. 5, three pass an amount of radiant energy during a single light pulse which is proportional to the desired product $f_n a'_{mk}$. These are cases (a) and (b) with trapezoid height $R = (c_1 c_3/v) f_n a'_{mk}$ and case (b) with $R = c_1 c_3 d f_n$. Of these three we select the first for practical consideration since it greatly reduces tolerance requirements in mask fabrication and in scan synchronization. Therefore, combining Eq. (10) and (11c), the total exposure in the x',y' plane is

$$\xi(x',y') = \frac{c_1 c_3}{v} \sum_{n=0}^{N-1} \left\{ \sum_{m=0}^{M-1} \sum_{k=0}^{N-1} f_n a'_{mk} \right. \\ \left. \text{rect} \left(\frac{y' - mB'}{W'} \right) \text{trap} \left[\frac{x' - (k-n)A'}{\frac{vd - a'_{mk}}{2}, \frac{vd + a'_{mk}}{2}} \right] \right\} \quad (12)$$

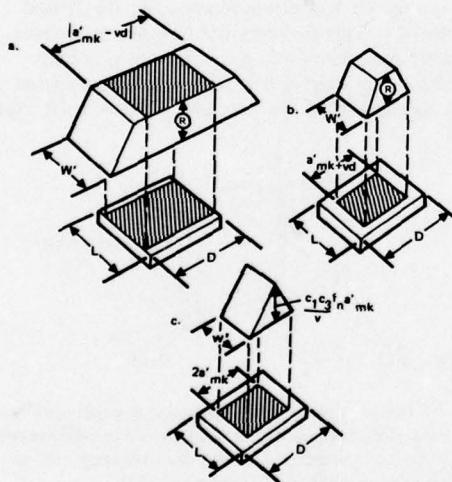


Fig. 5. Possible relationships between exposure element and detector element as described by Eq. (11). Eq. (11a) can correspond to cases (a) or (b) above where $R = c_1 c_3 d f_n$. Eq. (11b) is represented by case (c) above, and Eq. (11c) is described by cases (a) or (b) with $R = c_1 c_3 / v f_n a'_{mk}$.

As shown in Fig. 6, the expression in braces, $\{ \}$, above, represents a rectangular array of trapezoidal solids due to the n th LED pulse. A new such exposure array is created with each input pulse f_n , but each array is shifted from the preceding by an amount A' . Note from the figure that for the n th input light pulse, only the $k=n$ th column of the exposure array will be superimposed upon the detector. Finally, we assume that in the y' -dimension, each exposure element is narrower than a CCD element. In summary, the assumptions

$$k = n \\ L \geq W' \\ D \leq vd - a'_{mn}$$

when combined with Eq. (12), yield the total radiant energy entering the m^{th} CCD element during a complete mirror sweep as

$$Q_m = c_1 c_2 c_3 \frac{LD}{v} \sum_{n=0}^{N-1} f_n h_{mn}. \quad (13)$$

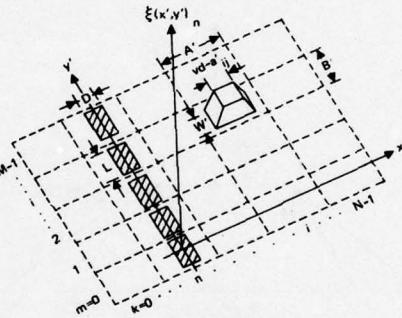


Fig. 6. Exposure pattern $\xi(x',y')_n$ due to the n th LED pulse. Pattern is rectangular array of trapezoidal solids (only i,j th exposure element shown) shifted in the negative x' direction by an amount nA' . Note that n th column of exposure array is centered on the detector array (shaded elements).

Comparison of Eq. (13) with Eq. (2) shows that the quantity Q_m is indeed proportional to the desired quantity g_m . At the completion of a given mirror sweep the charge packets stored in each of the M CCD elements are clocked sequentially out of the device yielding a time sequence of pulses which are respectively proportional to the elements of the desired column vector $[G]$ in Eq. (3).*

*The assumption is that the energy entering each CCD element is linearly converted to charge within the element. Deviations from this assumption, or compensation techniques, will not be discussed in this paper.

One final consideration is the relation between the length of the mask elements, a_{mn} , and their spacing in the x -dimension. A profile of the m,n^{th} trapezoid function of Eq. (12) is shown in Fig. 7, where it is superimposed upon the m^{th} CCD element of width D .

For a given pulse duration d and velocity v , note from the figure that, while the scope of the trapezoid sides depends upon the LED pulse strength f_n , the overall width of the exposure element depends solely upon the length of the mask image element a'_{mn} . Also notice that the upper vertices of the trapezoid lie on the legs of a triangle shown by dashed lines. Thus, for a given f_n , the top of the trapezoid gets higher and narrower as a'_{mn} increases. Since the detector must lie within the flat portion of the exposure element, a'_{mn} can vary between zero and a maximum value determined by the CCD element width D . In terms of the mask element itself,

$$0 \leq a_{mn} \leq \frac{vd - d}{\beta}. \quad (14)$$

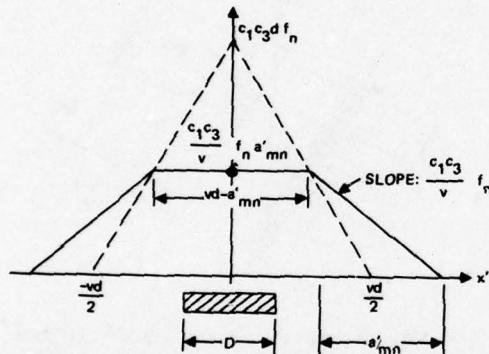


Fig. 7. Profile of m,n^{th} exposure element superimposed upon m^{th} CCD element (shaded). Upper vertices of trapezoid always lie on legs of triangle shown with dashed lines.

To calculate the minimum spacing required between mask elements, the overlap between two adjacent trapezoidal elements for which a'_{mn} is a maximum must be considered. As shown in Fig. 8, the minimum allowable spacing in the exposure plane then occurs when $d=T$. From the figure we conclude that the absolute minimum spacing of mask elements must therefore be

$$A_{\min} = \frac{vT}{\beta}. \quad (15)$$

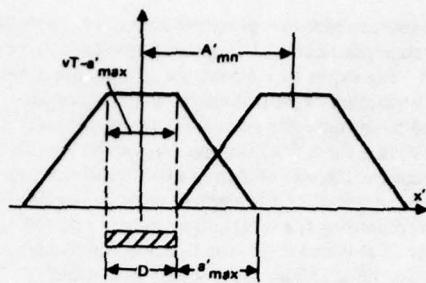


Fig. 8. Minimum possible spacing between adjacent exposure elements occurs when $d = T$ and when a'_{mn} assumes the maximum value $a'_{\max} = vT - D$.

AREA-ARRAY PROCESSOR

GENERAL DESCRIPTION

In the system described below, the need for a scanning mirror is eliminated by incorporating an area-array detector in place of the line-array CCD used above. By using a two-dimensional CCD, the scanning of the mask image can now be performed electronically within the detector itself. This allows considerable simplification in system design as well as analysis. Such a modified system is represented in Fig. 9, where up to the optical memory mask the geometry is essentially the same as in the line-array system described by Fig. 2. Immediately behind the mask is an area-array CCD whose output is a sequence of pulses representing the desired vector $[G]$. This geometry not only avoids the mechanical complexity of a scanning mirror, but also eliminates the imaging lens and the space associated with its mapping of the mask image onto the detector.*

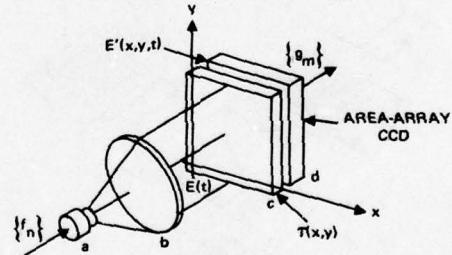


Fig. 9. Area-array electrooptical processor in which need for a scanning mirror is eliminated through use of a two-dimensional CCD. System consists of: (a) LED; (b) condensing lens; (c) optical memory mask; and (d) area-array CCD.

*We speak here of the mask and detector as being in physical contact, as indeed they could be with a specially designed CCD. However, for convenience in the experimental work performed thus far, the mask has been imaged onto the detector with a lens.

MATHEMATICAL ANALYSIS

As before, we represent the spatially uniform light field incident upon the optical mask by

$$E(t) = c_1 \sum_{n=0}^{N-1} f_n \operatorname{rect}\left(\frac{t-nT-d/2}{d}\right) \quad (16)$$

where c_1 is a constant scale factor.

For ease of fabrication, we again represent the elements of the optical mask as a rectangular clear apertures arranged on a rectangular array with spacing $A \times B$ (Fig. 10). Here the clear portion of the m,k^{th} mask element is of length $\sqrt{a_{mk}}$ in the x -dimension and width $K\sqrt{a_{mk}}$ in the y -dimension where

$$a_{mk} = c_2 h_{mk}, \quad (17)$$

$$K = B/A, \quad (18)$$

and c_2 is a scaling constant.

The transmittance function of the mask is then

$$r(x,y) = \sum_{m=0}^{M-1} \sum_{k=0}^{N-1} \operatorname{rect}\left(\frac{x-kA}{\sqrt{a_{mk}}}\right) \operatorname{rect}\left(\frac{y-mB}{K\sqrt{a_{mk}}}\right) \quad (19)$$

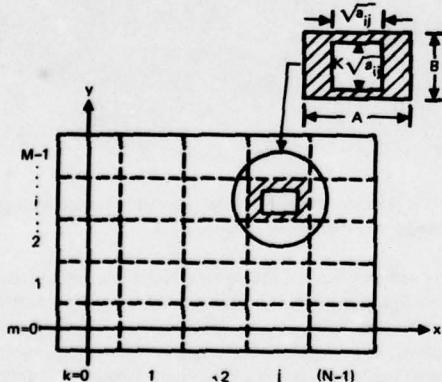


Fig. 10. Optical memory mask showing only i,j^{th} element. Mask consists of rectangular array of $M \times N$ rectangular elements. The clear area of the i,j^{th} element is $K\sqrt{a_{ij}}$, where $K = B/A$.

Immediately behind the optical mask the irradiance distribution incident on the detector plane is

$$E'(x,y,t) = E(t)r(x,y). \quad (20)$$

The optically sensitive region of the area-array CCD consists of a rectangular array of identical rectangular photosensors, as shown in Fig. 11. These CCD elements, each of size $D \times L$, are arranged on an array the same size and scale as the optical mask. In addition, the aspect ratio of each mask element is scaled to be the same as that of the corresponding CCD element. That is,

$$\frac{B}{A} = \frac{L}{D} = K. \quad (21)$$

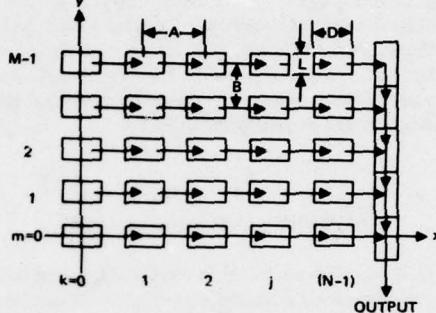


Fig. 11. Rectangular array of rectangular CCD photosensors. Each element is of size $D \times L$, where $L/D = B/A = K$. Column at right represents output shift register for clocking out charge transferred from the photosensor array.

We now focus attention on the energy entering the m,k^{th} element of the CCD due to the n^{th} LED pulse,

$$\begin{aligned} Q_{nmk} &= \int_{-\infty}^{\infty} \int_{-\infty}^{\infty} \int_{-\infty}^{\infty} E'(x,y,t) dx dy dt \\ &= c_1 c_2 d K f_n h_{mk}. \end{aligned} \quad (22)$$

In particular, the energy entering the $k = n^{\text{th}}$ element in the m^{th} row is proportional to $f_n h_{mn}$, the product inside the summation of Eq. (2). What is desired is the sum of such products for all values of n . Thus, if the charge content of each CCD cell in the m^{th} row is transferred laterally, as indicated in Fig 11, by one element between LED pulses, then the stored photocharge in the m,k^{th} element due to the n^{th} pulse can be added to the charge stored in the $(m,k-1)^{\text{st}}$ element due to the $(n-1)^{\text{st}}$ pulse. This means that the partial sum in the last ($k=N-1$) cell of the m^{th} row after the r^{th} pulse is

$$S_{mr} = c_1 c_2 d K \sum_{n=0}^r f_n h_{m,N-(r-n+1)} \quad (23)$$

Finally, after the last pulse ($r=N-1$), the charge stored in the last cell of the m^{th} row is proportional to

$$S_{m,N-1} = c_1 c_2 d K \sum_{n=0}^{N-1} f_n h_{mn}. \quad (24)$$

Again referring to Eq. (2), this expression is proportional to the desired quantity g_m . After N light pulses, the charge stored in the output shift register is vertically clocked out. This charge, in the form of discrete packets, yields a time sequence of pulses proportional to the values g_m of the desired column vector $[G]$.

COMMENTS AND CONCLUSIONS

Eq. (13) and (24) predict that the line-array and area-array systems described above are capable of performing the linear transformation of Eq. (2). A developmental model of the line array processor, shown in Fig. 12, has been assembled and tested. The system is similar to that previously reported,⁴⁻⁶ however, here a 500-element Fairchild line-array CCD has replaced the vidicon tube. In addition, a compact layout has been used in which the optical system is confined to a 4×5 inch circuit board.

An area-array processor which utilizes a 100×100 element Fairchild CCD has also been assembled, see Figure 13, and is currently being tested. The detector, which is a standard imaging chip, is being driven in a manner to suit this signal processing application. Used as an image sensor, the CCD array would continuously integrate during each full video frame.* However, for the case at hand the device integrates during each individual LED pulse, but between pulses the charge collected at each photosite is transferred laterally by one element and added to the photocharge from the next pulse. This shift-and-add process is repeated 100 times, after which the charge deposited in the output shift register, representing the desired output data vector, is clocked out.

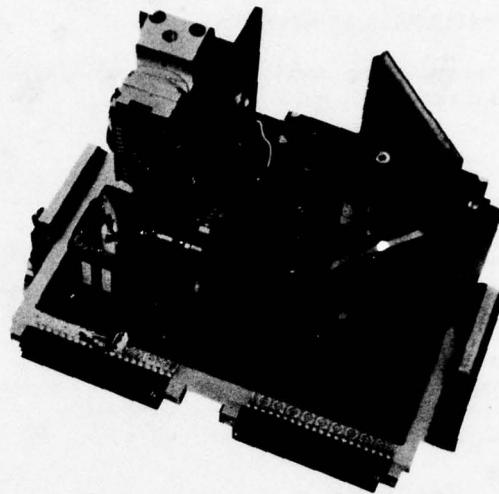


Fig. 12. Line-array electrooptical processor on a 4×5 inch circuit card. Device is programmable by inserting a desired program mask. Support electronics occupies three additional cards of the same size.

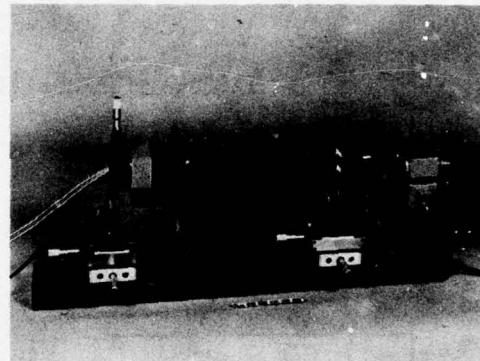


Fig. 13. Area-array electrooptical processor. Device is programmable by inserting desired program mask.

As described earlier, the optical memory masks fabricated thus far utilize an area modulation scheme for encoding the values h_{mn} . This technique is straightforward, not involving materials problems (e.g., nonlinearities), and lends itself to mask fabrication with a programmable desk calculator and x-y plotter. Two mask examples are shown in Fig. 14 for the cases of a discrete identity transform and a discrete cosine transform.

*Interlacing is ignored in this discussion.

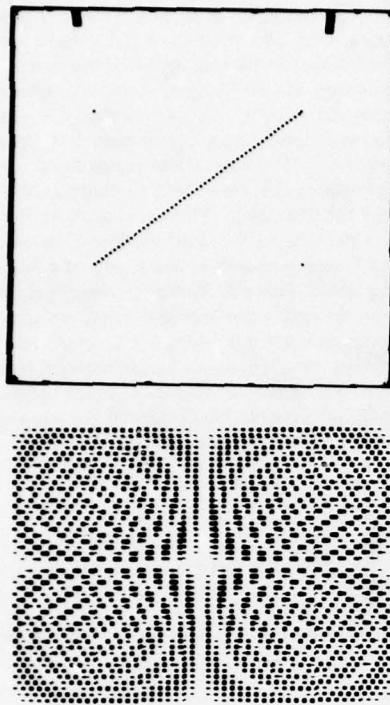


Fig. 14. Examples of 35 mm format memory masks designed to perform (a) a discrete identity transform, and (b) a discrete cosine transform.

These masks have been used in preliminary tests of the area-array processor, with favorable results illustrated in Figs. (15) and (16). As a first test we consider the case where the impulse response operator of Eq. (2) is a matrix with diagonal elements of unity and off-diagonal elements zero. This defines the so-called identity matrix. Its use in Eq. (2) reproduces at the output an exact replica of the input function. Typical performance of the area-array processor with an identity matrix in place is shown in Figure 15. In this example the input signal (lower trace) was a one volt (peak-to-peak) triangle wave of 0.8 kHz frequency, sampled at 10 kHz. As seen in the figure, the output signal (upper trace) is a well formed triangle wave of the same frequency as the input signal. The few spurious samples at each end of the output trace are not part of the processed signal and are ignored. As a second test, a mask was prepared for performing a discrete cosine transform. Theoretically, a pure cosine wave input results in two delta functions at the output, centered in the output array, and separated by a distance pro-

portional to twice the input frequency. The results of this test are shown in Fig. 16 for two input cosine waves of one volt (peak-to-peak) amplitude and frequencies (a) 1.1 kHz and (b) 2.5 kHz. As can be seen from the figure, these results agree quite well within the theoretically predicted outputs.

It is appropriate at this point to consider the data rates associated with these processors. In the 500×1 line-array system of Fig. 12, a rather slow scanning mirror was used rather than a high speed spinning prism to demonstrate the concept. The data must be emptied out of the CCD at the end of each mirror scan before a new scan can begin. The time required to perform the transform on the next set of input samples is determined by the 20 msec sweep period of the mirror. In this system, input samples can be fed in at a continuous rate of about 1 kHz. The resulting output comes in 0.5 msec bursts of 500 data pulses at 1 MHz with 20 msec between bursts.

For the 100×100 area-array processor, the data can also be clocked from the output shift register at 1 MHz. This must be 100 times faster than the rate at which charge is being transferred across the array. Since for each lateral data shift there is one light pulse, a continuous input rate of 10 kHz yields a continuous output pulse rate of 1 MHz.



Figure 15. Input (lower trace) vs. output (upper trace) with identity matrix programmed into electrooptical processor.

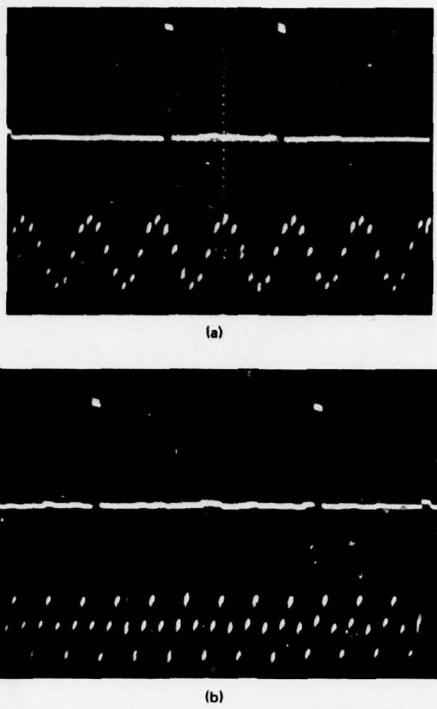


Figure 16. Input (lower trace) vs. output (upper trace) with processor programmed for a cosine transform. Input signals are cosine waves with frequencies (a) 1.1 kHz and (b) 2.5 kHz.

In performing a linear transformation, the line-array device operates on sequential windows of input data as shown in Fig. 17a. Although the output data appear in high-frequency bursts, over the period of one mirror cycle there are 500 output data pulses for each 500 input samples. However, in this area-array processor example there are 100 output data pulses for each input sample. What this means is that a new and complete transform is computed, with each input pulse, on a sliding window of input data (Fig. 17b). That is, each new set of output pulses represents the linear transformation of an input data set which differs from the preceding set by the addition of a new sample and the dropping of the oldest. If the functional form of the input signal varies in time, then its transform as a function of time can be continuously computed. This represents a useful capability inherently available in the device if required. An example of its use would be the computation of the discrete Fourier transform of a signal whose exact time of arrival is not known. Thus, one could avoid truncating the input signal by not including it entirely within the sampling window.

As a final comment, let us point out that although we have considered the analog input $f(t)$ to have been sampled before modulating the LED, this is not in general necessary. When the input signal is sampled according to Eq. (4), the total light collected by a given CCD element due to the n^{th} LED pulse is exactly proportional to f_n . However, if the analog input is not sampled beforehand, then the "sampling" is done in effect by the CCD itself. The photosensitive elements of the CCD integrate the light incident upon them only during a time determined by the length of a photogate clocking pulse. This performs a sampling operation. However, the light integrated will be proportional to the average value of $f(t)$ during the sampling interval. This average value will in most cases be sufficiently close to the instantaneous value f_n so that sampling of the input signal and all the associated synchronization problems can be eliminated.

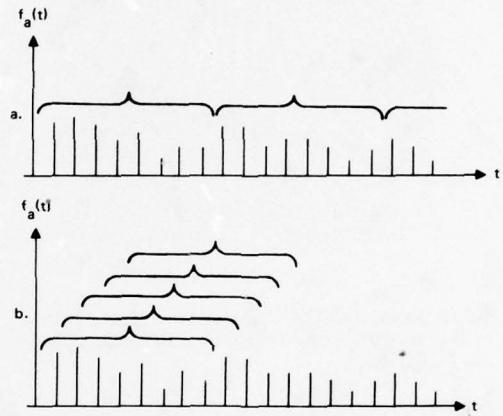


Fig. 17. With the area-array processor, transforms can be performed not only on (a) sequential windows of data but also on (b) input data under a sliding window.

ACKNOWLEDGMENT

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APPENDIX A

Many useful and often common functions must be defined in piecewise fashion because of abrupt changes in the value of the function. For example, consider the function $f(u)$ such that

$$f(u) = \begin{cases} 0, & u < -a, \\ \frac{u}{a} + 1, & -a \leq u \leq 0, \\ -\frac{u}{a} + 1, & 0 \leq u \leq a, \\ 0, & u > a. \end{cases}$$

To achieve compactness and clarity of notation for such simple but awkwardly expressed functions, we define in Fig. A1 a set of functions which implicitly include such abrupt behavior. We refer to these as the rectangle, triangle, and trapezoid functions, respectively. Note that the piecewise function cited in the above example now may be simply written as

$$f(u) = \text{tri}\left(\frac{u}{a}\right).$$

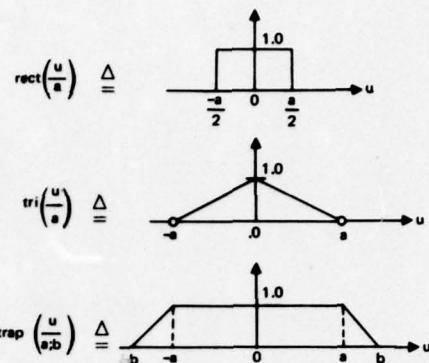


Fig. A1. Calculations involving abruptly changing functions are greatly simplified by adopting a compact notation. Used in this paper are three such awkwardly expressed functions which are simply defined as the (a) rectangle (rect), (b) triangle (tri), and (c) trapezoid (trap) functions, respectively.

APPENDIX B

The integral contained in Eq. (10) is of the form

$$\int_{-\infty}^{\infty} \text{rect}\left(\frac{u}{a}\right) \text{rect}\left(\frac{u+v}{b}\right) du. \quad (\text{B1})$$

The integrand in Eq. (B1) gives the area common to both rectangle functions when the second is offset from the first by an amount v (Fig. B1). Thus, the overlap area, which varies as a function of v , provides three possible solutions to the integral:

$$a \text{ trap } \left[\left(\frac{b-a}{2} ; \frac{b+a}{2} \right) \right], \quad v < b. \quad (\text{B2a})$$

$$b \text{ tri } \left(\frac{v}{b} \right), \quad a = b, \quad (\text{B2b})$$

$$b \text{ trap } \left[\left(\frac{a-b}{2} ; \frac{a+b}{2} \right) \right], \quad a > b. \quad (\text{B2c})$$

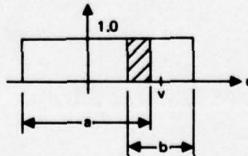


Fig. B1. Shaded overlap area between two rect functions gives value of integral in Eq. (B1) as function of displacement v .

ANALOGUE CORRELATORS USING CHARGE COUPLED DEVICES

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ABSTRACT

One of the desirable objectives in the development of CCD signal processing devices is to produce a fully integrated analogue cross-correlator. A processor with a code storage capability of, say 32, samples would meet a range of requirements. The ability to cascade such processors allows extended system applications. This paper reports on two developments towards such a processor, the construction and operation of a hybrid cross-correlator and the design of a 32 bit integrated correlator chip.

HYBRID CORRELATOR

The CCD is capable of sampling and storing analogue signals using a shift register action. When this function is combined with non-destructive tapping circuitry feeding into analogue multipliers, then it is possible to perform real time cross-correlation of analogue signals. A processor of this form is shown schematically in figure 1.

A hybrid correlator was assembled using two CCD's each using 8 taps, the respective tapped signals were fed into separate monolithic multipliers and the products were then summed in an operational amplifier. The CCD's were constructed using a simple single level aluminium structure with etched gaps 2-3 microns wide. They were three phase surface channel devices using an n-type substrate. A floating gate reset technique^{1,2} was used as the basis of the tap circuitry.

The analogue multipliers used were of type MC 1594 L. The maximum bandwidth of these multipliers is 0.8 MHz and it has a linearity of 0.5%. The summing function was performed using an operational amplifier, type LH0032CG, with a slew rate of 500 V/ μ s. The summed output was then fed into a sample and hold circuit type DMC 651. This device produces considerable

transient noise due to logic feedthrough, limiting its dynamic range to 22 db.

The ability to make use of the full performance of the CCD is obviously constrained by the performance of the peripheral circuitry. If the CCD has a dynamic range of m:1 then the multiplier needs to be capable of processing a signal range of $m^2:1$ and the amplifier a range of $nm^2:1$ if there are n taps.

The maximum bandwidth of the correlator was limited by the multipliers to 0.8 MHz. At the output of the correlator the maximum observable signal was limited by the feedthrough in the sample and hold circuit, reducing the dynamic range from 30 db at the output of the CCD to 20 db at the output of the sample and hold.

The storage time for the reference channel of the processor was limited by dark current in the CCD to the order of a few milliseconds. Very much larger storage times (many seconds) are theoretically possible and times of 100 msec are typical experimentally.

TV LINE CORRELATION

The processor described was used to correlate a portion of one television line

with the remaining lines of the same television frame. The video output from a CCD camera was fed into an interface unit which had controls to select any portion of the TV frame. The selected signals were stored in the reference channel and held constant by inhibiting the clock waveforms to the reference channel. The lines succeeding the reference line were then passed through the signal channel of the processor and correlated with the stored signal. A two dimensional picture could be built up by feeding the output to a monitor as shown in figure 2a. The upper trace is the reference line correlated with the reference signal (the reference signal is only part of the reference line). Successive lines on the display show the correlation function from successive TV lines correlated with the reference signal. For simplicity, only 16 lines have been displayed. An alternative method of display is to use the correlation output to intensity modulate a raster scan synchronised to the TV frame.

The performance of the correlator was measured using a test pattern, consisting of eight grey levels, one per reference sample, offset by one bit on each succeeding line, and repeating after 8 lines. The correlator display from this test pattern is shown in figure 2a and the theoretical correlation functions are shown in figure 2b.

This form of one-dimensional correlator can be extended to perform two dimension spatial correlation for images which are available as raster scanned video. This is illustrated in figure 3 where a sub-frame taken from a complete TV frame may be correlated with other portions of the picture, perhaps over the duration of several frames, to detect the magnitude and direction of movements of objects in the field of view.

The video is clocked through the reference and signal channels of M correlators in cascade, with discrete time delays interleaved, so that each correlator-plus-delay stores the L elements of a complete TV line (or as much of it as needs to be processed). The clock waveform to the reference channel is inhibited when a complete line is stored. At that time the M correlators

between them hold the NxM sub-frame to be compared with the rest of the complete frame. The correlation output will now show a maximum but as the video continues clocking through the signal channels, the correlation will fall off as the picture decorrelates in the horizontal dimension, until a new video line enters the system. For typical TV images, a new correlation peak will occur when the signal preserved as a reference in one correlator occupies the signal register of succeeding correlators in the system. The heights of these peaks represent the degree of correlation between vertically displaced subframes.

If the reference is held over succeeding frames and the correlator output is used to give a display similar to figure 2, the position of the central peak would represent the best estimate of the direction, and extent of the movement, of an image included in the original picture, or alternatively might represent a drift in the boresight direction of the camera.

INTEGRATED CORRELATOR

A 32 bit integrated correlator chip has been designed using an n-channel poly-silicon gate technology. This device contains two 32 bit tapped CCDs, each incorporating facilities for feedback linearisation³. The signal register taps drive simple MOS multiplier circuits⁴ (figure 4), the outputs of which are taken via positive and negative coefficient bus-bars to current summing amplifiers. The amplifiers are at present off-chip, but have been fabricated in a CCD compatible technology to allow full integration in future designs. The reference register taps drive the other multiplier terminal via sample and hold circuitry to provide true four quadrant multiplication.

CIRCUIT DESCRIPTION

A floating gate reset technique^{1,5,6} was utilised for the tap circuitry. The multiplier circuit (figure 4) consists of two identical MOS transistors, the gates of which are driven in anti-phase about a quiescent voltage, V_B , by a phase splitter circuit. The phase splitter circuit is driven from the reference register, V_{ref} . The output of the signal register taps, V_{sig} , is applied to the drain terminals of

the transistors, the source terminals being connected to the positive and negative coefficient current summing amplifiers.

A first order approximation⁷ to the current flowing in the MOSTs is given by:-

$$I_D = \beta ((V_{GS} - V_T) V_{DS} - V_{DS}^2/2),$$

$$V_{DS} \leq V_{GS} - V_T$$

where β = constant

V_{GS} = gate to source voltage

V_T = threshold voltage

V_{DS} = drain to source voltage.

The difference in the drain currents flowing in the transistors is given by:-

$$\Delta I_D = \beta (V_{GS1} - V_{GS2}) V_{DS}$$

and since

$$V_{GS1} = V_B + V_{ref}$$

$$V_{GS2} = V_B - V_{ref}$$

$$\text{and } V_{DS} = V_{sig}$$

the difference in currents may be written as

$$\Delta I_D = 2\beta V_{sig} \times V_{ref}.$$

A more accurate computer simulation of the circuit indicates that a multiplication accuracy for typical signal levels of better than 1% can easily be achieved by careful design.

The operation of such a multiplier fabricated on 10 Ω .cm, p-type material, is shown in figure 5. The upper and lower traces are the reference and signal inputs respectively, the output is shown in the centre.

CONCLUSIONS

It has been shown that it is feasible to use CCDs in correlators. Practical techniques have been demonstrated allowing the

design of a fully integrated analogue correlator using CCDs. The adoption of these devices should enable high speed real-time processing systems of small size and low power consumption to be constructed.

ACKNOWLEDGEMENTS

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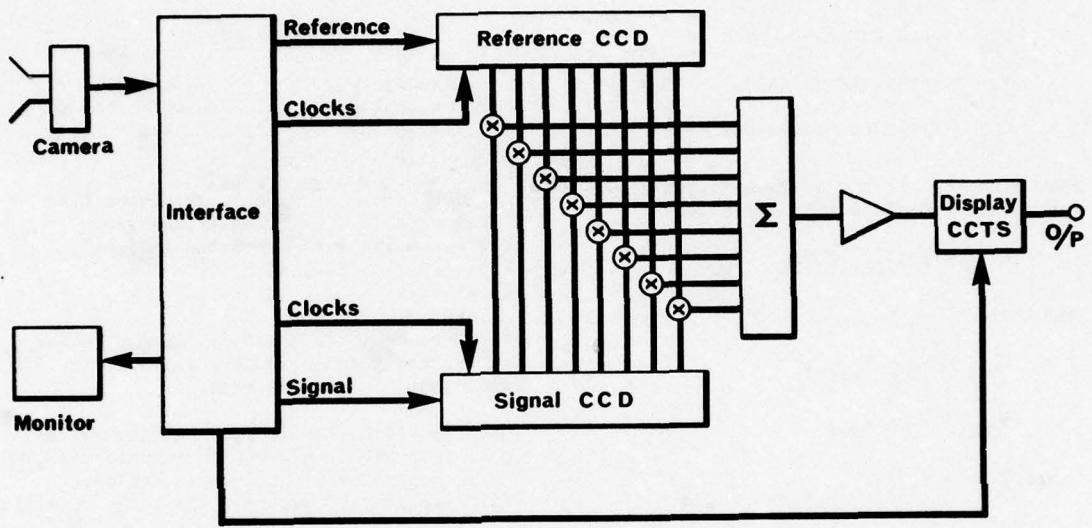


Fig. 1
Analogue correlator

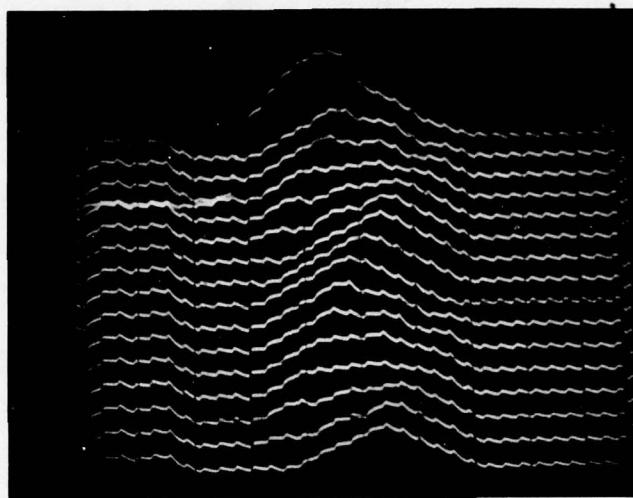


FIG 2A CORRELATOR OUTPUT

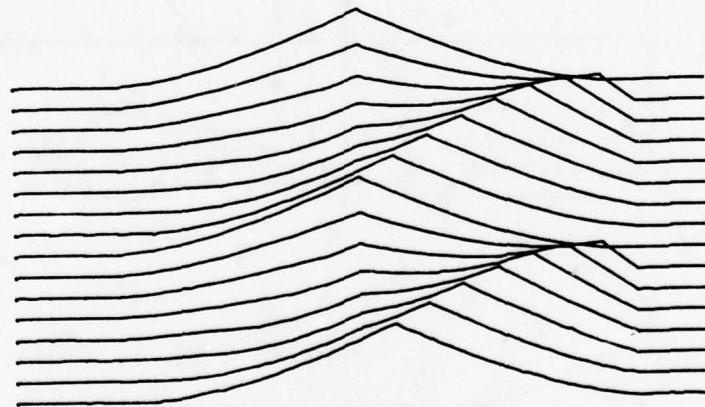


FIG 2B THEORETICAL OUTPUT

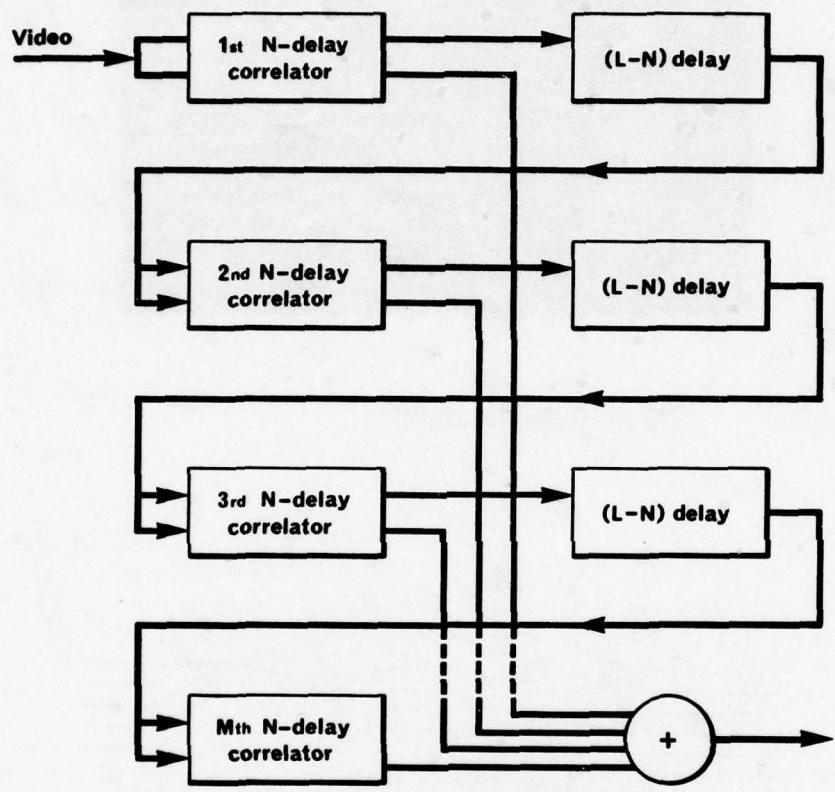


Fig. 3
Two dimensional correlator

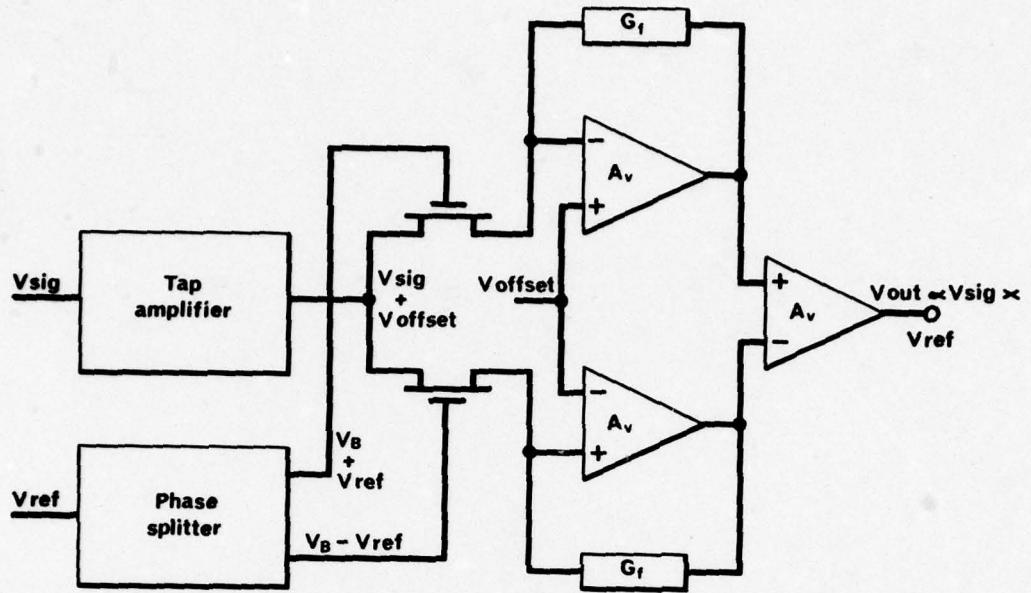
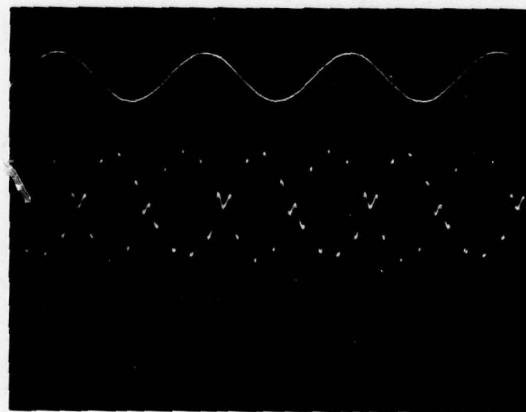


Fig. 4
4 Quadrant multiplier operation



Reference input 2V/Div

Multiplier output 0.5V/Div

Signal input 1V/Div

Time 50 μ s/Div

Figure 5 Multiplier Waveforms

DISCRETE-TIME ANALOG SIGNAL PROCESSING DEVICES
EMPLOYING A PARALLEL ARCHITECTURE

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ABSTRACT. Analog signal processing devices which use a parallel rather than a serial architecture will be described. These devices perform the functions of delay, time-base expansion/compression and binary/analog correlation. The fundamental operating principles as well as the unique advantages of a parallel architecture such as

1. Independent input-output,
2. The ability to do permuted as well as sequential sampling,
3. The realization of long retention time (exceeding 5 seconds at 25°C), and
4. The ability to read out non-destructively,

will be discussed.

Key features of each device as well as performance tradeoffs inherent in differing device designs will be discussed. Device characteristics and performance such as delay-bandwidth product, signal to noise, linearity, etc., will also be discussed.

The variety of applications for these devices is extremely broad. It ranges from low-frequency geophysical or medical instrumentation to high-frequency communications and radar. Specific applications which will be discussed include adaptive transversal filters, binary and p-n sequence correlators, transient recorders, and time-base correctors.

Sampled-data signal-processing devices for producing delay, frequency scale change, time-base expansion or compression, etc., may be devised using either parallel or serial storage architecture. The parallel architecture has unique advantages in flexibility, linearity, and speed which complement rather than compete with those of charge-transfer devices; each has its field of application. Of necessity comparisons with CTD will be made. Figure 1 lists in tabular form some of the salient features to be discussed. Some of these features are not necessarily unique to the parallel-

storage architecture, but parallel storage in many ways provides better means for exploiting the desired features.

Figure 2 is an updated version of a curve shown by Buss and Bailey about one and one-half years ago.¹ This updated version shows extension of the operating region into both a higher sampling-rate area and a longer time-delay area; both extensions are possible because of the parallel approach with its feature of independent input and output. Note that the independent control of input and output

permit operation within the area of the box above the $T_d W = 10^3$ line whereas the serial configuration only permits operation below the line. The parallel architecture thus allows considerable extension to permissible areas of operation.

To describe the devices and their features, let us take several concrete examples, each illustrating particular features or combinations. Figure 3 shows the simplified equivalent circuit for one fairly early example of the parallel-storage architecture. This particular device, called a Serial Analog Memory (SAM) because of its independence of input and output, has 64 memory cells. Two independent shift registers, one controlling the input and the second the output, sequentially activate elements from the two series of multiplex switches. The first register and its associated multiplexer sequentially time-samples an analog input signal, storing each of the samples on discrete capacitive storage cells. The second register and its associated multiplexer sequentially interrogate the memory elements, connecting successive stored values to the output line.

This device has a sampling-rate range from 5KHz to 12MHz and a greater than 55 db dynamic range. These devices have been successfully used in a number of applications ranging from simple time delay to time-base correction of video signals as obtained from video tape recorders.

Figure 4 shows a different example of the parallel architecture in the form of a 100-element Serial Analog Delay (SAD). Included in the figure is the peripheral control required. The device is similar to that of Figure 3 except that it does not have the independence of control of the input and output registers of Figure 3. Each of the delay channels in Figure 4 has 50 storage elements so arranged that each storage site is read out just prior to the receipt of a new sample, thus giving maximum delay. The two delay channels are normally processed in staggered fashion, thus giving a multiplexed 100-element delay unit. Additional delay or higher effective sampling rate can be achieved by

further multiplexing additional packages. Note that this multiplexing is free from problems of ghosting - there is no tailing of the signal in one packet into adjacent packets; each sample is and remains discrete and unique. Improvements in processing have permitted a dynamic range exceeding 66 db with permissible input levels up to a peak value of approximately 5 volts.

Figure 5 shows the simplified equivalent circuit of a Serial Analog Memory which has buffered readout of the memory. Along with the independent readin and readout capability, the buffering permits non-destructive readout as well as the interrogation of more than one memory cell at a time. A binary sequence entered into the output shift register can thus be correlated with the signal (analog or binary as desired) entered into the memory input. Figure 6 shows the correlation function of two binary sequences derived from the same source, illustrating the functioning of the correlator.

The ability of devices with buffered independent readin and readout to provide correlation processing has proved so important that special devices have been designed to perform more complex processing. Figure 7 illustrates the simplified circuit of such a device. This device, referred to as a Serial Analog Processor (SAP), in its simplest form is similar to the memory devices illustrated previously except that the output control is by means of a static shift register whose flip-flop elements control dual output buffer amplifiers. Each memory cell is connected to two buffers, one to give positive or unit weighting, the other negative or zero weighting. Further, the static shift register may have its data circulated in either direction. Buffer outputs are in the form of currents which are collected by the positive- or negative-weight output lines. Thus, binary correlation may easily be obtained as above. If the circulation is reversed, convolution may be obtained.

The above devices are limited to a zero or one for each weight value. However, it is possible to parallel circuits such as

the above to obtain four-bit or greater quantization of each weight. Such a combination is not limited to binary signals; it permits discrete time correlation or convolution of two analog signals (one of which is converted to a binary quantized form). But correlation is the foundation for discrete-time filters, so that highly sophisticated discrete-time filters may be simply, easily and economically built. The manifold advantages of discrete-time processing are combined with the speed and convenience of analog processing to give an extremely flexible, highly precise key element for all forms of transversal and recursive filters, as well as being applicable to the more obvious correlation and convolution processing. A schematic arrangement is illustrated in Figure 8.

SAP devices have been made with 16, 32, 64 and 128 cells (or filter taps); four such devices can then give any of 16 possible positive weights (or 16 negative weights) to each tap.

Two other developments permitted by the parallel architecture are in late stages of development. The first takes advantage of recent technology to obtain very low residual thermal pair excitation (leakage) and hence very long memory retention times - of the order of ten seconds. Such devices have all the desirable features of the family such as high sampling-rate capability, wide dynamic range, good linearity, etc., with the added capability to operate at very low clock frequencies to give long delay, etc. Figure 9 illustrates performance of this device. The lower trace shows the input signal (with an abrupt frequency change). The upper trace shows the output signal with a delay of approximately 9 seconds. In 35 seconds, stored amplitude decayed to approximately 80% of initial amplitude.

The second development capitalizes further on the parallel-storage architecture to permit decoded random selection of the input storage sequence. Thus arbitrary time-slot selection of filter-tap elements is possible. A filter or processor of new and

unique characteristics thus becomes possible.

In summary, the parallel architecture has features complementary to those of charge-transfer devices. Certain of those features such as convolution processing and decoded input-sequence selection are possible only with the parallel architecture; others are more easily and effectively implemented in the parallel form, for example the multi-bit weighting of a multi-tap device. Finally, the physical processing is such that functions such as switching and storage are more easily optimized in the parallel architecture.

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FEATURES OF PARALLEL PROCESSING ARCHITECTURE

1. INDEPENDENT INPUT AND OUTPUT
 - a. TIME SCALE CHANGES
 - b. CORRELATION AND CONVOLUTION PROCESSING POSSIBLE
2. POSSIBILITY OF NONDESTRUCTIVE READOUT
 - a. REPEATED READOUT
 - b. ISOLATION
3. REALIZATION OF VERY LONG RETENTION TIMES
4. THE ABILITY TO PERFORM PERMUTED AS WELL AS SEQUENTIAL SAMPLING
5. HIGH SAMPLING RATE WITHOUT SUFFERING TRANSFER INEFFICIENCY
6. LINEARITY AND WIDE DYNAMIC RANGE
7. PERFORMANCE DIRECTLY RELATED TO CELL AREA

Figure 1. Advantages Available with a Parallel Processing Approach

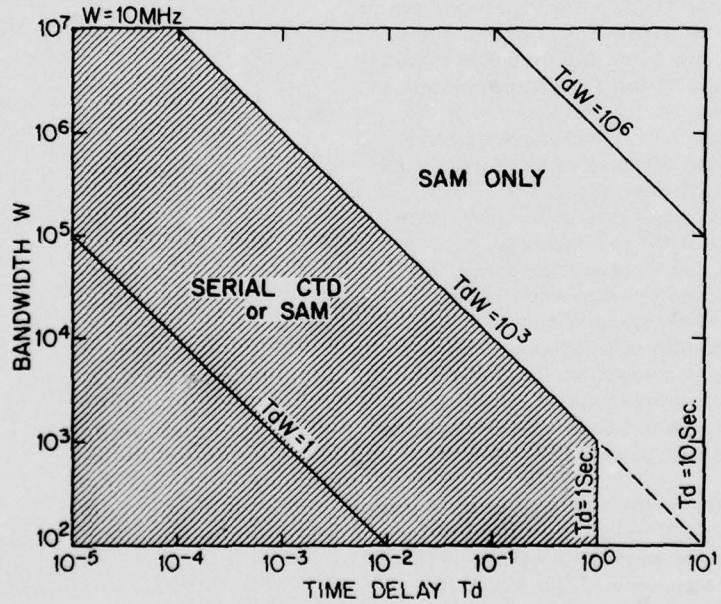


Figure 2. Useful Time Delay vs. Bandwidth

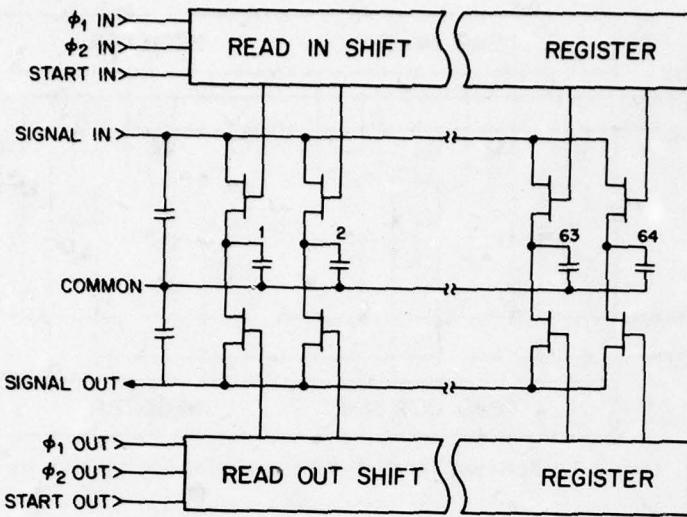


Figure 3. Parallel-storage Serial Analog Memory

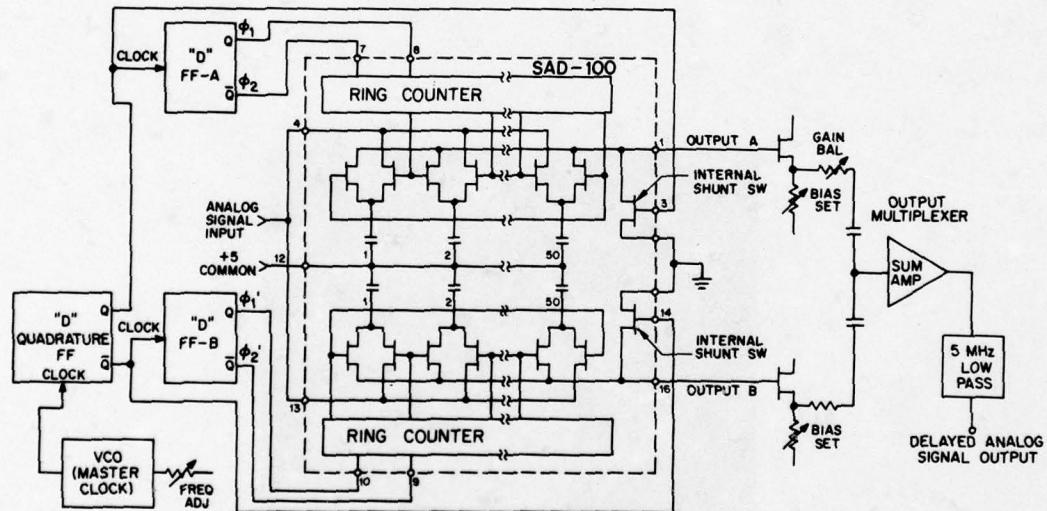


Figure 4. Duplex Parallel-Storage Serial Analog Delay

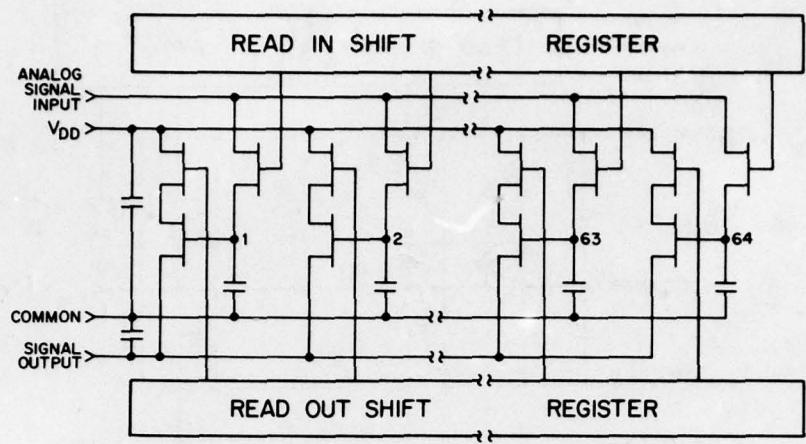


Figure 5. Buffered Parallel-storage Serial Analog Memory

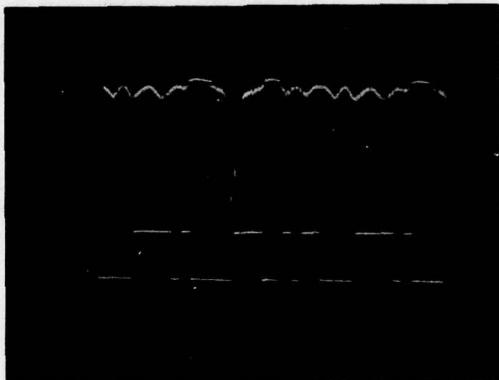


Figure 6. Correlation Oscillogram Obtained for Two Binary Sequences Using the Buffered Serial Analog Memory of Figure 5.

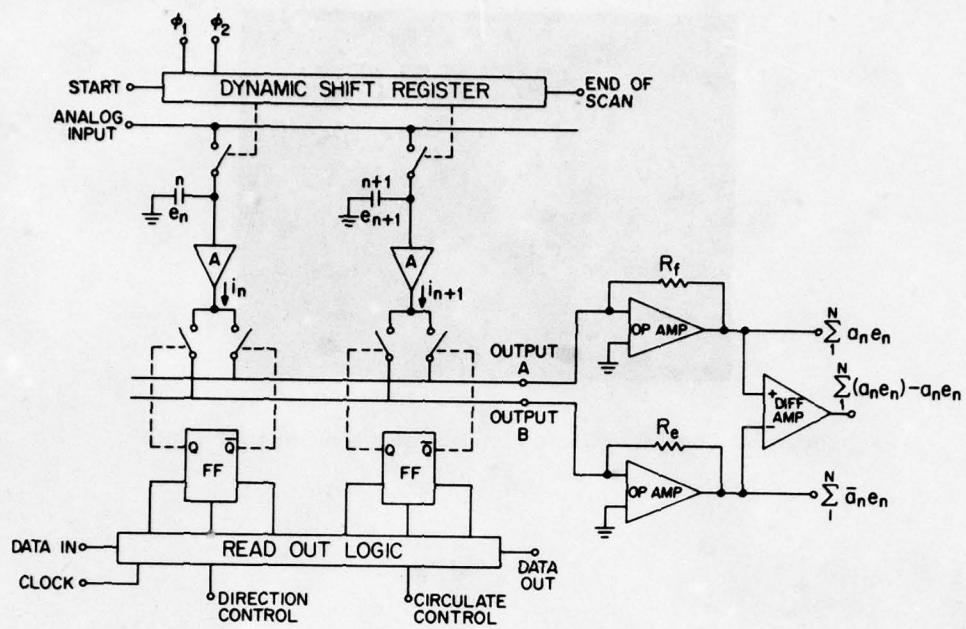


Figure 7. A More General Serial Analog Processor

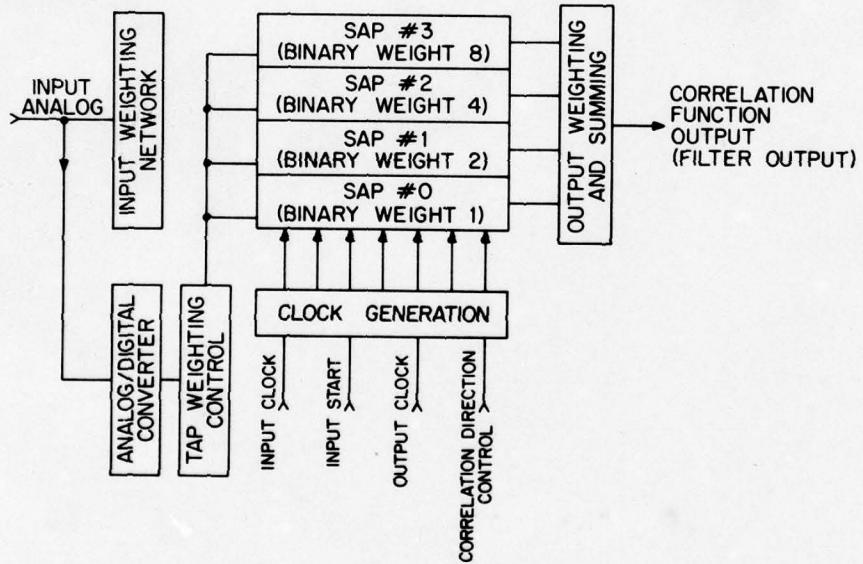


Figure 8. Schematic Diagram for a 4-bit Serial Analog Processor

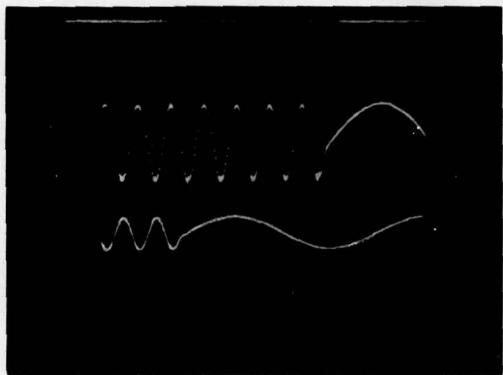


Figure 9. Retention Characteristics of a Long-retention SAM

MULTIPLE FILTER CHARACTERISTICS USING A SINGLE CCD STRUCTURE

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ABSTRACT

The split electrode approach to the design and implementation of on-chip tap weights has been generalized to obtain several types of filter functions using a single CCD delay line. The concept was used to implement two types of transversal filters using a 32 stage 2 phase CCD delay line. The θ_1 storage electrodes were split to obtain a low-pass filter whereas the θ_2 storage electrodes were split to obtain a bandpass filter.

The design and operation will be described and the theoretical and experimental characteristics will be compared. An analysis of the tap weight errors introduced by design layout aids will be presented. The advantages and limitations of this technique will be compared to the single filter approach.

INTRODUCTION:

The use of CCD's in transversal filter applications have been discussed in the literature(1-5). In all these studies a single CCD delay line was used to obtain a single type of filter frequency response. Although different CCD structures and technologies have been used in the implementation, the design principles are similar. The on-chip tap weights were achieved by splitting one of the CCD storage electrodes of every delay stage. The tap weight values were obtained by varying the split location along the channel width and differentiating between the charge signal on the two outputs. The output was obtained either by floating gate voltage sensing⁽²⁾, or current sensing methods^(1,4). The trade-off between the two methods are in the linearity and dynamic range of the filter output. Using these approaches lowpass, bandpass and highpass filters have been fabricated. Typical filter parameters of 50dB rejection in the stopband, ripples of less than 0.2dB in the passband and linearity of 50dB were experimentally obtained.^(2,4)

The purpose of this paper is to discuss the performance of CCD transversal filters

where a single CCD was used to obtain two different types of filters.

DEVICE DESCRIPTION

Figure (1) shows a schematic diagram of the structure as applied to the two phase CCD's. As shown, not only θ_1 storage electrodes are split to form one type of filter function but also θ_2 storage electrodes are split to obtain another type. Each clock phase has a positive and negative output. The circuit was designed to operate with the floating gate voltage sensing technique as shown in Figure (2a). Figure (2b) shows the timing diagram for the circuit operation. For signal sensing under θ_1 electrodes, θ_1 goes high and the potential of the floating gates increases positively until θ_{1S} is applied. Through bootstrap action, the potential at A becomes stable and the electrodes are left floating. At this point θ_2 goes low and charge is transferred to the floating gate causing a drop in the surface potential. This change is measured at the source follower output using sample and hold pulse θ_{1S} . A similar reset and sample and hold timing scheme is applied on θ_2 floating gate

electrodes.

Figure (3) shows the test chip used to evaluate the structure. It consists of 33 stages of CCD delays. A 32 tap lowpass and 32 tap bandpass filters were implemented under θ_1 and θ_2 storage electrodes respectively using split electrode technique. The 33rd stage was used to monitor the output charge signal for efficiency of transfer measurements. The structure was fabricated using n-channel two-level polysilicon gate technology on 3Ω cm p-type silicon substrate. Input and output logic and timing circuitry were fabricated on the same chip using n-channel MOS transistors. Also protection against surge pulses were fabricated on the address lines.

At the split in each electrode a floating diffusion was used to couple the two channels under the positive and negative sections. Thus the surface potential across the channel will be equal. In the current sensing method, where a constant voltage is maintained on the gate, the diffusion will equalize the charge density in both sides and consequently when the next transfer occurs the charge will split according to the new capacitive ratio. The charge equalization could have been established during the transfer process if a true four phase clocking system had been used. However, in the devices discussed here, the sample & hold pulse has to occur as shown in Figure 2(b), immediately after the charge transfer, so that the voltage change is measured before surface potential equalization can be established.

A LINFIR (Linear phase impulse response) program, which is an adaptation of the Parks, McClellan and Rabiner⁽⁶⁾ program, was used for the design and performance measurement of Linear phase transversal filter. Also a MCPPOST (Monte Carlo post processor) program was used to analyze the effect of random tap weight errors. The layout and process errors have been compensated for, using inhouse developed CAD program. Figure (4) shows the impulse frequency response of the two filters.

The operation will be described and the theoretical and experimental characteristics will be compared. An analysis

of tap weight error introduced by design layout aids will be presented. The advantage and limitation of this design technique will be compared with the with the single filter approach.

ACKNOWLEDGEMENT:

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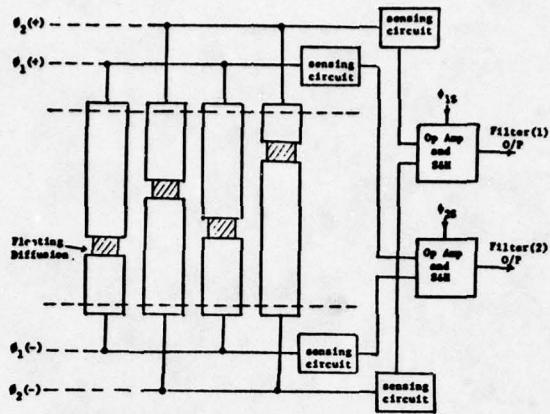


FIGURE 1 - Implementation of split electrode approach under θ_1 and θ_2 storage electrodes.

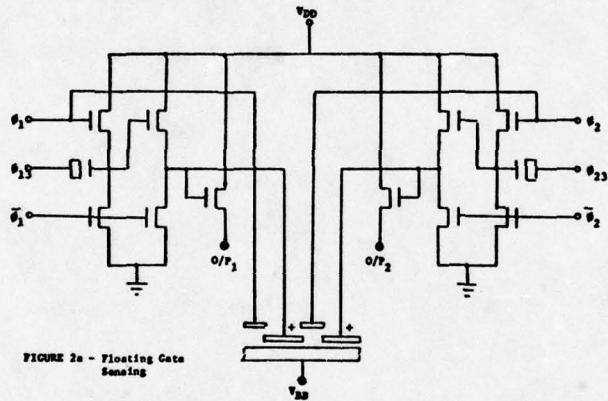


FIGURE 2a - Floating Gate Sensing

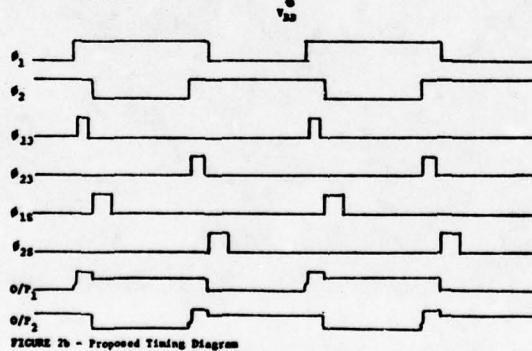


FIGURE 2b - Proposed Timing Diagram

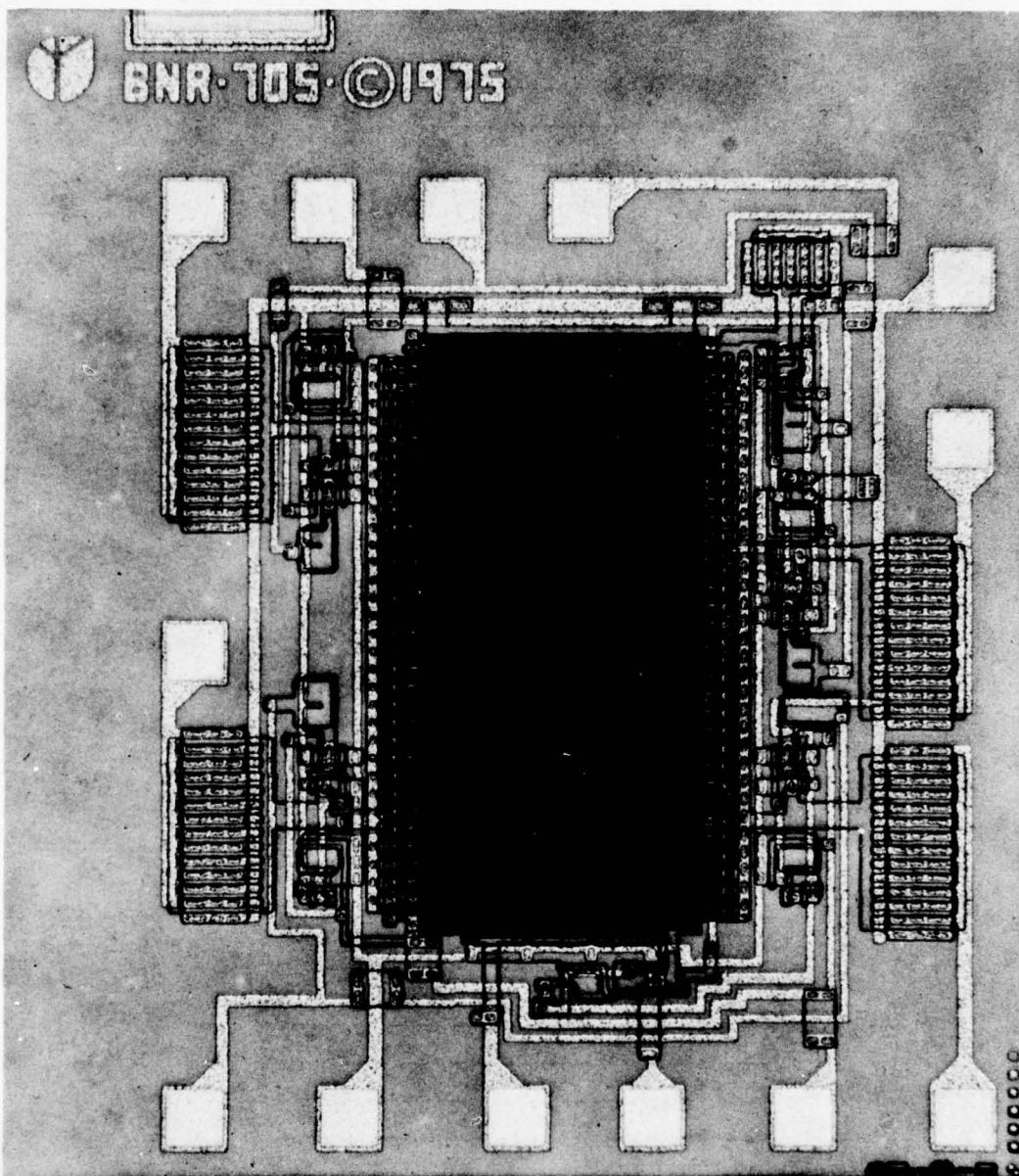
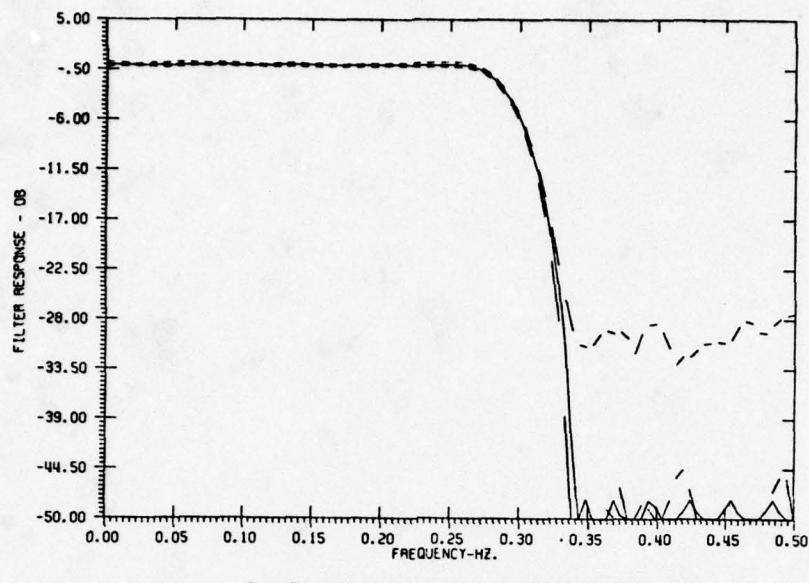
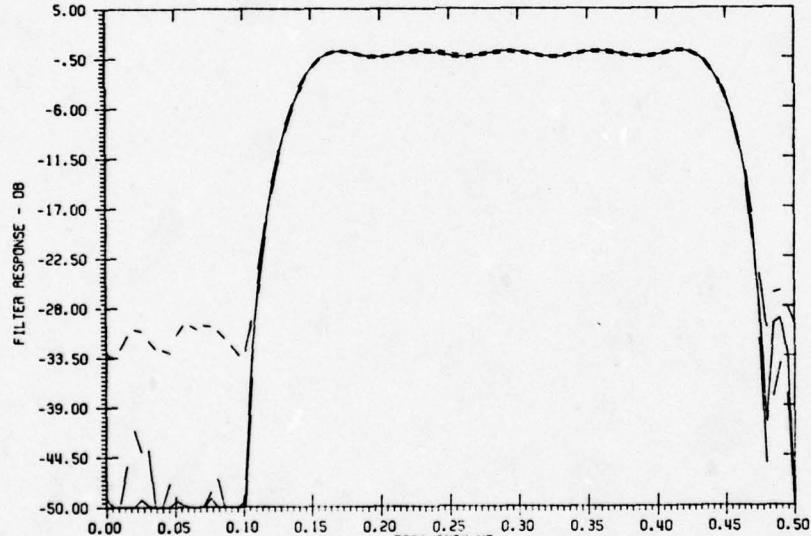


FIGURE 3 - FABRICATED TEST CHIP



C.C.D. TRANSVERSAL FILTER RESPONSE
SOLID LINE = IDEAL RESPONSE
BROKEN LINE = WORST CASE MONTE CARLO



C.C.D. TRANSVERSAL FILTER RESPONSE
SOLID LINE = IDEAL RESPONSE
BROKEN LINE = WORST CASE MONTE CARLO

FIGURE 4 - SIMULATED FREQUENCY RESPONSE

APPLICATIONS OF A CCD LOW-PASS TRANSVERSAL FILTER

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ABSTRACT The application of a CCD low pass filter to several different systems is described. These applications include; a channel filter for a frequency division multiplex communication system, an anti-alias filter for a time division multiplex communication system, an anti-alias filter for a digital monitoring system and an interface between two asynchronous sampled data systems.

I. INTRODUCTION

Low pass filters are required in a large number of systems. In some cases the required filter characteristics are easily obtained with simple passive networks, but in many cases, system performance can be improved if higher performance filters are used. Until now, it may not have been economically attractive to use higher quality filters in these applications, but with the advent of low cost CCD low-pass transversal filters having very sharp cut-off characteristics and low in-band ripple, many opportunities now exist for improving cost/performance by upgrading the quality of the low pass filters.

Sampled data analog systems, for example, all require a low pass filter for the elimination of alias responses. This filter must have a pass band that is adequate for the signal bandwidth, but for typical applications it must be down by 40 to 50 dB by the Nyquist frequency. In the past, this has been accomplished by oversampling the data by

a factor of three or four so as to move the Nyquist frequency sufficiently far above the signal pass band that a relatively simple filter can suffice. While this practice simplifies the filter, it requires that three to four times as many samples be stored, processed, or transmitted (depending on the system) as are actually needed.

In these cases, a low-pass filter with sharper cut-off characteristics can reduce the number of samples that have to be stored (thereby effecting a cost saving in memory) or processed (thereby effecting a saving in CPU loading) or transmitted (thereby effecting a saving in bandwidth).

Sampled data systems whose pass bands are close to the Nyquist limit also pose problems at the output end. Since the sample rate is only about one octave above the pass band edge, it is also necessary to employ a high quality low pass filter at the output of these systems.

The function of the CCD low-pass filter is to perform an interpolation between the output samples, thereby increasing the sample rate without appreciably changing the signal spectrum.

An experimental CCD low-pass filter has been designed and tested, and the application of this filter to a number of systems has been explored. The frequency characteristics of this filter are first presented, and the application of this filter to the following systems is then discussed in detail:

- A. Frequency division multiplexed channel filter.
- B. Alias filter for time division multiplexed communication system.
- C. Alias filter for digital patient monitoring system.
- D. Interface between two asynchronous sampled data systems.
 - 1. Video communications system.
 - 2. ERTS image processor.

II. FILTER CHARACTERISTICS

The low-pass filter discussed in this paper was designed for the frequency division multiplexed communication application discussed in the following section. The pass band for each channel extends from 200 Hz to 3200 Hz, and the channels are to be frequency division multiplexed on 4.0 KHz centers. Thus, the stop band to pass band ratio required is $4.2/3.2 = 1.31$.

Within the pass band, the ripple may not exceed 0.1 dB, and the adjacent channel suppression must be greater than 34 dB. Using the Parks and McClellan algorithm,⁽¹⁾ a 63 tap

filter design was generated where the pass band and stop band edges were chosen to be 0.1 and 0.131 times a clock frequency of 32 KHz, respectively.

The resulting tap weight values were rounded off to the closest of 600 discrete values to accommodate the automatic mask making apparatus that was used to generate the art work for the chip, thereby introducing a tap weight roundoff error of at most one part in 1200 at each tap. A comparison between the calculated and measured performance of this filter is shown in Fig. 1.(2)

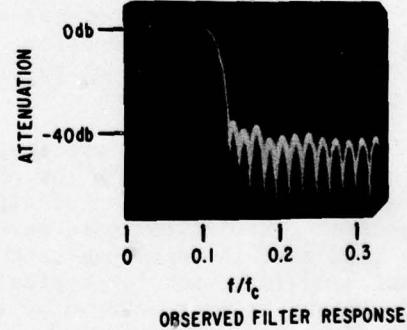
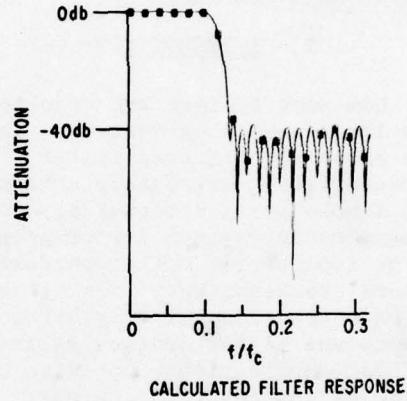


Fig. 1-CCD low pass filter response

A tap weight accuracy of the order of 0.1° due to random processing variations can be achieved in practice.^(3,4) This is comparable to the roundoff error.

III. SYSTEM APPLICATIONS

A. FREQUENCY DIVISION MULTIPLEXED CHANNEL FILTER

In this application, each channel is represented as a single side-band signal of 3.0 KHz bandwidth (200 Hz-3.2 KHz) with channels on 4.0 KHz centers. These channels are conventionally separated with a bank of high quality band pass elliptic filters whose outputs are then modulated to the audio range. Although this approach could be implemented directly with appropriate CCD band pass filters, the passive band pass filter cannot be eliminated because of the alias responses of the CCD. A preferable approach from the point of view of cost appears to be to perform the band pass function with low pass filters rather than with band pass filters.⁽⁵⁾ This introduces a problem of image rejection, which is not present when band pass filters are employed, but it can be solved either by phase cancellation or by using the Weaver method. In the Weaver method, the desired channel is first modulated to base band I and Q channels with appropriate modulators, and these are low pass filtered and combined to form the desired audio signal as shown

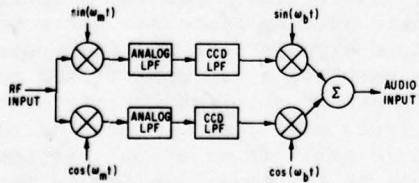


Fig. 2-Block diagram of Weaver demodulator

in Fig. 2.

In the CCD implementation, which is inherently a sampled system, the function of the modulators can be provided automatically by the samplers themselves. Since these samplers can be operated from a frequency divider driven by a single clock running at four times the sample rate, a precise 90° phase shift can be obtained without using any critically balanced components.⁽⁶⁾ A block diagram showing this implementation is shown in Fig. 3.

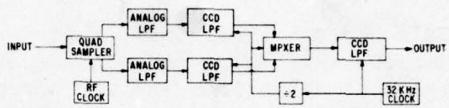


Fig. 3-CCD implementation of Weaver demodulator

In addition to the CCD low pass filter, an analog filter must also be employed to eliminate the alias response of the CCD. For the filter described above, where the pass band extends to .13 times the sample rate, the analog filter must be down by about 40 dB at .87 times the sample rate. This can be accomplished by a three pole filter (one pole on the real axis plus one conjugate pair) and can be implemented with a single op-amp. The responses of the CCD filter and the three pole Chebyshev filter are shown superposed in Fig. 4. Since the combined response is the product of the two individual filters, the net result is a single sharp cut-off low pass filter with no alias responses.

Previous attempts to use the Weaver method have been limited by phase tracking errors in the low pass filters. This problem is considerably alleviated by using

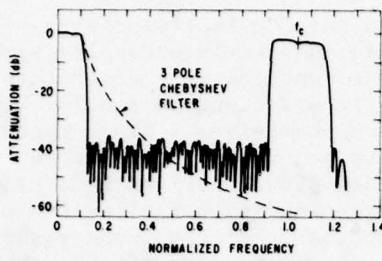


Fig. 4-Alias response of CCD filter and 3 pole Chebyshev anti-alias filter

CCD's because their phase shift characteristics are independent of component variations and are therefore much easier to control. Excellent band pass characteristics were obtained as shown in Fig. 5, and suppression of spurious responses by an average of 45 dB was achieved as indicated in Fig. 6.

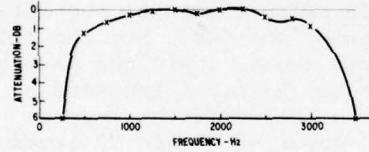


Fig. 5-Band pass characteristics of the CCD Weaver demodulator

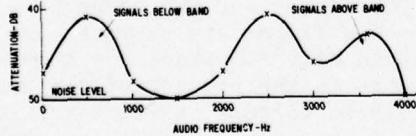


Fig. 6-Out of band suppression of the CCD Weaver demodulator

B. TIME DIVISION MULTIPLEXED COMMUNICATIONS SYSTEM

In this system, 24 audio channels are low pass filtered and sampled at 8.0 KHz, and these samples are multiplexed and converted to a digital data stream by a single A/D converter and transmitted. At the receiving end, the samples are converted back to analog by a single high speed D/A converter and demultiplexed in the analog domain. In this application, the most significant aspect is cost. CCD low pass input filters appear advantageous because most of the overhead circuitry can be shared by all of the filters. Under these conditions, the trade-off is between two or three active filter stages with precision trimmed components and the CCD filter chip and its associated level-shift and signal recovery circuits. From the point of view of component count, this trade-off is approximately equal, but in terms of component tolerance and immunity to component drift, the CCD approach appears preferable.

C. DIGITAL MONITORING SYSTEM

The amount of risk associated with recovery from serious illness can be dramatically reduced by continuous monitoring of physiological data such as the electrocardiogram. Since the warning signs contained in these data are sometimes quite subtle, digital processing appears to be the most practical approach for automatically providing appropriate warning signals. Since the output signals from the transducers are sampled, a low pass filter must be provided to prevent distortion due to frequency folding. This filter should fall off as sharply as possible so that oversampling is not required, but to prevent phase distortion, it should also have a linear phase response. A further

complication is the relatively low cut-off frequency required. (For an ECG waveform, a bandwidth of about 50 Hz is appropriate.) The conventional solution to this problem is to use a low pass filter with a cut-off frequency several times higher than necessary and to oversample by a factor of two or three. This approach reduces the bulk of the filter and permits good phase response, but memory requirements and processor speeds are increased. In this application, the linear phase and sharp cut-off characteristics of CCD filters such as the one described above provide a more optimum solution. The cut-off frequency can be reduced to the appropriate value with no increase in component size or degradation of phase response, so operation up to about 80% of the Nyquist limit becomes practical. This means that the digital system only sees about half as many samples for a given bandwidth as in the conventional approach, and it therefore can handle more patients.

D. INTERPOLATION

There are a number of cases where a continuous analog signal needs to be recovered from a sampled data system. This is usually done by holding each sample for the duration of each clock period and passing the resulting staircase waveform through a low pass filter. If this output signal has to be sampled a second time, and if the clock frequency of the first sample rate gets through the low pass filter, the clock frequency components may be folded back by the second sampling operation and cause alias distortion. Although this problem is usually not severe, it can be a problem when the signals represent video images. In this case, phase distortion is not acceptable, and conventional low pass filters cannot be used. Two

examples where this problem has appeared are:

1. A sampled data video transmission system in which the clock frequencies of the camera, the transmission link and the display are all asynchronous.
2. The generation of rectilinear raster data from raw ERTS data. In this case, the direction of the scan lines from the satellite data do not conform to the raster direction, and the spacing of the scan lines does not conform to the spacing of the raster lines. One approach toward generating the interpolated data for the output raster is to reconstruct a band limited continuous signal from the samples of raw data and to resample this continuous signal at the points corresponding to the pixel locations along the raster.

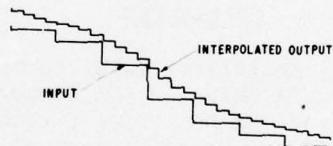


Fig. 7-An example of interpolation.

This approach can be conveniently implemented with CCD low pass filters of the type described above followed by a simple analog filter.

The function of the CCD is to provide a large number of interpolated sample values at a higher sample rate than that of the input samples as shown in Fig. 7. The output sample stream can be filtered by a much simpler analog filter than would have otherwise been required because the clock frequency has now

been moved much farther away from the signal pass band.

IV. ACKNOWLEDGMENTS

The CCD transversal filter has involved the participation of a number of people. W. E. Engeler was responsible for the initial design concepts. H. S. Goldberg has performed device evaluation and circuit development. C. M. Puckette was responsible for the tap weight design and has been concerned with tap weight error. O. M. Mueller of GE Telecommunications Products Dept. has evaluated the devices in a communications application. R. C. Sherick has evaluated CCD's in the Weaver demodulator. D. Meyer and J. F. Richotte have been responsible for device fabrication, and L. J. Petrucco for circuit fabrication. Finally the authors would like to thank J. O. Quesnel for preparing this manuscript.

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SAMPLED ANALOG CCD RECURSIVE COMB FILTERS

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ABSTRACT - Sampled analog comb filters using a recursive implementation with CCD's as the delay elements are studied. A theoretical analysis based essentially on digital recursive filters is developed with modifications taking into account that a CCD delay generally consists of more than one delay stage. Using the standard Z and the bilinear Z transforms, transfer functions of a lowpass and a highpass continuous filter are transformed into $H(Z)$ forms suitable for CCD implementations. Design formulas for both the canceller type and integrator type comb filters using one CCD delay are obtained. Six different comb filters are implemented using an 8-bit two-phase P surface channel CCD clocked at 20 kHz. The agreement between measurements and theoretical calculations is encouraging. Possible causes for the deviation from theory are discussed. The bilinear Z transform design procedure is shown to be superior because it provides a zero in the transfer function which leads to theoretically infinite attenuation at a series of periodically separated null frequencies. Applications of this type of comb filter to either suppress or to enhance a signal having periodic spectrum are suggested. The work performed was partially supported by the Naval Electronics Systems Command and the Naval Postgraduate School Research Foundation.

1. INTRODUCTION

Designers of sampled analog CCD signal processors have concentrated mainly on transversal filters,(1,2,3) correlators,(4) chirp Z transformers,(5,6) and two-dimensional transforms.(7,8) This paper discusses sampled analog recursive filters, which have not received as much prior attention. They were first studied using a BBD as the delay elements (9,10) and, recently, a three-pole(11) and a two-pole/one zero(12) CCD recursive filter and a one-pole CCD recursive integrator (13) have been reported.

This paper addresses three aspects of sampled analog CCD recursive comb filters: theory, experimental results, and possible applications. The general characteristics of comb filters are highlighted in Section 2, and their recursive implementations are described. In Section 3, a theoretical analysis based essentially on digital recursive filter theory is

presented. Modifications of the digital theory to fit the sampled analog recursive filter case are provided. Measured results of recursive comb filters using an 8-bit, two-phase, P surface channel CCD delay line are presented and compared with theoretical calculations in Section 4. The agreement is generally close at low frequencies but deteriorates as the frequency is increased or as the order of comb teeth is increased. However, the feasibility of using a CCD to implement a recursive comb filter is confirmed. Possible applications using this type of comb filter are discussed in Section 5.

2. COMB FILTER AND RECURSIVE IMPLEMENTATION

Comb filters are characterized by their periodic transfer characteristics in the frequency domain. They can be classified into two general types. The first type is the bandstop or canceller type

shown in Figure 1a. It has strong attenuation in a narrow neighborhood of a series of periodically separated frequencies and good transmission in between. The second type is the bandpass or integrator type shown in Figure 1b. It has good transmission in a narrow neighborhood of a series of periodically separated frequencies and strong attenuation in between.

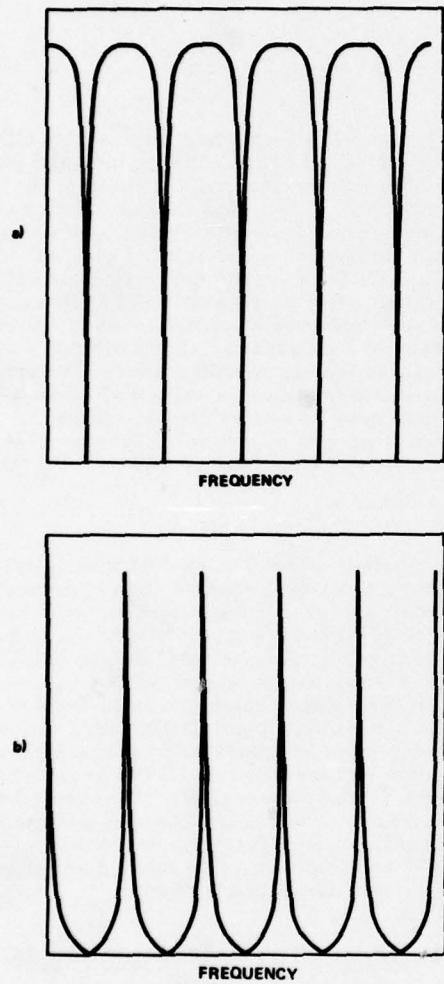


Figure 1. Frequency Characteristics of Two General Types of Comb Filters - Bandstop, Canceller Type, and Bandpass, Integrator Type

Both analog comb filters (17, 18, 19) and digital comb filters (20, 21) have been developed based on several different implementation techniques: feedforward, frequency sampling, (22) fast Fourier transform, and recursion. All use delay devices in some manner.

In the analog case, a quartz delay line has been the major candidate. For digital, the delay device is the shift register. However, a new family of comb filters is being developed using a different type of integrated circuit delay device, such as the BBD (bucket brigade device), CCD (charge coupled device), and SAD (serial analog delay). (23) In these, analog signals are first sampled and then delayed. As a result of the sampling, these devices not only have standard analog properties but also some digital properties such as aliasing and stability of delay.

Using these integrated circuit delay devices, sampled analog comb filters are being developed based on the feedforward circuit, (11, 14, 15) chirp Z transform, and recursive filter implementations. (9, 10, 11, 12)

We are studying the recursive implementation using the canonical circuit shown in Figure 2. The results presented use only one CCD delay device, i.e., $b_2 = 0$, $a_2 = 0$. However, the delay device consists of N delay stages (in the experimental study, $N = 8$). As shown in later sections, the presence of N stages of delay in

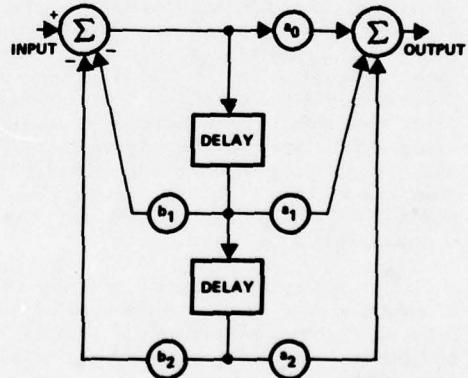


Figure 2. Canonical Form of a Second Order Recursive Filter

one delay device can be used to advantage in providing the comb feature of the frequency characteristics and also very large attenuation between these comb teeth.

The reason for this is that, since the signal is delayed N clock periods before it is fed back to the input, the frequency of recursive operation, f_r , is only one N^{th} of the clock frequency, f_c (or sampling frequency). Therefore, the frequency characteristics of the recursive filter are periodic with the frequency f_r . Since $f_r = f_c/N$, there are $N/2$ teeth within the Nyquist frequency range from 0 to $f_c/2$. This is in contrast to the usual digital recursive filters where the recursions take place after each delay stage, resulting in only one comb tooth within the Nyquist range. Since there are now $N/2$ teeth, a proper design procedure which introduces a zero at the recursion frequency f_r will provide infinite attenuation, in principle, at each of these teeth even when only one delay element is used. The procedure is known as the bilinear Z transform.

3. THEORY

Since the sampled analog recursive filters are implemented by the same circuit configurations used for digital recursive filters, we know intuitively that the theory of digital recursive filters should apply. However, proper modifications must be made to account for the fact that the signal is now sampled-analog and that the delay device now consists of N delay stages instead of one.

It is known that two general design approaches have been developed for the IIR (infinite impulse response) type digital recursive filter. The first approach is indirect. It starts with the transfer function in the Laplace transform variable S of a continuous filter and follows by digitizing the transfer function $H(S)$ into a transfer function in the discrete time variable Z. Many different transforms are employed such as mapping by differential transform, impulse invariant (standard Z) transform, bilinear Z transform, and matched Z transform. The second approach is a direct digital design in either the frequency domain or the time domain using some type of computer aided design procedure.

We feel that the direct approach using the frequency domain is probably more

instructive, and we will present it in this paper using two of the four transforms listed earlier (standard Z transform and bilinear Z transform).

The modification used to take into account the fact that one CCD delay device consists of N delay stages will be described. In conventional digital filter theory, Z^{-1} is used to represent a delay of one clock period. For a recursive filter using only one CCD device of N delay stages, the transfer function is

$$H(z) = \frac{a_{Nz}^{-N} + a_0}{b_{Nz}^{-N} + 1} \quad (1)$$

In other words, it is actually an N^{th} order recursive filter but with many of its coefficients, $a_{N-1}, \dots, a_1, b_{N-1}, \dots, b_1$, equal to zero.

The analysis can be simplified greatly if we consider the N clock delay stages as "one recursion" delay stage with its corresponding recursion frequency $f_r = f_c/N$, then the transfer function is simplified to

$$H(z) = \frac{a_1 z^{-1} + a_0}{b_1 z^{-1} + 1} \quad (2)$$

with the understanding that Z^{-1} actually consists of N clock periods of delay and that its frequency characteristics are periodic with respect to f_r and have $N/2$ comb teeth in the frequency range from 0 to $f_c/2$, the Nyquist limit. Because there is now more than one period in the frequency characteristics (or more than one tooth), the effects due to sampling and/or the sample and hold circuit should be taken into account in the theory. Only the effect due to the sample and hold circuit is considered in this paper, and it is discussed in Section 4.

Using this straightforward modification and the well developed digital recursive filter theory, a set of design formulas was derived for a first order lowpass filter

$$H(S) = \frac{\omega_x}{S + \omega_x}$$

and a highpass filter

$$H(S) = \frac{S}{S + \omega_x}$$

where $\omega_x = 3$ dB corner frequency. The following two transforms are used:

$$\text{Standard Z transform } Z = e^{ST}$$

$$\text{Bilinear Z transform } S = \frac{2}{T} \frac{Z-1}{Z+1}$$

where $T = N \frac{1}{f_c}$, the CCD delay.

Table 1. Summary of Design Formula of Sampled Analog Recursive Comb Filter Using One CCD Delay

Design Method	Filter Type	Coefficients		
		a_0	a_1	b_1
Standard Z	Lowpass, integrator $\frac{\omega_x}{\omega_c} < \frac{1}{4}$	ω_x	0	$-e^{-\omega_x T}$
	Lowpass, canceller $\frac{\omega_x}{\omega_c} > \frac{1}{4}$	$1 - \omega_x$	$-e^{-\omega_x T}$	$e^{-\omega_x T}$
	Highpass, canceller $\frac{\omega_x}{\omega_c} < \frac{1}{4}$	$1 - \omega_x$	$-e^{-\omega_x T}$	$-e^{-\omega_x T}$
	Highpass, integrator $\frac{\omega_x}{\omega_c} > \frac{1}{4}$	ω_x	0	$e^{-\omega_x T}$
Bilinear Z	Lowpass, integrator $\frac{\omega_x}{\omega_c} < \frac{1}{4}$	$\frac{\omega_x T}{\omega_x T + 2}$	$\frac{\omega_x T}{\omega_x T + 2}$	$-\left \frac{\omega_x T - 2}{\omega_x T + 2} \right $
	Lowpass, canceller $\frac{\omega_x}{\omega_c} < \frac{1}{4}$	$\frac{\omega_x T}{\omega_x T + 2}$	$\frac{\omega_x T}{\omega_x T + 2}$	$\left \frac{\omega_x T - 2}{\omega_x T + 2} \right $
	Highpass, canceller $\frac{\omega_x}{\omega_c} < \frac{1}{4}$	$\frac{2}{\omega_x T + 2}$	$\frac{-2}{\omega_x T + 2}$	$-\left \frac{\omega_x T - 2}{\omega_x T + 2} \right $
	Highpass, integrator $\frac{\omega_x}{\omega_c} > \frac{1}{4}$	$\frac{2}{\omega_x T + 2}$	$\frac{-2}{\omega_x T + 2}$	$\left \frac{\omega_x T - 2}{\omega_x T + 2} \right $

Without presenting the derivations in detail, the results are summarized in Table 1. It should be pointed out that an approximation, $\tan \omega/\omega_c \approx \omega/\omega_c$, was used. The cases of integrator type comb filters and canceller type comb filters are listed separately. They are determined by the relative signs of the coefficients a_0 , a_1 , and b_1 . The theoretical frequency characteristics of six special cases are presented as solid curves in Figures 3 through 7. The cases that have been implemented and measured experimentally are summarized in Table 2. The coefficients have all been normalized to unity. Their comb filter characteristics are also plotted in relative amplitudes in Figures 3 through 8. In Figure 8, the theoretical comb filter characteristics are modified by taking into account the effect of the sample and hold circuit. This introduces a factor of $\sin(\pi k/N)/(wk/N)$, where k = the order of the comb tooth. Discussions relating to this correction are given in Section 4.

Table 2. Summary of Six Experimental Sampled Analog Recursive Filter Cases

Design Method	Filter Type	Coefficients			Figure
		a_0	a_1	b_1	
Standard Z	Highpass, integrator	1	0	0.7	3
	Lowpass, integrator	1	0	-0.3	4
	Lowpass, canceller	1	1	0.7	5
	Lowpass, canceller	1	1	0.3	6
	Lowpass, integrator	1	1	-0.9	7
	Highpass, integrator	1	-1	0.7	8

NOTE: 8-bit, 2 phase, surface channel CCD (Figure 9)

$f_c = 20$ kHz

Circuit schematic (Figure 11)

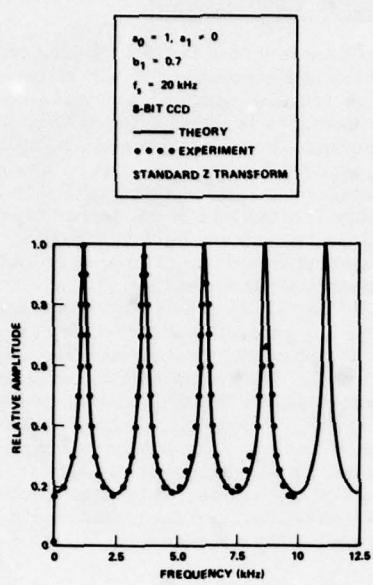


Figure 3. Highpass Integrator Filter – Frequency Characteristics

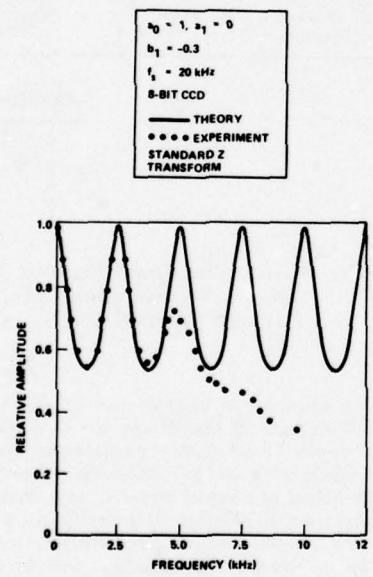


Figure 4. Lowpass Integrator Filter – Frequency Characteristics

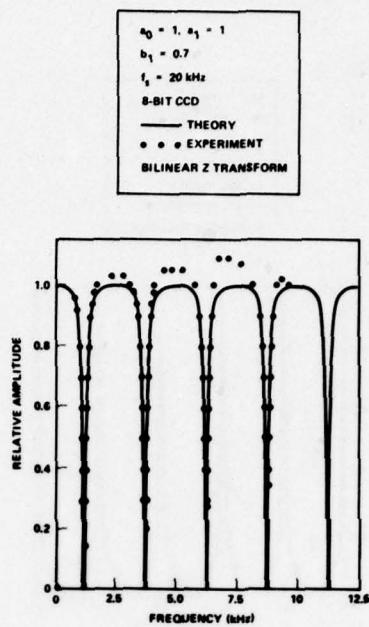


Figure 5. Lowpass Canceller Filter – Frequency Characteristics

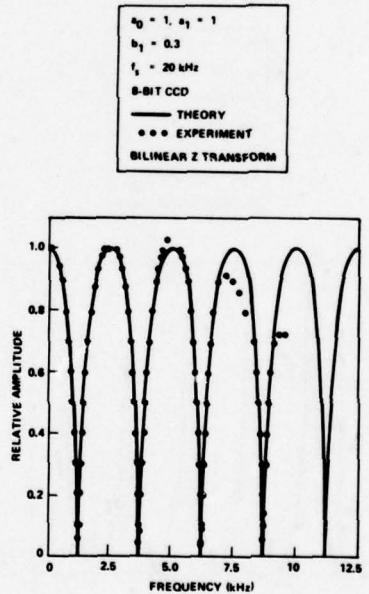


Figure 6. Lowpass Canceller Filter – Frequency Characteristics

4. EXPERIMENTS, COMPARISONS, AND DISCUSSIONS

To demonstrate the feasibility of using CCD as delay elements for the implementation of sampled analog recursive comb filters and also to verify the validity of the theoretical analysis presented in Section 3, six cases of comb filters are implemented. They are listed in Table 2. The table includes both canceller type and integrator type comb filters whose Z transform transfer functions were obtained from both lowpass and highpass continuous filters. The CCD used is a two-phase, overlapping gate, P surface channel, 8-bit CCD. Its physical description is presented in Figure 9. Its output circuit consists of a reverse biased floating diode, gated by a reset MOSFET and followed by a MOSFET source follower. The load resistor is connected off the chip. Its input circuit consists of one diode, pulsed to a forward biased condition, and four gates with appropriate dc bias applied.

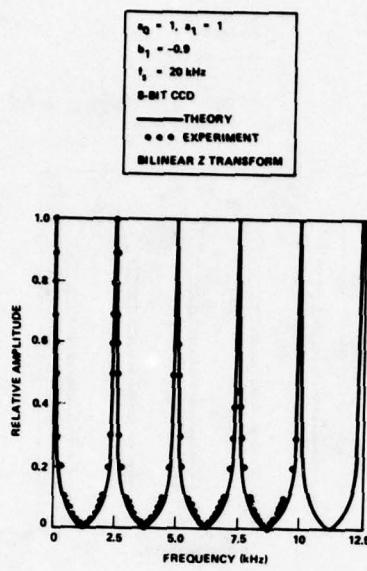


Figure 7. Lowpass Integrator Filter – Frequency Characteristics

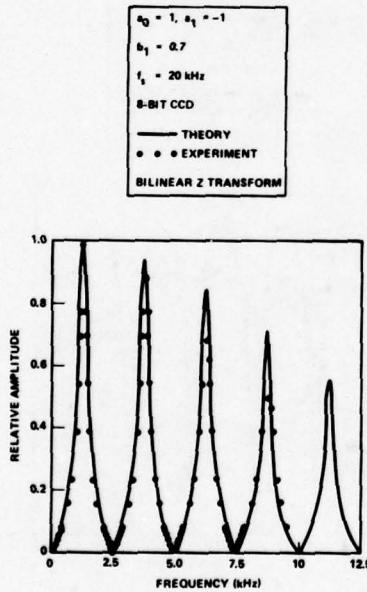


Figure 8. Highpass Integrator Filter – Frequency Characteristics

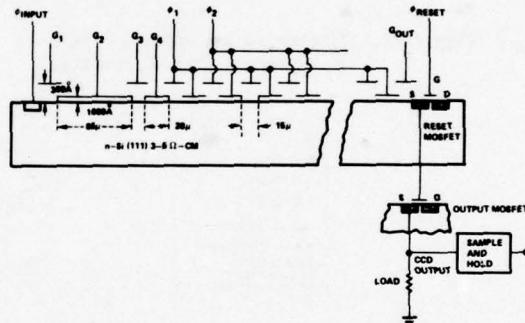


Figure 9. Cross-Sectional View of Two Phase, Overlapping Gate, P Surface Channel CCD

The electrical signal can be fed into the CCD either at the diode or at a gate. In this study, an input signal technique known variously as the surface potential equilibration method, the fill and drain method, or the scuppering method is used. To carry out this input procedure, a clock pulse is applied to the diode, and dc voltages of various levels are applied to the gates. The signal is applied to one of the gates. The combination of third and fourth

gates provides one of the widest dynamic ranges, as shown in Figure 10. The figure presents the output voltage measured after the sample and hold circuit as a function of the input signal expressed by a varying dc voltage level at the third gate. The bias voltage on the fourth gate is held at selected values. The operating conditions are described as follows:

- Four clock pulses:

ϕ_{input} = input diode pulse level from -12.8 to -2.4 V

ϕ_{reset} = reset MOSFET gate pulse level from -37.5 to -19 V

ϕ_1, ϕ_2 = 50% duty cycle CCD clock pulses from -22.5 to -10 V

- Four dc gate biases:

G_1, G_2 biased at -30 V

G_{out} and V_{DD} at -35.5 V

Load resistor = 50K ohms

Clock frequency = 20 kHz.

From Figure 10, it can be seen that two operating modes exist. The first is a high gain mode occurring in a third gate voltage range from approximately -11.7 volts to values from -11.9 to -12.5 volts, depending on the bias voltage on the fourth gate. This mode is quite nonlinear. The

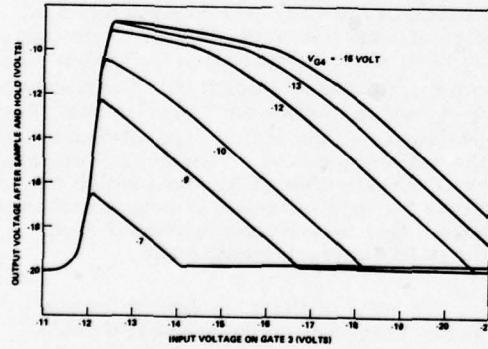


Figure 10. Input G_3 vs Output Characteristics of Two Phase Surface Channel 8 Bits CCD

second mode is characterized by a much lower gain but occurs over a much wider bias range on G_3 . The range is more than 8 V for $V_{G4} = -15$ V. For $V_{G4} = -12$ V, it can be seen that a section of the mode characteristics is linear from -16.9 to -20.5 V. Therefore, the combination of $V_{G3} = -18.7$ V and $V_{G4} = -12$ V was chosen as the electrical bias condition. The ac input signal was applied to the third gate to carry out the frequency response measurements. In this way, a linear range of approximately 3.7 V was obtained.

The circuit schematic for the comb filter measurements is shown in Figure 11. The coefficient $a_0 = 1$ is easily implemented by direct connection. The coefficients $a_1 = \pm 1$ and the different values of b_1 were implemented by using two potentiometers connected after the sample and hold circuit and the level shifter. Operational amplifiers with the proper feedback were used to provide the two summation operations.

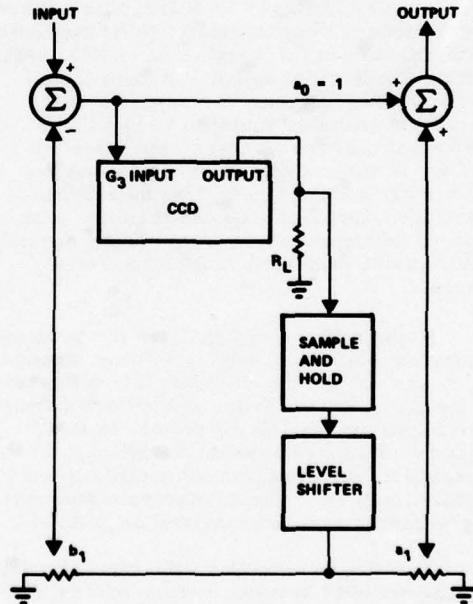


Figure 11. Circuit Schematic of CCD Recursive Filter Experiment

The measured frequency characteristics of six comb filters are presented as dots in Figures 3 through 8. Figures 3 and 4 are filters designed by the standard Z transform procedure. Figures 5 through 8 are filters designed by the bilinear Z transform procedure. The filter type and corresponding filter coefficients are shown in each figure and are also listed in Table 2. The advantage of the bilinear Z transform design procedure over the standard Z transform is clear by noticing the theoretically infinite attenuations achieved at the null frequencies separated by the recursion frequency, $f_r = f_c/N = 20 \text{ kHz}/8 = 2.5 \text{ kHz}$.

In conventional filter designs, large attenuations in the stop bands can be achieved by using higher order filters in the case of recursive filters and by using many bits of delay in the case of nonrecursive filters. In this case of sampled analog recursive comb filters, infinite attenuation is theoretically achieved even in cases where only one delay element is used. Of course, the reason for such an interesting property is that the delay element has N stages of delay; this causes its frequency characteristic to be periodic with respect to f_c/N and to have $N/2$ teeth within the Nyquist range. A zero introduced by the bilinear Z transform will force the transfer function to zero at a series of null frequencies separated by f_c/N . In the conventional digital recursive filter design where N equals 1, the zero introduced causes the transfer function to become zero at frequencies beyond the Nyquist limit and is therefore not useful.

It should be noted that, in the preliminary experimental study, infinite attenuation was not found. Instead, the measured attenuation varied from -60 dB down from the maximum to -10 dB down. In fact, this is but one of several deviations of measured results from theoretically calculated values. The agreements and disagreements are summarized as follows.

For the first tooth of the comb filter, the agreement between theory and experiment is excellent in all six cases. However, measured values and calculated values started to deviate from each other as the frequency increased or as the order of the comb tooth increased. On the one

hand, the attenuation at the null frequencies for the bilinear Z cases started to deteriorate. On the other hand, the filter shape did not always stay in close agreement with the theoretical results. However, different trends of deviation were discovered.

In four cases (Figures 3 and 4 for the standard Z transforms and Figures 7 and 8 for the bilinear Z transforms), the measured frequency response steadily became lower than the calculated response. The worst case is shown in Figure 4. Such a decrease could be caused by several factors including effects due to the sample and hold, effects due to charge transfer inefficiency, and effects due to the frequency rolloff of the electrical instrumentation. In Figure 8, the effect due to the sample and hold circuit is included in the theoretical calculation. However, its rolloff effect does not adequately account for the measured decrease. This suggests that other factors must be considered. The explanation for these deviations is made more complicated by the opposing trend shown in Figures 5 and 6 for two other bilinear Z transform cases. Here the measured frequency responses are higher than the calculated values. We are only beginning to search for the factors which could cause such increases.

The general deterioration of the attenuation at null frequencies is considered to result from two effects. The first is the change of a_1 as a function of frequency; this includes the effects of frequency variations in the CCD, the sample and hold circuit, and the level shifter. Note that a_0 is directly connected to the output summing operational amplifier. The imbalance of a_0 and a_1 makes the "zero" a less than perfect zero and yields less attenuation at the null frequencies. The second effect is the general noise background which prevents the measurement of very small signals. One major contribution of such noise is the clock feedthrough.

In spite of these deviations of measured results from theoretical calculations, it is proper to conclude that the feasibility of using a CCD to implement sampled analog recursive comb filters is confirmed,(10,11,12) and the basic approach of a theoretical analysis based

essentially on the digital recursive filter theory is correct to the first order. Obviously, refinements are needed to extend the success of the theory at the first comb teeth to all higher order teeth.

5. APPLICATIONS

The range of applications of sampled analog recursive filters is obviously very broad. However, it is important to recognize that the performance of this type of filter is somewhere between that of analog and digital filters. Compared with regular analog filters, the delays of this family of integrated circuit electronic delay devices are controlled by the main clock pulse, and these IC filters do not have nearly the narrow bandwidth and time and temperature drift problems which plague other analog filters. They are as stable as the main clock. Compared with digital filters, they process signals in sampled analog form, thus avoiding the expense of A/D converters and digital multipliers, though there are penalties of somewhat lower performance and relatively more limited programmability. Another feature of sampled analog recursive filters is the possibility of time shared filtering because the delay elements generally have more than one stage.⁽¹⁵⁾

They are particularly useful as comb filters. Their periodic transfer characteristics make them well suited to process signals which are periodic in time and in frequency such as most radar and sonar signals. Canceller type comb filters can be used to reject periodic signals by aligning the null frequencies of the comb filter with the periodic frequency spectrum of the undesired signal. This is indeed the principle of both the feedforward and recursive filters⁽¹¹⁾ being developed to cancel clutter spectrum in MTI radars. Also, because the delay can be changed rather conveniently by changing the main clock frequency, the canceller type sampled analog comb filter may simplify the signal processing in either staggered PRF or jittered PRF radars.

In a different direction, integrator type comb filters can be used to enhance periodic signals contaminated by noise and/or interferences. A video integrator is being developed⁽¹³⁾ based on this principle.

6. CONCLUSIONS

Sampled analog comb filters by recursive implementation have been studied. A theoretical analysis based essentially on digital recursive filter theory was used to calculate the frequency characteristics of both the canceller type and the integrator type comb filters, using only one delay element. The fact that the delay element has N delay stages is used to achieve the comb feature of the transfer characteristics. Using the zero introduced by the bilinear Z transform, infinite attenuations are achieved at null frequencies, which is a very desirable feature. Six calculated cases were selected for implementation using an 8-bit CCD as the delay element. The agreement between measurements and theory is excellent at the first set of comb teeth and varying degrees of closeness are achieved as the order of comb teeth is increased. The causes for this are under study. Studies are in progress to extend this work to cases where more than one delay element is used and to examine the reasons why the experimental results at higher order comb teeth are at variance with some of the theoretical predictions.

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COMPARISON BETWEEN THE CCD CZT AND THE DIGITAL FFT

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ABSTRACT. The CCD analog transversal filter is a tremendously cost-effective component in terms of its simplicity compared to equivalent digital hardware. In view of this, the chirp z-transform (CZT) algorithm for performing spectral analysis is ideally suited to CCD implementation because, in this algorithm, the bulk of the computation is performed in a transversal filter. The CCD CZT has some performance limitations relative to the digital fast Fourier transform (FFT), and for this reason, it is not applicable to all military signal processing systems. However, for those applications which fall within the CCD performance capabilities, the CZT offers significant potential cost saving over the digital FFT. The performance of the CCD CZT is evaluated and compared with the digital FFT. A discussion is given of selected military applications where the CCD CZT can be used to advantage.

I. INTRODUCTION

Charge-coupled device (CCD) analog transversal filters can be used to perform the discrete Fourier transform (DFT) on electrical signals using an algorithm called the chirp z-transform (CZT).^{1,2} The CCD CZT has been demonstrated,^{3,4} and it has been proposed as a replacement for the digital fast fourier transform (FFT), in a number of military signal processing applications.⁵ It is the purpose of this paper to compare the CCD CZT with the digital FFT.

In a general way, the comparison can be summarized as follows. The CCD CZT has performance limitations when compared with the digital FFT, and it is somewhat less flexible. However, it has a tremendous projected cost advantage when manufactured in high volume, and has additional advantages in smaller size, lighter weight, lower power and improved reliability. Although the CCD CZT has modest performance, significant cost advantages can be realized for those applications which fall within its performance capabilities. It is the goal of this paper to quantitatively compare the CCD CZT with the digital FFT and to identify a few major military applications in which the CCD CZT is certain to be important.

Section II reviews conventional digital spectrum analysis techniques; the digital FFT and the deltec spectrum analyzer. Section III discusses the CCD CZT and a related prime transform. Section IV compares the CCD CZT with the digital FFT in error, resolution and implementation, and Section V discusses selected military applications of modest required performance for which the CCD CZT has clear cost advantages over digital implementation.

II. REVIEW OF DIGITAL SPECTRAL ANALYSIS METHODS

The FFT is currently the most widely used technique for digital spectral analysis. It is important because it requires only $N/2 \log_2 N$ complex multiply operations to perform an N -point DFT, as compared with N^2 complex multiply operations required to directly implement the DFT formula

$$F_k = \sum_{n=0}^{N-1} f_n e^{-i2\pi nk/N} \quad (1)$$

The deltec spectrum analyzer historically preceded the FFT, and has been largely replaced except in certain sonar spectrum analysis applications.

FFT

The FFT algorithm is discussed from an elementary point of view in References 6, 7 and 8. In this section, it will be reviewed for the purposes of establishing nomenclature for discussion in later sections.

FFT algorithms can be classed as decimation in time or decimation in frequency. The former is discussed here, but the latter is quite similar. The most common FFT algorithms are radix 2, meaning that the entire FFT is performed by sequential operations involving only pairs of elements. The fundamental operation in a radix 2 FFT is the so-called butterfly which takes two complex inputs A and B and combines them to give X and Y through the operation

$$\begin{aligned} X &= A + W_N^k B \\ Y &= A - W_N^k B \end{aligned} \quad (2)$$

where $W_N \equiv \exp[-j2\pi/N]$, and the W_N^k are the so-called twiddle factors. The butterfly structure is indicated schematically in Figure 1a, using the notation of Reference 8.

An 8-point, radix 2, decimation-in-time, FFT algorithm is illustrated in Figure 1b. The data are first reordered by bit reversal,⁸ and the first set of butterflies essentially performs the 2-point DFT on the re-ordered input data by pairs. The second set of butterflies combines the 2-point DFT's using twiddle factors to achieve two 4-point DFT's on the even and odd numbered input data. The final set of butterflies combines the 4-point DFT's using twiddle factors to achieve the final 8-point DFT.

Several important facts about radix 2 FFT's are apparent from the above discussion: (1) N must be an integral power of two. (2) There are $\log_2 N$ stages each requiring $N/2$ butterfly operations for a total of $N/2 \log_2 N$ butterflies required, and (3) Each Fourier coefficient is processed through $\log_2 N$ butterfly operations so that quantization errors are cumulative.

In many applications, the FFT is used to obtain a transform which will later be inverted to obtain the original signal. In such applications, the phase of the transform must be maintained. However, in many other cases it is desired to obtain a measure

of the spectral energy density of a quasi-periodic waveform or a quasi-stationary random process. For these applications, the phase of the transform is not important. In addition, the true DFT is not performed, but the input data are apodized or windowed by an appropriate windowing function w_n to suppress frequency sidelobes in the spectrum.^{6,7,8} The desired result is

$$|F_k|^2 = \left| \sum_{n=0}^{N-1} f_n w_n e^{-j2\pi nk/N} \right|^2 \quad (3)$$

For even moderate values of N the computational saving of the FFT algorithm is extremely significant, and for common spectrum analysis applications the savings is easily a factor of 10 to 100. The FFT is flexible enough and powerful enough to be considered a general purpose spectrum analysis tool.

DELTIC SPECTRUM ANALYZER

The deltic spectrum analyzer has been implemented in analog, digital and hybrid technologies. It is essentially a straightforward implementation of equation (1) in which the time series f_n is stored in a circulating delay line, usually in digital form. A complete circulation of the time sequence is performed in the time between each newly acquired input sample. During this circulation, the f_n are operated on either digitally or analog to form a spectral estimate at a selected frequency. To obtain a complete spectrum at N frequencies requires N^2 operations. However, N is not restricted to be a power of 2, and the frequencies are not restricted to be of uniform spacing as in the DFT. Often, one-bit quantization is used to represent the f_n . This minimizes hardware requirements but results in significant detection loss and small signal suppression effects.⁹

III. CCD SPECTRAL ANALYSIS TECHNIQUES

From the standpoint of minimizing the number of digital operations required to perform the DFT, the FFT algorithm is optimal. However, in determining the optimum algorithm for implementation with analog CCD's, a whole new set of ground rules exists. It is no longer important to minimize multiplications, because CCD transversal filters can be built which perform a large number of multiplications simultaneously in real time.^{10,11,12,13,14,15} Consequently, for

CCD implementation, algorithms should be selected in which the bulk of the computation is performed by a transversal filter. Two such algorithms have been identified for cost-effective CCD implementation; the CZT^{1,2} and the prime transform.^{16,17} Both algorithms are discussed in this section.

CCD CZT

The DFT can be performed using the chirp z-transform (CZT) algorithm.² The CZT gets its name from the fact that it can be implemented by (1) premultiplying the time signal with a chirp (linear FM) waveform, (2) filtering in a chirp convolution filter, and (3) postmultiplying with a chirp waveform. When implemented digitally, the CZT has no clear cut advantages over the conventional FFT algorithm.² However, the CZT lends itself naturally to implementation with CCD transversal filters.¹

Starting with the definition of the DFT given in equation (1), and using the substitution

$$2nk = n^2 + k^2 - (n - k)^2 \quad (4)$$

the following equation results:

$$F_k = e^{-i\pi k^2/N} .$$

$$\sum_{n=0}^{N-1} (f_n e^{-i\pi n^2/N}) e^{i\pi(k-n)^2/N} \quad (5)$$

This equation has been factored to emphasize the three operations which make up the CZT algorithm. It is illustrated in Figure 2.

To implement the conventional N-point CZT, the CCD filters are chirp filters of length $2N-1$ which chirp from $-f_c$ to $+f_c$, and the premultiply waveform has a time duration N/f_c and chirps from zero to $-f_c$. A physical interpretation in terms of correlation of the input chirp with the filter is given in Figure 3. When the input signal has zero frequency, the product with the premultiply chirp results in an input waveform to the filter which chirps from 0 to $-f_c$. The samples corresponding to frequencies near $f = 0$ are clocked into the filter first, and those near $f = -f_c$ are clocked in last. This sequence of samples results in a correlation peak at $t = t_o$, when the product wave-

form has been clocked into the first half of the filter. When the input frequency is $f_1 \neq 0$, the product with the premultiply chirp results in an input to the filter which chirps from f_1 to $-f_1 + f_c$. The input waveform ($V_{in} \times \text{chirp}$) in Figure 3 corresponds to an input signal at a frequency f_1 at time $t = t_o$. This waveform is shifted to the right as t increases resulting in a correlation peak at t_1 . The shift in time relative to the dc correlation peak is

$$t_1 - t_o = \frac{N}{f_c^2} f_1 \quad (6)$$

In this way, the time axis of the output is calibrated in frequency. The postmultiply is needed to obtain the proper phase of the DFT coefficients and can be omitted when phase is not required.

Several undesirable features of this implementation become apparent from the above description. The output must be blanked during the loading of the chirp into the filter, and the input must be set to zero during the calculation of the coefficients. Also undesirable is the inefficient use of the CCDs since only half of the CCD filter has useful information at any point in time.

For DFT applications, such as video bandwidth reduction,¹⁸ in which the transform is to be inverted to regain the original signal, the CZT is performed in the way described above. However, when the spectral density is required, the CZT can be simplified greatly. Using the substitution of equation (4) in equation (3) gives

$$|F_k|^2 = \left| \sum_{n=0}^{N-1} f_n w_n e^{-i\pi n^2/N} e^{i\pi(k-n)^2/N} \right|^2 \quad (7)$$

In this case, simplification of the CZT algorithm results from two observations: (1) The postmultiply operation can be eliminated and (2) The sliding CZT can be used.

The sliding DFT is defined in this paper to be

$$F_k^S = \sum_{n=k}^{k+N-1} f_n e^{-i2\pi nk/N} \quad (8)$$

and it gives a windowed power density spectrum

$$|F_k^s|^2 = \left| \sum_{n=0}^{N-1} f_{n+k} w_n e^{-j2\pi nk/N} \right|^2 \quad (9)$$

$$= \left| \sum_{n=0}^{N-1} f_{n+k} w_n e^{-j\pi n^2/N} e^{j\pi(k-n)^2/N} \right|^2 \quad (10)$$

Comparison of equations (9) and (10) with equations (3) and (7) indicates that the sliding CZT differs from the conventional CZT in that the sliding CZT indexes the data each time a spectral component is calculated. For a periodic waveform, indexing results in a phase factor which does not affect the result, and for a stationary random signal, the time record is different for each spectral component but stationarity insures that the result is unaffected. For these two classes of signal the sliding CZT gives the same result as the conventional CZT.

Figure 4 gives a pictorial comparison between the conventional CZT and the sliding CZT for the simple case of a 3-point transform. With the conventional CZT, all three Fourier coefficients F_0, F_1, F_2 are calculated using the first three time samples f_1, f_2, f_3 . These coefficients are being calculated by the filter during the next three clock periods, so that time samples $f_4 - f_6$ must be blanked. Then the cycle repeats as shown in Figure 4a. Using the sliding CZT, F_0^s is calculated on the sample record f_1, f_2, f_3 as before, but F_1^s is calculated on the sample record f_2, f_3, f_4, f_5 on the record f_3, f_4, f_5 , and the next F_2^s computation is made on the sample record f_4, f_5, f_6 . The sample record is continually updated by replacing the oldest sample with a new one. The above description shows that N Fourier coefficients are obtained for N time samples (100% duty cycle).

The advantages of the sliding CZT are (1) For an N -point transform, N -stage filters are required which chirp through a bandwidth f_c ($-f_c/2$ to $+f_c/2$ for example). (2) No blanking is required. The filters operate with 100% duty cycle; i.e., one spectral component out for each time sample in. (3) Windowing can be achieved by weighting the chirp impulse response of the filter with

the desired window function. (4) The degradation due to imperfect charge transfer efficiency is less for the sliding CZT than for the conventional CZT.

The block diagram for obtaining the spectral density using the sliding CZT is shown in Figure 5. The rectangles represent CCD filters having impulse responses $w \cos \pi n^2/N$ and $w \sin \pi n^2/N$, $-N/2 < n < N/2-1$. This system has been implemented using 500-stage CCD filters. The window function is coded into the metal photomask and systems have been demonstrated both without windowing ($w_n = 1$) and with Hamming windowing.⁵ Spectra obtained using Hamming windowing are shown in Figure 6.

CCD PRIME TRANSFORM

Another algorithm exists for computing the DFT which is also suitable to CCD implementation in the analog domain because the bulk of the computation is performed in a transversal filter.^{16,17} The prime transform algorithm is implemented in 3 steps as indicated in Figure 7; (1) permutation of the input data, (2) Transversal filtering and (3) permutation of the output Fourier coefficients. (for details see Reference 17) The advantages of the prime transform over the CZT are (1) the multipliers are replaced by permuting memories. (This may or may not be an advantage depending upon the speed and dynamic range required) and (2) For a real input, only two filters are required instead of the four shown in Figure 5. The disadvantages are (1) the zero order Fourier coefficient (dc term) must be computed separately (2) Imperfect charge transfer efficiency does not result in a simple degradation in resolution as it does in the CZT and (3) The sliding DFT cannot be implemented with the prime transform.

The CCD prime transform has not yet been tested but preliminary estimates suggest that it may be important for applications in which (1) the phase of the DFT is required thus ruling out the sliding CZT and (2) high speed and high dynamic range make on-chip multipliers difficult to implement.

IV. PERFORMANCE COMPARISONS

In this section some important comparisons are made between the CCD CZT and the digital FFT. Perhaps the most important point of comparison is accuracy. CCD's,

being analog, limit the accuracy of the CCD CZT. The major CCD limitations are (1) Charge transfer efficiency (CTE) (2) thermal noise (3) accuracy of the filter weighting coefficients (4) accuracy of the pre and post multipliers and (5) linearity of the CCD filters. With proper operation of the CCD filters it is expected that CCD operation can be made sufficiently linear that errors due to nonlinearities are not important. Each of the first four limitations is discussed in this section in the context of digital FFT comparison.

CTE affects the resolution of the DFT and is discussed separately. Thermal noise, weighting coefficient accuracy and multiplier accuracy are best discussed on terms of rms error in the transform. These sources of error are evaluated and related to the number of bits required to achieve equivalent error in an FFT. Finally, a state-of-the-art custom 1²L FFT is discussed and compared with the CCD CZT.

CTE

The effect of imperfect CTE is somewhat different for the conventional CZT than for the sliding CZT. In this section the sliding transform will be discussed.

The CZT is of course a sampled-data system, and the DFT is only defined for integral values of k. It is useful, however, to treat k as a continuously varying envelope which determines the spectral value at each integral k. Assuming the input is a complex sinusoid at frequency f, then equation (3) gives

$$|F_k|^2 = \left| \sum_{n=0}^{N-1} w_n e^{-i2\pi n \left(k - \frac{Nf}{f_c} \right) / N} \right|^2 \quad (11)$$

We can treat F as a function of continuously varying k by writing

$$|F(k)|^2 = G \left(k - \frac{Nf}{f_c} \right) \quad (12)$$

where the envelope function G(k) is the transform of the window function

$$G(k) = \left| \sum_{n=0}^{N-1} w_n e^{-i2\pi nk / N} \right|^2 \quad (13)$$

The frequency resolution, sidelobe level etc. are all determined by G(k), and the effect of imperfect CTE is to broaden and shift the peak of G(k).

Equation (11) can be rewritten as

$$|F_k|^2 = \left| \sum_{n=0}^{N-1} e^{-i\pi(n+k-N)f/f_c} h_n \right|^2 \quad (14)$$

where h_n is the ideal impulse response of a windowed chirp filter

$$h_n = w_n e^{i\pi n^2 / N} \quad n=0, N-1 \quad (15)$$

Imperfect CTE modifies the weighting coefficients to h'_n and changes the envelope $G'(k)$ to

$$G'(k) = \left| \sum_{n=0}^{N-1} e^{-i\pi(n+k)f/f_c} h'_n \right|^2 \quad (16)$$

Physically G(k) represents the correlation of a chirp waveform in a windowed chirp filter and equation (16) shows how the correlation response degrades as the filter decorrelates due to imperfect CTE. The decorrelating effect can be crudely estimated by scaling the clock frequency down by a factor on the order of $1 - \epsilon$, where ϵ is the fractional loss per stage.¹¹ This has the effect of decreasing the df/dt of the chirp filters by a similar factor with the result that the correlation peak broadens due to mismatch and shifts by an amount $\Delta t \sim N\epsilon / f_c$. This approximate behavior is confirmed by the calculations of Figure 8 which show the response of the 500-point sliding CZT with Hamming windowing to an input sinusoid having frequency $f = 3.3 f_c / N$.

Conclusions regarding the effect of imperfect CTE on the sliding CZT are summarized below. (1) The resolution degradation is on the order of $N\epsilon$ times the ideal resolution f_c / N . For $N\epsilon \sim .1$, the degradation is negligible. (2) The degradation is the same for all frequencies whereas in the conventional CZT, the degradation is three times worse for the high frequencies than for the low frequencies. (3) The degradation can be eliminated by modifying the filter coefficients to compensate for imperfect CTE or by modifying the premultiply chirp.

ERROR ANALYSIS

The accuracy which can be achieved using the CCD CZT is perhaps the most important performance criterion. In this section, the error sources are identified and evaluated in terms of bits in an equivalent digital FFT.

FFT Accuracy. Finite word length effects in a digital FFT fall into three categories.^{8,19,20} (1) Quantization of the data at the input A/D converter. (It is assumed that no external gain control is used with either the FFT or the CCD CZT). (2) Errors due to the finite word lengths used to represent the twiddle factors.¹⁹ (3) Truncation and roundoff effects generated within the butterflies.²⁰ In treating truncation effects a block floating point truncation algorithm is assumed in which all words are shifted right each time overflow occurs in any butterfly.

If the A/D converter has an accuracy of b_1 bits plus a sign bit, the quantization step size is 2^{-b_1} normalized to unity, and an rms error can be defined by

$$\Delta_Q = \left[\frac{1}{N} \sum_{n=0}^{N-1} \left(f_n - f_n^Q \right)^2 \right]^{\frac{1}{2}} \quad (17)$$

$$= 2^{-b_1} / \sqrt{12} \quad (18)$$

This noise does not scale with signal size. It represents a noise level below which signals cannot be processed. It dominates at low signal levels but other errors which scale with signal size dominate FFT error at large signal size.

If the twiddle factors are quantized to b_2 bits plus sign, the resulting rms error is given by¹⁹

$$\Delta_T = \frac{\log_2 N}{6} 2^{-b_2} \sigma_F \quad (19)$$

where σ_F is the rms level of the output signal and is related to the rms input signal σ_f through $\sigma_F = \sqrt{N} \sigma_f$.

The most important source of error in a digital FFT is usually overflow and round-off of data words during butterfly computation. If the data words are carried with b_3 bits plus sign, an upper bound on error in

a block floating point machine can be determined assuming overflow occurs at every stage. The result is²⁰

$$\Delta_B = .3 \sqrt{8} N^{\frac{1}{2}} 2^{-b_3} \quad (20)$$

If the twiddle factors are quantized to the same accuracy as the data words ($b_2 = b_3$) Δ_B dominates FFT error. Although equation (20) does not contain the input signal size explicitly, Δ_B does scale in a general way with signal because for smaller signals, overflow does not occur at every stage. The dependence of Δ_B on the length of the transform indicates that higher accuracy (large b_3) is required for longer transforms.

CCD CZT Accuracy. The sources of error in a CCD CZT are (1) thermal noise, (2) quantization of the pre and post multiply chirp waveforms, (3) weighting coefficient error in the CCD transversal filters, and (4) CTE. When the criterion of rms error to rms signal is applied, imperfect CTE generates large errors, because the errors add coherently. Because of this fact, however, CTE effects can be treated as a resolution degradation as discussed above and not as "random" error.

Thermal noise is analogous to input quantization in a digital FFT because it generates an error which is independent of signal size. Thermal noise in the CCD CZT is dominated by noise in the output amplifier of the filter.⁵ Assuming the rms noise referred to the input is 60 dB below the maximum peak signal, the equivalent quantization accuracy is $b_1 = 8$ bits plus sign. If 80 dB can be achieved⁵ this will correspond to $b_1 = 11\frac{1}{2}$ bits plus sign. At higher signal levels thermal noise, like input quantization noise in a digital FFT, is dominated by signal dependent errors.

In implementing the CCD CZT, the pre and post multiply chirp waveforms can be stored digitally in a ROM and multiplication can be performed in multiplying D/A converters.²¹ If the waveforms are stored with an accuracy of b_4 bits plus sign, the errors are analogous to twiddle factor quantization in a digital FFT. The calculated rms output levels Δ_M for both the pre and post multipliers is

$$\Delta_M = \frac{2^{-b_4}}{\sqrt{12}} \sigma_F \quad (21)$$

In Figure 9 the rms error to rms signal (Δ_M/σ_F) is plotted as b_w . The solid line is calculated using equation (21). The points are obtained from computer simulation of a 32-point CCD CZT. The input data were normally distributed random numbers. However, similar results are obtained using sine waves.

Weighting coefficient error arises from a number of sources, but let us assume as a model, that the placement of the gap in the split electrodes is quantized in steps of δ during photomask fabrication. δ is typically 10 μ m and the channel width W is typically 5 mil giving $\delta/W = .002$ this is equivalent to quantizing the weighting coefficients to 8 bits plus sign and is again analogous to twiddle factor quantization. The error which results is given by

$$\Delta_W = \frac{1}{\sqrt{6}} \frac{\delta}{W} \sigma_F \quad (22)$$

A plot of this expression together with computer simulated results are given in Figure 10.

Comparison. The major source of FFT error increases like \sqrt{N} (equation 20) whereas the major sources of CCD CZT error are independent of transform length.

Figure 11 compares the digital FFT with the CCD CZT using as the criterion the ratio of rms error to rms signal for large signals. The results are plotted as a function of the transform length N . A word length of 13 bits plus sign was assumed for the data and twiddle factors and on this case Δ_B dominates FFT error. For the CCD CZT, the multiplying chirp waveforms are quantized to 7 bits plus sign and $\delta/W = .002$.

CUSTOM FFT

In evaluating the potential of the CCD CZT, it is important to compare it, not with currently existing digital implementations of the FFT, but with projected state-of-the-art implementations which are under development. A potential digital competitor for the analog CCD spectrum analyzer is a custom FFT, and a low-power LSI FFT system using all I^2L technology is presented here for comparison.

A few introductory statements concerning the state of I^2L and the design philosophy of the custom FFT presented here are appropriate. I^2L is a very low-power, high density technology currently in early stages of product development. Current devices are running at speeds up to 2 MHz, but it is expected that speeds will improve significantly as the technology matures. The hypothetical FFT design presented here is custom in the sense that the architecture is tailored to perform the algorithm relatively efficiently and has matched the memory and computation speeds. None of the chips have actually been built, but are believed to be within the state-of-the-art. Flexibility normally expected in an FFT is provided, and with additional firmware, other vector oriented algorithms could be implemented. Therefore, this design can be considered as a general purpose digital signal processing module.

Table 1 lists the specifications of a hypothetical FFT processor.

Table 1. FFT Specifications

Algorithm	Inplace
Cycle Clock	2 MHz
Butterfly Time	4 μ sec
Transform Speed*	$N/2 \log (N+1) \times$ Butterfly Time
Transform Lengths	$N=1,2,3,\dots,512$ complex points
Arithmetic	16 bit block floating point with rounding
Coefficient Word Length	8 bits
Data Word Length	16 bits

*Include unscrambling.

The processor is designed from three basic I^2L chips: a single control chip, a 4 bit arithmetic unit slice, and a 1024 \times 4 bit RAM slice. The control chip includes the coefficient memory, the FFT micropogram memory, and the control and address generation circuitry. The arithmetic slice is a complex arithmetic unit (CAU) tailored to perform a parallel FFT (radix-2) Butterfly operation. Although the processor can be configured in multiples of these 4 bit slices, a 16 bit configuration, sketched

in Figure 12, has been chosen as a prototype model. Itemized power estimate of this processor with a 500 nanosecond cycle time is 300 mW dominated by the memory.

The I²L hypothetical FFT processor described above has overwhelming advantages over the CCD CZT in (1) flexibility and (2) accuracy in a sense that additional slices can be added. However, when flexibility and high accuracy are not required the CCD CZT compares favorably in two important aspects. (1) Number of packages: The 512-point sliding CZT illustrated in Figure 5 can be implemented with 3 IC's; 2 CCD filter IC's and one ROM containing the premultiply chirp. The I²L digital processor requires 9 IC's (see Figure 12) and in addition, requires A/D conversion. Even when state-of-the-art custom digital hardware is postulated, the CCD CZT maintains a clear cut advantage in package count and hence cost. (2) Speed: The I²L FFT operating at its maximum clock rate (2 MHz) generates spectral points at a 50 kHz rate. In general digital FFT hardware is limited to this kind of speed, and increased speed through parallel processing can be achieved only by a proportional increase in hardware. The CCD CZT, on the other hand operates in real time at speeds up to 5 MHz.

CCD's have also been proposed to perform the digital functions required to implement the FFT,^{22,23} and it has been claimed that, compared to competing devices from other technologies, charge-coupled devices appear to enjoy a ten to one advantage in device density and greater than a ten to one advantage in speed-power product^{1,23} Detailed comparisons with competing technologies need to be made to substantiate this claim.

V. APPLICATIONS OF THE CCD CZT

For a given spectral analysis application to be considered as a candidate for CCD CZT implementation it must satisfy two criteria: (1) It must be of modest performance which lies within the CCD performance limitations and (2) It must be required in sufficiently high volume that low cost is a dominant design specification. These two criteria rule out a large class of applications. However, there have been identified, several applications of great military importance which do satisfy both of the above criteria. These will be discussed in this section.

VIDEO BANDWIDTH REDUCTION

Transform encoding of video images for the purpose of bandwidth reduction is a potentially important application of the CCD CZT. A hybrid transform system has been developed¹⁸ which performs a discrete cosine transform (DCT) in one dimension and differential pulse code modulation (DPCM) in the other dimension.

DFT and DCT on "typical" video images have resulted in variance compaction approaching that of optimum transforms,¹⁸ and both the DFT and DCT can be cost effectively implemented with the CCD CZT. The CCD CZT becomes particularly attractive in remote sensing applications such as RPV's where small size, light weight, and low power are essential in addition to low cost.

SPEECH PROCESSING

Spectral analysis is one of the most important functions in speech processing,²⁴ and speech processing requirements in terms of sample rate (10 kHz), delay time (40 ms) and dynamic range (40 dB) are well within the CCD capabilities outlined above.

The simplest speech processing systems decompose speech into its spectral components as in the early channel vocoder systems. Channel vocoders perform well only at high bit rates²⁵ and therefore do not achieve optimal bandwidth reduction, but they are useful in word recognition systems.

There exist several algorithms which do achieve adequate bandwidth reduction and of these, one, is particularly well suited to CCD implementation. It is called homomorphic deconvolution²⁶ and operates upon the principle of the deconvolution of speech into pitch and to vocal tract resonances. In Figure 13 a block diagram of such a system is shown.²⁴ Since only the magnitude of transform 1 is required, the postmultiply can be eliminated, and in addition, the postmultiply of the inverse transform 2 cancels the premultiply of transform 3. Therefore the only chirp multiplications remaining are the premultiples of transforms 1 and 2 which can be implemented at the input to the CCD.²⁷ After transform 2, the pitch of the voiced speech is detected and then windowed out so that only the smoothed speech spectrum remains at the output. This spectra can be used to extract

formant data and if this information is efficiently encoded data rates as low as 1000 bits/s are realizable.²⁴ Homomorphic deconvolution is costly to implement digitally in real time because of the three sequential transforms which are required. However, the CCD CZT holds the promise of truly low cost implementations of this type of processing.

DOPPLER PROCESSING IN MTI RADAR

MTI (moving target indicator) radar operates upon the principle of detecting moving targets of small cross section in the presence of stationary background having much larger cross section. The doppler shift of the radar return is determined, and from this, the target velocity parallel to the radar line of sight, can be determined.

Radar returns are quasi-periodic, and the sliding CZT can be used. Typical transform lengths are 10 to 100 and typical pulse repetition frequency (PRF) is 1 kHz to 100 kHz. A doppler processor may be required to process thousands of DFT's on parallel, (one for each range gate) so reducing the cost of the DFT has a large cost impact on the overall system.

A doppler processor IC has been developed^{28,29} which performs ten 17-point CCD CZT's of the type shown in Figure 5. The IC contains all the integrated amplifiers and squaring circuitry required to obtain the power density spectrum in each range bin. A doppler processor for thousands of range bins can be implemented by cascading 10-bin IC's at a projected cost of approximately one-third that of an all digital processor designed using state-of-the-art digital hardware.²⁸

OTHER APPLICATIONS

Other potential applications of the CCD CZT include processing for FLIR images, sonobuoy signal processing, and remote surveillance.

The CCD CZT is not expected to make the digital FFT obsolete in military systems. However, for those spectral analysis applications which fulfill the twin requirements of modest performance and high volume, tremendous cost advantages can be gained using the CCD CZT. More applications will certainly emerge, but in the meantime,

the potential cost impact in the application areas already identified guarantees the importance of the CCD CZT in military electronic signal processing systems of the future.

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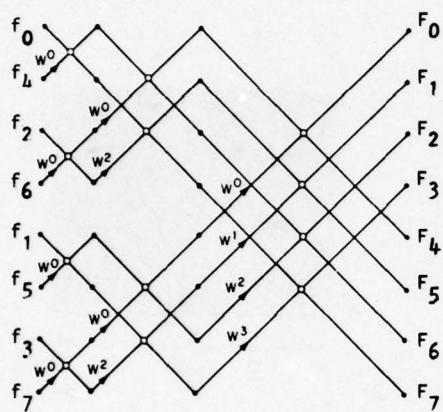
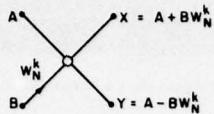


Fig. 1 a) Schematic of the butterfly. (see Eq. (2)) b) Schematic of an 8-point, radix 2, decimation in time FFT (Ref. 8)

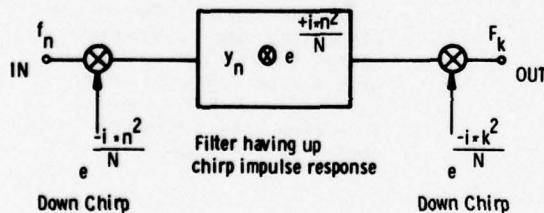


Fig. 2 Schematic of the CZT algorithm.

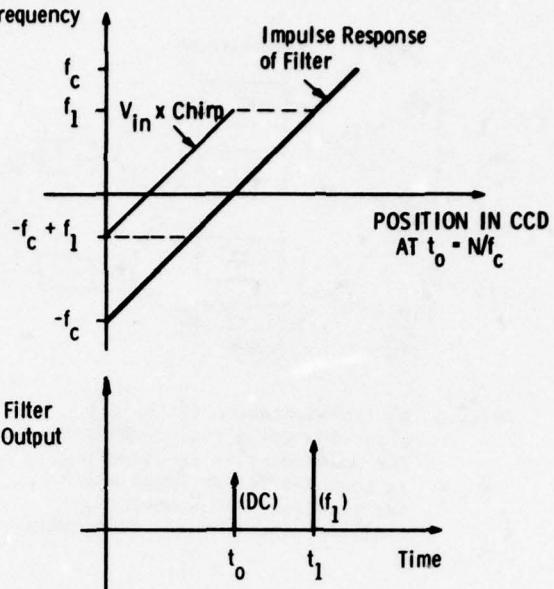


Fig. 3 Interpretation of the CZT in terms of chirp input waveforms in chirp filters.

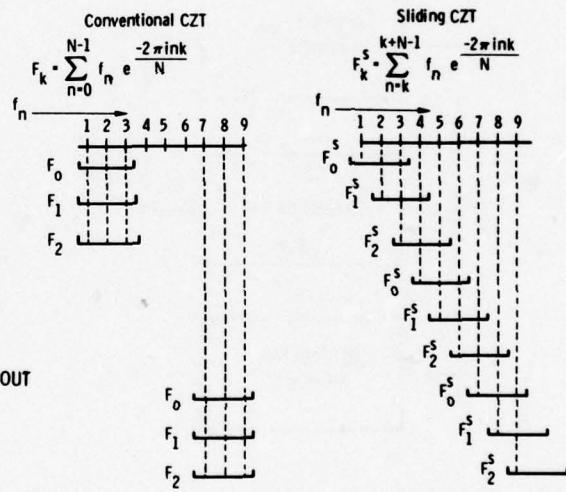


Fig. 4 Comparison between the conventional CZT and the sliding CZT for the case of a 3-point transform.

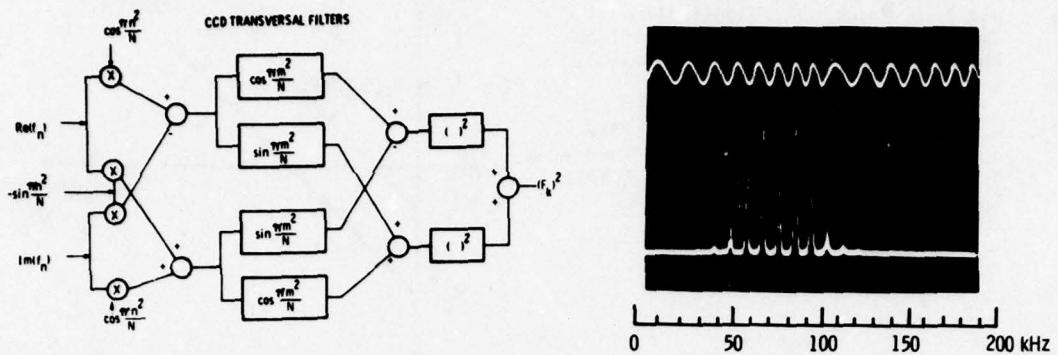


Fig. 5 An implementation of the CZT algorithm using real components. The power density spectrum $|F_k|^2$ is computed for an input which has both real (in-phase) and imaginary (quadrature) components.

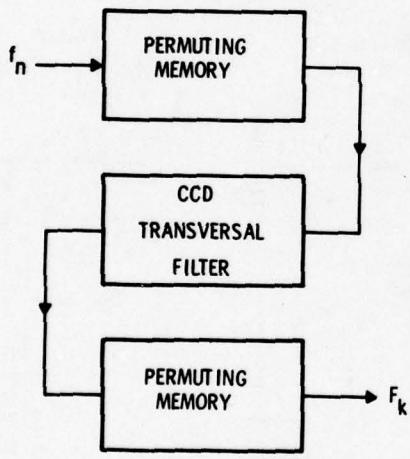


Fig. 7 Block diagram of the prime transform implemented with CCDs.

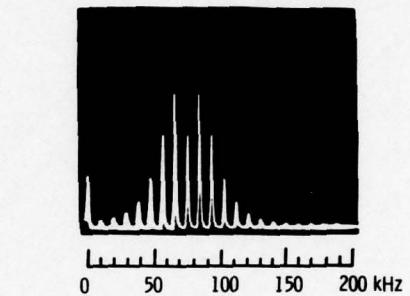
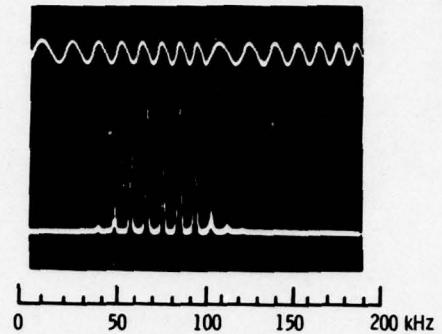


Fig. 6 A comparison of the 500-point sliding CZT power density spectrum (upper photograph) with the output of a conventional spectrum analyzer (lower photograph which shows the square root of the power density spectrum).

The input signal shown at the top of the upper photograph chirps from 50 kHz to 100 kHz with a repetition period of $T_d = 110 \mu\text{sec}$. This results in a line spectrum having period $T_d^{-1} = 9 \text{ kHz}$.

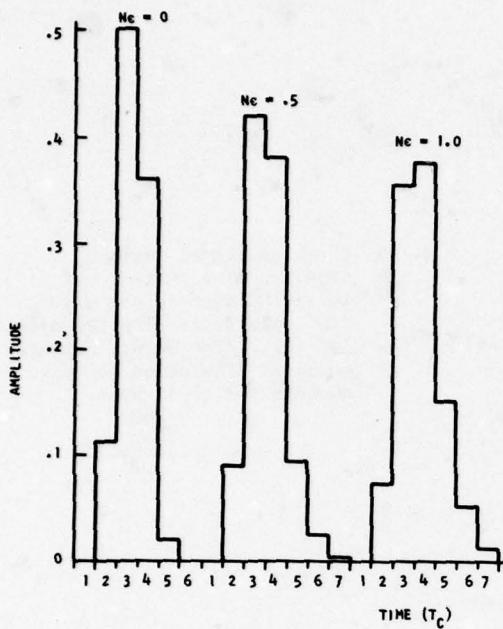


Fig. 8 The calculated response of the 500-point sliding CZT with Hamming weighting to a complex input sinusoid of frequency $f_{in} = 2.3 f_c$. The response is calculated for different values of CTE.

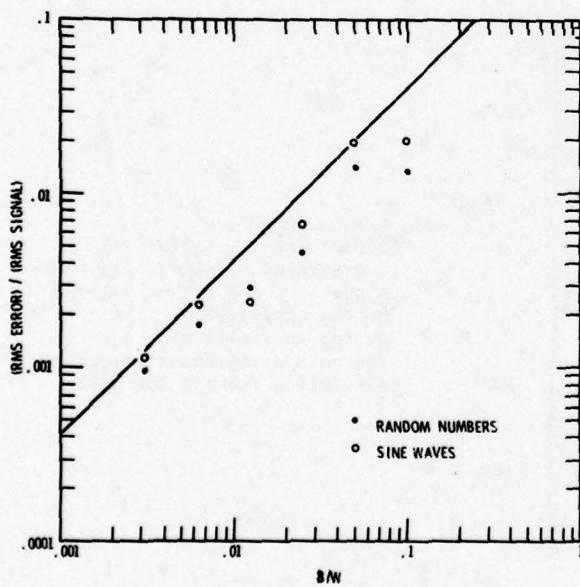


Fig. 9 Error to signal ratio Δ_M computed as a function of the number of bits b_4 used to quantize the premultiply and postmultiply chirp waveforms. The line represents Eq. (21). The points represent computer simulation in which just the premultiply or postmultiply is quantized.

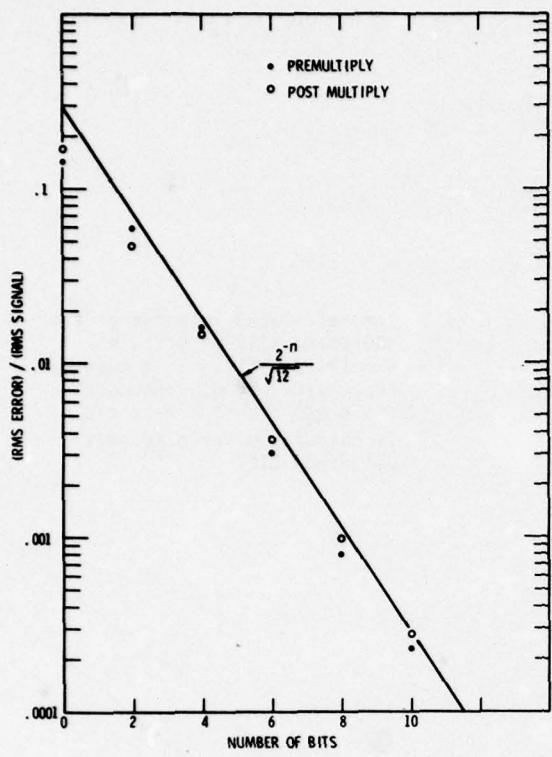


Fig. 10 Error to signal ratio Δ_W computed as a function of weighting coefficient error δ/W . The solid line represents Eq. (22). The points represent computer simulation for random numbers and sine waves.

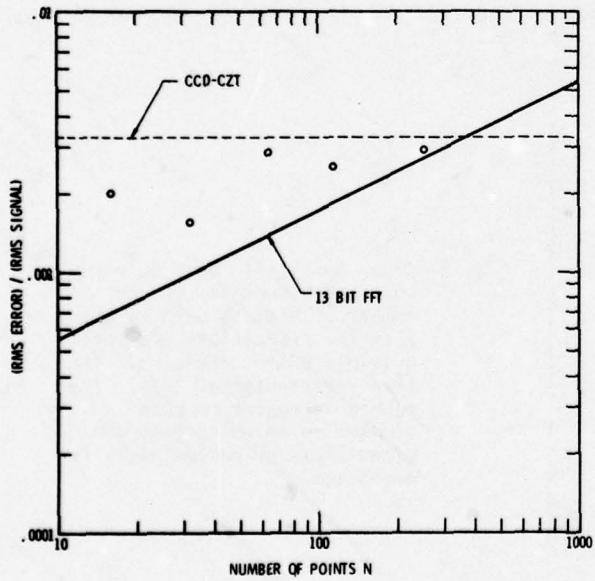


Fig. 11 Error comparison between a CCD CZT and a digital FFT implemented using 13 bits plus sign. The CCD CZT is limited by the quantization of multiply chirps to 7 bits plus sign. The points represent computer simulation for the CCD CZT.

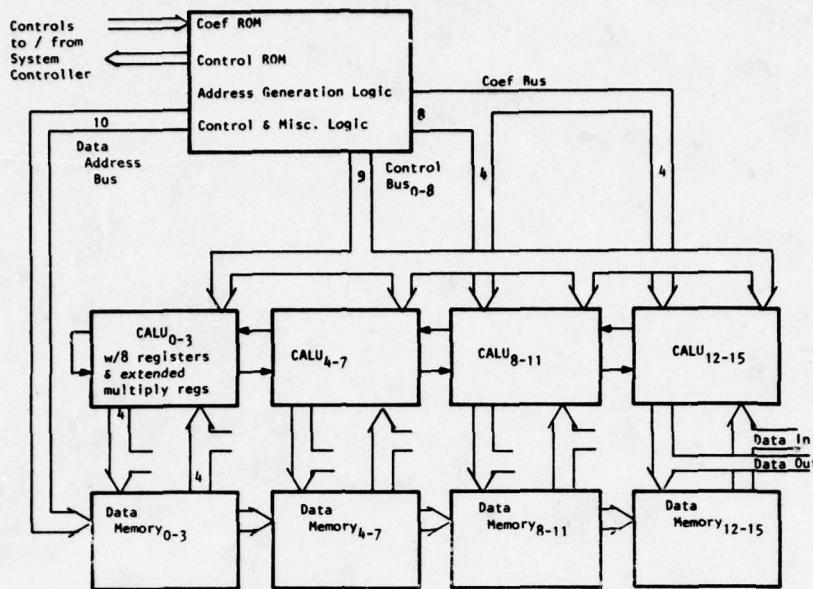


Fig. 12 A custom 16 bit 12L FFT requiring
9 IC's.

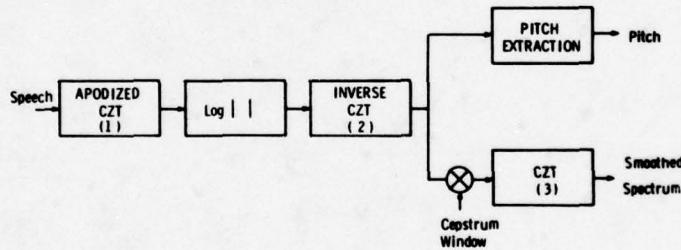


Fig. 13 Block diagram of a system to
perform homomorphic deconvolu-
tion of speech for bandwidth
reduction (Ref. 24). This is
one type of speech processing
which is particularly amenable
to implementation with CCDs.

RADAR VIDEO PROCESSING USING THE CCD CHIRP Z TRANSFORM

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ABSTRACT. Radar applications for CCD's appeared hopeless due to high data rate requirements until the realization that CCD's were applicable to pulse train processing instead of monopulse processing (e.g., SWD's). As a result, CCD's have found considerable applications in radar video signal processing. CCD implementation of the Chirp Z Transform is a powerful spectral analysis technique applicable to radar Doppler Processing. Successful integration of a small CCD Chirp Z Transform and associated peripheral electronics makes a small size, low power, and low cost Doppler processor for large multirange bin radar systems very attractive. The development of a 10 range bin, 17 point Doppler processor chip demonstrates the feasibility of such a processor.

INTRODUCTION

During recent years, basic radar transmitter, receiver, and antenna design has become relatively mature. Meanwhile, larger numbers of potential targets, higher resolution, and more stringent detection requirements are plaguing radar designers. As a result, more emphasis is being placed in signal processing development in recent years. The development of surface wave device pulse compression filters is a prime example. The use of digital Doppler processors based upon the FFT algorithm has similarly been a significant development within the past decade. The powerful computational equivalency of CCD transversal filters¹ in performing convolution operations as well as their small size and low power make the development of a CCD Doppler processor exciting from the aspects of size, weight, and power requirements.

The problem of detecting a target in the presence of Gaussian noise is well understood. However, the discrimination of multiple tar-

gets is less straightforward. The most common problem is the detection of a target in the presence of clutter, the radar return from land, water, trees, man-made structures, etc. In many cases, clutter returns may contain more power than desired target returns from the same range bin requiring target discrimination on the basis of a characteristic other than amplitude. This operational environment is indicated in Figure 1.

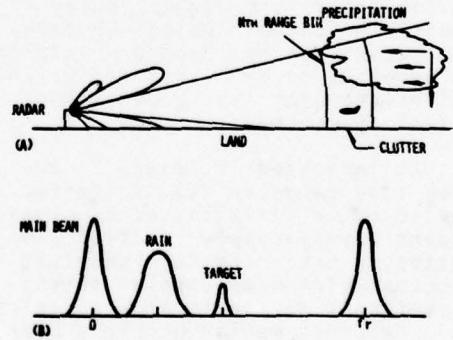


Figure 1. Relationship between
(A) Radar Operating Environment
and (B) Spectral Characteristics

VIDEO SPECTRAL ANALYSIS TECHNIQUES

The most common criterion for discrimination of multiple targets within a range bin is the use of Doppler frequency discrimination techniques. Since many clutter targets are stationary (or nearly so), the most common approach to clutter rejection is the delay line canceler moving target indicator (MTI) which in its simplest configuration delays a radar video return for a PRI and differences the delayed return from the succeeding new return. Since the returns from stationary targets occur at the same location in the data stream each PRI, such returns should be canceled. When considering the delay line canceler operation in the frequency domain, it may be observed to have a spectral response as indicated in Figure 2. This response has nulls near zero frequency and the PRF which attenuate the clutter returns and the aliased clutter returns.

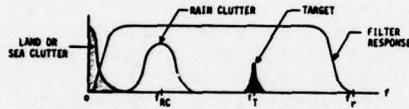


Figure 2. Canceler MTI Response

Internal clutter motion, high clutter rejection requirements, and system instabilities cause delay line cancelers to be more sophisticated than indicated above. Such cancelers have typically been implemented using A/D converters and digital delay lines. The use of analog CCD delay line cancelers² has been demonstrated and promises to be a less costly and smaller approach than conventional digital approaches.

As indicated in Figure 2, the delay line canceler MTI is ineffective in the discrimination of clutter returns having Doppler shifts. Rain clutter or chaff are two important examples which have Doppler shifts proportional to the local wind velocity. Internal motion within a rain cell will generally cause a spread in the spectral characteristics of the return as indicated in Figure 2. In

order to discriminate against Doppler shifted clutter returns or against multiple targets within a range bin, more sophisticated spectral analysis is required.

The use of range sorting techniques followed by contiguous band-pass filter banks in each range bin is an obvious approach to frequency discrimination of targets within a range bin. This approach is generally impractical for large radars since the filter bank must be duplicated for each range bin.

Another crude frequency analysis technique is the single sideband modulation of an incoming signal with a repetitive linear FM (chirp) waveform which is then passed through a band-pass filter. The relative time of occurrence of the filter's output can be used as a measure of the incoming signal's frequency. This technique is conceptually similar to the Chirp Z Transform which can be shown to give the true power spectral density of the incoming signal.

Digital implementations of discrete (DFT) or fast (FFT) Fourier transforms have permitted the achievement of the necessary frequency resolution to inhibit the processing of Doppler shifted clutter targets. In addition to improving subclutter visibility, DFT processing provides coherent integration over N samples which ideally increases the signal-to-noise ratio by a factor of N for a signal in the presence of white noise.

While the use of DFT or FFT techniques to implement a pulse Doppler processor are well understood, such a processor is quite complex for practical multirange bin radars contributing to a significant fraction of the total cost of the system.

THE CCD CHIRP Z TRANSFORM

The powerful computational equivalency of CCD transversal filters in the solution of matrix equations, and particularly, the performance of convolution operations, has led to the observation that such a filter can provide an operational breakthrough

in performing high speed (up to 10 MHz) DFT's through use of the Chirp Z Transform (CZT). The CZT has been known for some time,^{3,4} but has generally been considered a mathematical curiosity since on the order of $N \log_2 N$ computations are required, and thus, offers no simplification over a conventional FFT using digital implementations.

By starting with the classical DFT equation,

$$F_k = \sum_{n=0}^{N-1} f_n e^{-\frac{i2\pi nk}{N}} \quad (1)$$

it may be shown that the DFT may be easily implemented using CCD transversal filters to perform the bulk of the required computation.^{5,6} By substituting

$$-2nk = (n - k)^2 - n^2 - k^2 \quad (2)$$

into Equation 1, the expression for the CZT is derived:

$$F_k = e^{-\frac{i\pi k^2}{N}} \sum_{n=0}^{N-1} \left(f_n e^{-\frac{-i\pi n^2}{N}} e^{\frac{i\pi(n-k)^2}{N}} \right) \quad (3)$$

This equation may be viewed as a series of operations performed with the complex linear FM, or chirp, waveform, $e^{-\frac{i\pi n^2}{N}}$. The calculation

of F_k may be accomplished by (1) multiplication of the sequence f_n by a chirp waveform, (2) convolution of the new waveform with the oppositely sensed chirp waveform, and (3) a final chirp multiplication which gives the correct phase. When only the power density spectrum $|F_k|$ is desired, the final chirp multiplication may be replaced by a sum-of-the squares operation.

In order to calculate the complete spectrum (i.e., F_k for $0 < k < N-1$) in general requires $2N-1$ calculations of the summation indicated in Equation 3 due to the filter loading time. The calculation of all N Fourier coefficients requires convolution of

the input sequence $f_n e^{\frac{-i\pi n^2}{N}}$ with N values of a chirp waveform which has a total of $2N-1$ values implying that the input data f_n must be blanked such that

$$f_n^* = \begin{cases} f_n & 0 \leq n \leq N-1 \\ 0 & N \leq n \leq 2N-1 \end{cases} \quad (4)$$

in order that the undesired filter weighting coefficients do not contribute when calculating the appropriate Fourier coefficients.

Equation 3 can be more directly implemented using CCD's by substituting

$$n = k - m + N \quad (5)$$

where m denotes the m^{th} CCD stage.

The Fourier coefficient is then

$$F_k = e^{-\frac{i\pi n^2}{N}} \sum_{m=1}^{2N-1} e^{\frac{i\pi(m-N)^2}{N}} \left[f_{k-m+N}^* e^{-\frac{-i\pi(k-m+N)^2}{N}} \right] \quad (6)$$

which implies convolution in a complex CCD correlator of length $2N-1$. Due to the blanked nature of the input data, the chirp multiplication indicated in the bracketed term is only necessary over the range of n over which f_n was nonzero so that the input sequence f_n is required to be multiplied by

$$c_n = e^{-\frac{i\pi n^2}{N}} \quad 0 \leq n \leq N-1 \quad (7)$$

The CCD transversal filter tap weights are defined as

$$h_m = e^{\frac{i\pi(m-N)^2}{N}} \quad 1 \leq m \leq 2N-1 \quad (8)$$

The blanking of the input sequence f_n can be a problem when a continuous spectrum of a continuous signal is desired. This can be accomplished by two CZT's which have stag-

gered timing. However, the use of the continuous, or sliding, CZT² can be used to advantage in many such applications. Figure 3 indicates the primary differences between the exact CZT and the continuous CZT for a five point transform. The exact CZT utilizes input samples $x_0 - x_4$ to obtain Fourier coefficients $X_0 - X_4$. Input samples $x_5 - x_9$ are required to be blanked and a new set of Fourier coefficients are calculated from $x_{10} - x_{14}$. The continuous CZT calculates the first Fourier coefficient X_0 on the input samples $x_0 - x_4$, the second coefficient X_1 on input samples $x_1 - x_5$, etc. The continuous CZT is equivalent to the exact DFT in the calculation of power spectra for spectra unchanging over the time $2NT_c$ where N is the transform length and T_c is the sampling period. The continuous CZT calculates the same phase as the exact DFT for input signals periodic in N.

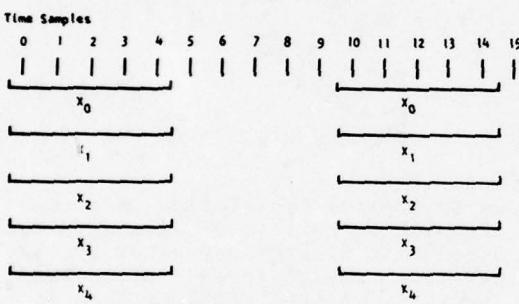


Figure 1(b) displays four time series plots, each consisting of 15 data points. The horizontal axis represents time samples from 0 to 14.

- Series x_0 :** Values are 0 at samples 0-4, 1 at sample 5, 0 at sample 6, and 1 at samples 7-14.
- Series x_1 :** Values are 1 at samples 0-4, 0 at sample 5, 1 at sample 6, and 0 at samples 7-14.
- Series x_2 :** Values are 0 at samples 0-4, 1 at sample 5, 0 at sample 6, and 1 at samples 7-14.
- Series x_3 :** Values are 0 at samples 0-4, 1 at sample 5, 0 at sample 6, and 1 at samples 7-14.

Figure 3. Comparison of the Exact CZT with the Continuous CZT

The continuous transform can be defined by the equation

$$F_k^C = \sum_{n=k}^{k+N-1} f_n e^{-i2\pi nk/N} \quad (9)$$

In this case, an N point correlator is capable of generating N Fourier coefficients. By making a substitution similar to Equation 5 and a shift of the summation index, this expression can be reduced to an expression similar to Equation 6 in which chirp through zero frequency waveforms may be used. This is especially convenient for using CCD filters since it permits minimization of the Nyquist sampling rate. The input chirp waveform samples for this continuous chirp through zero case are defined by

$$c_n = e^{-i\pi(n-N/2)^2/N} \quad 1 < n < N \quad (10)$$

which implies Nyquist sampling at the frequency extremities.

Sidelobe reduction is a key factor in the achievement of high clutter visibility. Apodization for reduction of sidelobes may be utilized on filter weighting coefficients for the continuous CZT, but must be accomplished on either the input chirp or signal waveforms for the exact CZT. Most apodization techniques are approximations to Dolph-Chebyshev weighting and are well documented.⁷ Attendant with sidelobe reduction are correlation pulse width broadening which sacrifices frequency resolution and a decrease in processing gain. Sidelobe levels for CCD filters are ultimately limited by tap weight round-off inaccuracies, but computer simulation indicates sidelobe levels below 40 dB are achievable. Aliasing considerations are extremely important in the realization of low sidelobe levels when using the continuous CZT. Of particular importance is the generation of C_n such that

$$c_{n+N} = c_n \quad (11)$$

in order that the phase of the product $f_n C_n$ is continuous through the folding frequency.

CCD CZT DOPPLER PROCESSOR IMPLEMENTATION

Figure 4 shows the conceptual implementation of a range-gated CZT Doppler Processor. Functionally, this processor is analogous to the FFT processor. The I and Q video signals for all range bins of given pulse return are multiplied by the properly weighted sample of the down-chirp signal as required in the first step of the CZT algorithm. Range gating may be accomplished by commutation or demultiplexing operations. Commutation is accomplished by sequentially switching the appropriate correlator into an analog data bus. Demultiplexing may be accomplished by storing video samples corresponding to M range bins in a serial in - parallel out CCD each PRI. At the completion of the PRI, the samples are simultaneously transferred out into M chirp correlators. It is seen that these chirped time samples propagate through the chirp filters at a rate of one position per PRI. Thus, one spectral sample is produced every PRI from the output of each chirp filter. That is, for a given range bin, the spectral samples emerge in sequence with N PRI's required to obtain an N-point spectrum of the input time series.

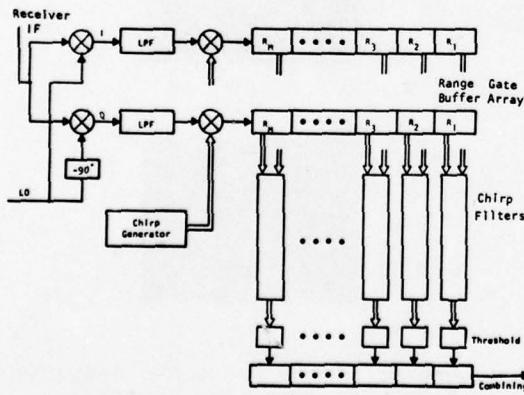


Figure 4. Range Gated Pulse Doppler Processor Utilizing the CZT

In general, all quantities in the previous CZT equations are complex. To perform complex processing in real hardware, parallel channels are implemented for the real and the imaginary components of each term. [The complex data sample f_n has already been separated into real and imaginary components by virtue of the I and Q radar video processing.] Figure 5 shows in more detail the implementation of the CZT by examining the processing for the K th range bin. The range gate buffer array supplies sine and cosine components of the chirped time series at the sample rate (i.e., the PRF). Each of these components is then processed in sine and cosine filters. For example, the cosine components of the chirped series when applied to the cosine filter is performing the correlation operation:

$$\sum_{n=0}^{N-1} g(n)h(k-n), \quad (12)$$

where

$$g(n) = x_n \cos\left(\frac{\pi n^2}{N}\right), \\ h(k-n) = \cos\left[\frac{\pi(k-n)^2}{N}\right], \quad (13)$$

which is a component of the required correlation. This component is combined with the three other outputs as shown in the figure.

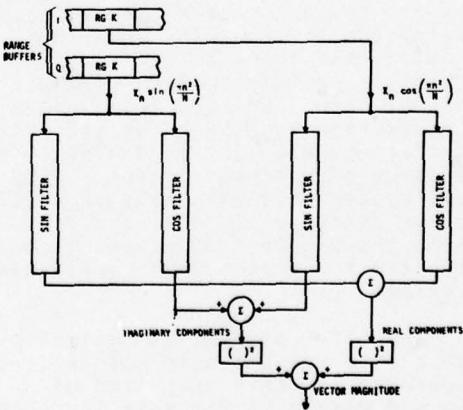


Figure 5. Filter for a Single Range Bin

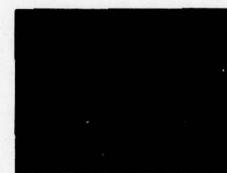
In pulse Doppler radar processing, the power spectrum, rather than the complex Fourier transform, is usually the quantity of interest. Thus, the third step of the algorithm (multiplication by the second chirp) may be omitted. The I and Q channel components are finally combined in a vector magnitude algorithm. Output processing consists of thresholding, which may be adaptive or fixed (on an individual Doppler bin basis to reject clutter and detect moving targets), and Doppler bin combining.

Since the number of range bins required for most radar systems varies between 50 and several thousand, a Doppler processor chip approach that can readily be expanded to accommodate any required number of range bins is desirable. This approach can best be effected by commutating the video return into a desired number of identical chips. These chips can be structured to perform the block diagram functions of Figure 4. The video return on the chip must first be sorted into appropriate range bins by a demultiplexing or commutating operation. This range-sorted video return must then be applied to in-phase (I) and quadrature (Q) matched filters whose outputs are squared and summed to eliminate an output amplitude - input phase dependence. Of significant importance in the successful integration of these functions is the ability to derive the output signal from the CCD matched filters, to perform a reasonable approximation to an analog squaring function, and to do an analog signal summation a multiplicity of times on a single chip. If such functions are not integrated on the chip, the package size quickly becomes dominated by the large pinout requirement. The small system size advantage of a CCD Doppler processor is not as obvious due to the requirement of additional circuitry to perform these processing functions.

The first attempt at designing such a chip was a single channel, four-range bin chip comprised of a sine and cosine filter pair for each range bin. A single on-chip differ-

ential current integrator (DCI) complete with dual MOS integrating capacitors was placed on this bar. Two filter chips (I and Q channels) as well as sixteen DCI chips were combined to construct a four range bin version of the system shown in Figures 4 and 5. Bipolar operational amps and analog multipliers were utilized to accomplish the majority of the remaining functions. The breadboard was operated assuming a PRF of 1 kHz and a transmitted pulse width of 10 μ s.

A very elaborate SSB generation scheme was utilized to simulate I and Q baseband radar video signals over the frequency range from 30 Hz to 800 Hz which was determined by the sideband filter characteristics. The breadboard was capable of performing spectral analysis over the frequency range from 0 to 1 kHz with resolution of 58.8 Hz. Figure 6 indicates the response of the breadboard to sinusoids of 100 and 500 Hz. Figure 7 indicates the simultaneous response of the four range bins to a continuous sinusoid. Sampling the I and Q sinusoids during the appropriate range bin window permits the simultaneous response of Figure 8 to be achieved.



(a)



(b)

Figure 6. Single Range Bin Response of Doppler Processor Breadboard to (a) 100 Hz Sinusoid and (b) 500 Hz Sinusoid



Figure 7. Simultaneous Response of Four Range Bins to a Continuous Sinusoidal Input Signal

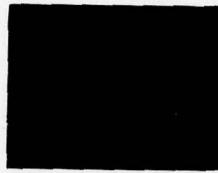


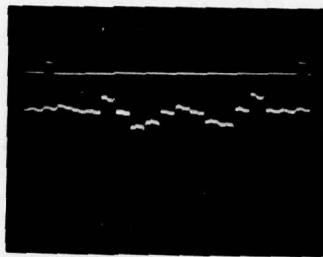
Figure 8. Simultaneous Response of Four Range Bins to a Sampled Sinusoidal Input Signal

A second bar has been fabricated in an attempt to develop a modular Doppler processor chip which may be cascaded to achieve any desired number of range bins of processing. This chip contains complete I and Q processing of 17 point CZT's for 10 range bins. This bar has the dimensions of 275 mils by 280 mils and contain the following:

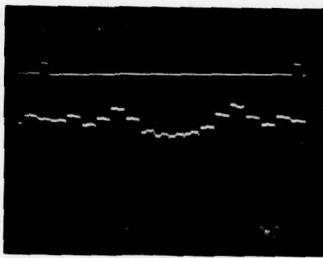
- 2 - Range Commutating Shift Registers
- 40 - 17 Point Chirp Filters
- 20 - Differential Current Integrators
- 20 - Sample and Hold Circuits
- 20 - Differential Amplifiers
- 20 - Transconductance Multipliers

This bar is perhaps the most ambitious attempt made to date in the integration of peripheral CCD electronic circuitry. Chip operation has been achieved as indicated in Figure

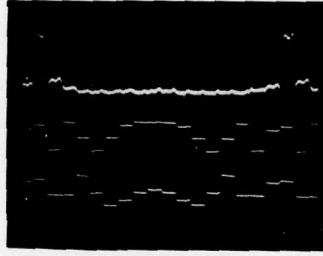
9 which shows the impulse response of two of the filters as well as an overall correlation response.



(a)



(b)



(c)

Figure 9. Impulse Responses for

$$(a) -\sin \frac{\pi(n - \frac{N}{2})^2}{N} \quad \text{and}$$

$$(b) -\cos \frac{\pi(n - \frac{N}{2})^2}{N} \quad \text{filters and}$$

(c) Correlation Response for 10 Range Bin, 17 Point Doppler Processor Chip

CONCLUSION

The development of the 10 range bin Doppler processor bar has demonstrated the feasibility of integrating short CCD transversal filters and the required peripheral electronics on the CCD chip to accomplish sophisticated functions such as multirange bin Doppler processing. Such integration is the key to an economical Doppler processor chip which can serve as a building block for large multirange bin systems. Improvements in circuit performance and minimization of chip size (or extension to longer transforms) are expected with improvements in peripheral circuitry technology.

ACKNOWLEDGMENT

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LINEARISATION OF THE CHARGE COUPLED DEVICE TRANSFER FUNCTION

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ABSTRACT

The adoption of charge-coupled devices in analogue signal processing applications is dependent on several performance parameters being achieved such as:

- (a) Low charge transfer inefficiency,
- (b) High sampling rate,
- (c) High signal to noise ratio, and
- (d) Low harmonic distortion.

The first three parameters have been studied in some detail and are at the stage where most applications can be satisfied. Parameter (d) however, is not easily achieved, and currently only one technique has been developed which yields overall ccd distortion lower than 40 dB without seriously degrading dynamic range. The limitations of this technique are outlined and a potentially powerful technique for obtaining low harmonic distortion coupled with optimum dynamic range is discussed in detail. The technique utilises a sensing structure positioned adjacent to the ccd input gate in order to sense the quantity of charge being injected into the ccd; the signal from this circuit being used as feedback to control the quantity of charge entering the ccd. Assuming low loss transfer, this technique may be utilised to obtain a highly linear transfer function from many of the ccd devices likely to be used in signal processing applications.

INTRODUCTION

The operational parameters of charge-coupled devices in signal processing applications can be clearly specified for many applications. High transfer efficiency, bandwidth and signal to noise ratios can be achieved, and in some cases these are obtainable with low harmonic distortion. In many situations however, low distortion and high dynamic range are difficult to achieve simultaneously unless some method is used to linearise the charge injection and detection. It is thus extremely important to produce ccd's for signal processing applications, which have a low harmonic distortion, independent of dynamic range.

Many different schemes exist for injecting charge into ccd's. Their basis is to inject a quantity of charge which is proportional to the input signal voltage level. The most commonly used linearisation technique, potential equilibration^{1,2}, involves injecting a quantity of charge in such a manner as to produce a linear relationship between the surface potential under the collecting well and the surface potential under an input gate. The technique relies on the assumptions that:

- (a) No distortion is introduced during transfer
- (b) A detection circuit is available which can transform surface potential linearly to an output signal.

The latter assumption proves to be an important limitation in the fabrication of delay lines and programmable matched filters when a floating-gate sensing technique is utilised. This limitation has led to the development of a technique which overcomes the problems of sensing and input circuit non-linearities and thus provides a linear ccd transfer function.

FEEDBACK LINEARISATION

The principles of operation of the linearisation technique are demonstrated in Figure 1. The input signal is applied to a differential amplifier, the output of which is connected to a diode diffusion at the ccd input. Adjacent to this diffusion is a gate, the potential of which is pulsed high after the commencement of the second-phase pulse and is returned to a low potential prior to the termination of the succeeding third-phase pulse. During the period when this gate potential is high, minority carriers flow from the input diffusion to the potential well below the first tap

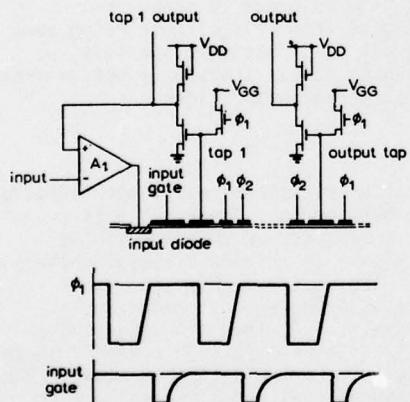


Fig.1. Circuit and timing diagram for feedback linearisation technique

electrode. The quantity of charge residing in this well is sensed using a floating-gate reset technique and the output of the sense amplifier is used as feedback to the differential amplifier. As a result of the feedback, the charge injected into the ccd is controlled in such a manner as to give an output voltage from the sense amplifier which follows the input voltage according to the equation:

$$V_{\text{out}} = V_{\text{in}} / (1 + 1/(A_1 \times A_2)),$$

where A_1 is the gain of the differential amplifier stage and A_2 is the variable loss between the input diode and the sense amplifier output. From this equation, when $A_1 \times A_2$ is much greater than unity, the transfer function of the device is linear. For reasonable amplifier gains, this inequality is valid over virtually the entire signal charge range; A_2 only tending to zero for zero charge and as saturation of the tap potential well is reached.

The technique was implemented using a single-level metal ccd fabricated on $10 \Omega \text{ cm}$, $<100>$ orientation n-type silicon. The tap electrodes and the transfer electrodes were 8 and 4 μm long respectively with 2 μm gaps. The gain of the differential amplifier was 100 giving an overall open loop gain ($A_1 \times A_2$) of approximately 25.

Figure 2 demonstrates the open loop response of the device to a triangular waveform and Figure 3, the response with feedback applied. The improvement in linearity can clearly be seen, even for the relatively low open loop gain used. The only curvature visible on the corrected waveform occurs just prior to saturation being reached as predicted above.

A spectral analysis of the output of the first tap sense amplifier was performed. A low frequency sinusoidal signal was applied to give a 95% of maximum output voltage swing and the following results were obtained:

Fundamental	0 dB
2nd harmonic	< -40 dB
3rd harmonic	< -50 dB
4th harmonic	-50 dB
5th harmonic	< -50 dB

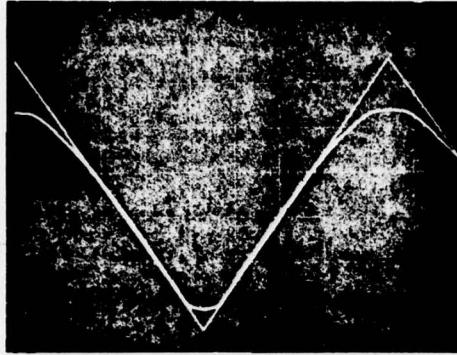


Fig.2. Input and output waveforms without linearisation

Input: 10 mV/division
Output: approximately 200 mV/division
Horizontal: 5 ms/division

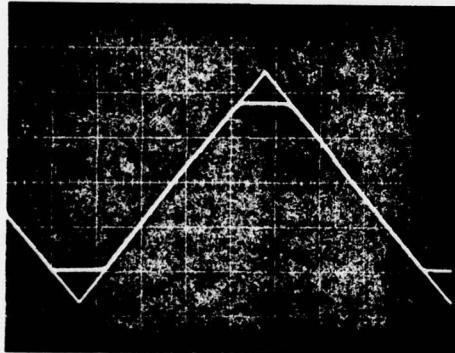


Fig.3. Input and output waveforms with linearisation

Input: 200 mV/division
Output: approximately 200 mV/division
Horizontal: 5 ms/division

A measurement of charge residual after 127 transfers gave a residual inefficiency of less than 3×10^{-4} per transfer and the signal to noise ratio at both input and output taps was much greater than 50 dB. The signal was, however, subjected to a 20% of maximum reduction in charge magnitude at the ccd output tap due to recombination at the low resting potential

used. This resulted in the output sensing circuitry being operated in a different part of its non-linear transfer curve from the input. Using the measurement technique outlined by Sequin and Mohsen², the 2nd and 3rd harmonics at the ccd output tap were less than -35 and -45 dB respectively, even for the highly unacceptable loss of signal experienced.

AMPLIFIER CONSIDERATIONS

The design of the differential amplifier used in the feedback loop is of fundamental importance to the stability and frequency performance of the technique. A wideband bipolar operational amplifier was used in the prototype system described above, but for frequencies up to several MHz there appears to be no fundamental reason why a MOS amplifier could not be used. In many of the signal processing applications utilising this type of linearisation, an operational amplifier could prove to be a useful device to have integrated with the ccd and for this reason a MOS operational amplifier is considered to be particularly desirable.

The open loop response of the circuit with the input gate in the on condition should, for stability, contain a dominant pole at frequency ω_c producing a 20 dB/decade roll-off until below unity gain, Figure 3. As the input gate is switched off, however, the series resistance associated with the channel directly below it increases in value, introducing a constantly reducing pole in the loop response. Hence, from the time that this pole reaches unity gain frequency ω_u until it is lower than ω_c^2/ω_u , the closed loop is potentially unstable. However, since the time taken for this to occur is much less than the loop delay, there appears to be no deleterious effect on the closed loop stability.

The equivalent input drift of a MOS operational amplifier could also prove to be a problem. However, since the amplifier is active for somewhat less than 50% of the time, it should be possible to incorporate a stabilisation circuit similar to that discussed by Fry⁴ and substantially reduce this effect.

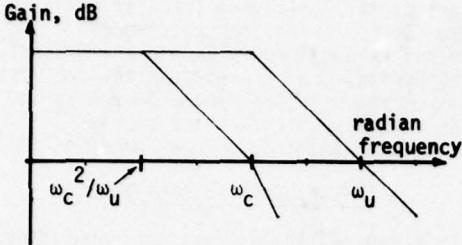


Fig.4. Change in open loop response during input gate switch off

CONCLUSIONS

In conclusion, a technique has been developed for electronically controlling the quantity of charge introduced into a ccd in such a manner as to produce an output signal from a non-linear sensing circuit, which is a near replica of the input signal. The advantages of the technique may be summarised as follows:

- (a) It produces a linear, ccd transfer function,
- (b) May be used with any non-linear, non-destructive sensing technique,
- (c) May be applied to buried channel and peristaltic ccd's,
- (d) Provides a designable, fixed gain transfer function,
- (e) Allows the designer to choose the degree of linearity desired by varying the open loop gain, and
- (f) May be used with multiplexed ccd's to overcome input threshold voltage variations.

The requirement for an operational amplifier at the ccd input may initially appear to be a major disadvantage. However, some form of buffer amplifier is likely to be necessary in virtually all applications. In recursive filters for example, such an amplifier is essential for the summation process, and if combined

with ccd's allows other signal processing functions such as multiplication to be performed. Hence, the amplifier should ideally be produced in a technology compatible with the ccd in order that a high level of integration, and thus low unit cost, may be achieved in signal processing devices.

ACKNOWLEDGMENTS

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A CCD-SAW PROCESSOR FOR PULSE DOPPLER RADAR SIGNALS

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ABSTRACT The use of different clock rates for data input and output in CCD analogue signal processors provides a convenient means of adjusting the duration and bandwidth of signals to suit subsequent operations. This feature can be usefully incorporated into a CCD analogue store for radar data which is also designed to re-order the data sequence for doppler-frequency analysis using surface acoustic wave chirp filters. The combination of msec storage times available with CCD and the precision high-speed processing of SAW devices, made compatible by the flexibility of CCD time scales, provides a powerful capability for high resolution multi-channel frequency analysis involving comparatively simple hardware which can accommodate a range of radar parameters.

INTRODUCTION

A coherent pulse radar signal contains much information which it is usually uneconomic to extract because of hardware size and complexity. In particular, it is advantageous to resolve the doppler frequencies of targets even when their velocities are not required because narrowband detection excludes much of the noise (or jamming) which tends to obscure the target. Full doppler processing of this kind requires a bank of many narrow (eg tens of Hz) band filters for each resolved range cell or some equivalent hardware, for example using digital Fourier transformation. Such processing is rarely implemented because of the complexity and cost of existing methods but it now appears that the advent of CCD and surface acoustic wave (SAW) signal processing methods may change this situation, allowing a processor to be built up to suit a given requirement (specified in terms of pulse repetition frequency (prf), number and size of range cells and number of pulses to be coherently processed) from fairly simple standard modules.

The basis for this is that the established capability of SAW spectrum analysers using 'chirp' filters (linearly dispersive delay lines) can be applied to radar doppler analysis by time-compressing the data using

a CCD. This expands the bandwidth and shortens the duration by a factor of order 1000 so that these parameters are brought within the scope of SAW processing. The CCD store can also be configured so as to separate the incoming data stream into sequences from different range cells, for individual spectral analysis. Because of the shortened time scale, data from many range bins can be analysed in a time equal to the accumulation period. The duration of the CCD output streams are matched to the fixed length of the SAW filters but the input rate is set by the radar pulse repetition rate (prf) and range cell spacing.

ARCHITECTURE OF THE PROCESSOR

The CCD data store required is a serial-to-parallel arrangement schematically shown in Fig 1. The input accepts a video signal as discrete analogue samples clocked into the upper (serial) CCD register during the strobed time interval following the transmission of a radar pulse and corresponding to the range interval of interest. For simplicity we will assume that 1 sample per range gate interval is used (2 would allow more protection against range straddling loss). After the serial acquisition of data from each radar pulse, the serial clock is stopped and the clock for the parallel registers taken through one cycle so that

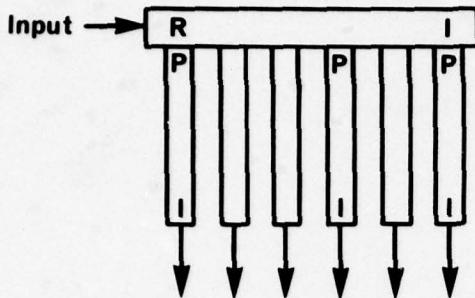


Fig 1 Storage Format

the latest samples enter the top of the parallel stacks. After a number of radar pulses, these each contain the history of the video amplitude corresponding to a particular range.

In the simplest mode of operation, a data matrix is filled containing RP samples from P radar pulses and R range cells, the input is inhibited or directed to another similar store, and the stacks are clocked in turn to output the data streams at high speed for

rapid spectral analysis. Frequently only a restricted proportion of the pulse repetition interval, T, is to be analysed so that some dead time is available between pulses during which the readout of one parallel register can occur. In this case the Doppler frequency processing for successive range cells is based on slightly offset time windows. For the particularly simple case of $R = P$ each range store is just filled as its turn for readout occurs. If $P > R$ then each new cycle of readouts has to await the refilling of the store while if $P < R$, more than one range readout is necessary between radar pulses to avoid losing data.

The output data is put through a sample-hold circuit to strip off the unwanted clock transients and presented to the spectrum analyser. Since only the power spectrum is required, this takes a simple form built around two 'chirp' or linear FM filters. The first is impulsive to generate a chirp signal at a convenient IF which is mixed with the signal to form the input for the second chirp filter.

The second filter acts as a pulse compressor for each frequency component of the original signal, delivering an amplitude peak delayed in time proportionally with the input frequency. The detected output then represents

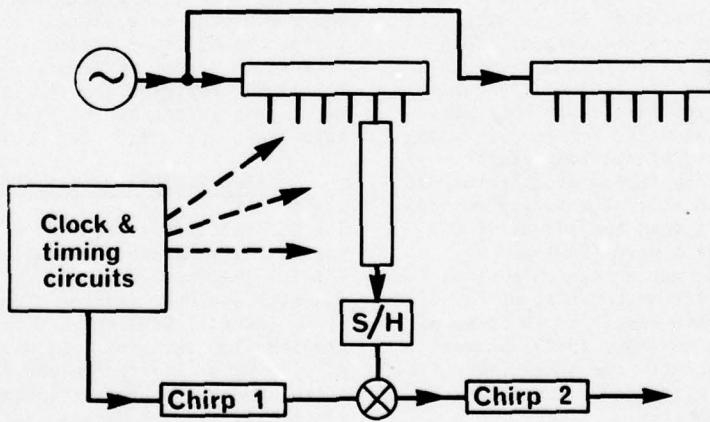


Fig 2 Experimental Configuration

the amplitude-frequency spectrum of the input signal from one range interval and threshold detection can be applied. The noise against which the signal competes is limited to that within the resolved Doppler bandwidth which is of order $(P T)^{-1}$ and the time of threshold crossing can be interpreted in terms of the target radial velocity.

EXPERIMENTAL VALIDATION

Available components have been assembled to establish the feasibility of the CCD-SAW approach. A 100-sample linear CCD has been used to store data in a way representing a single range cell system. Fig 2 shows how the data is fed to the store from a tapped analogue delay line which receives the radar bipolar video signal. The choice of tap used represents the radar range examined (the first tap corresponding to the furthest range cell). Each tapped line is clocked at 4 MHz, corresponding to a range cell spacing of about 40 m, in bursts repeated at 4 kHz (the simulated prf). Following each burst the CCD store is clocked once until, after 1CO cycles, it is filled with new data. At this point 100 clock cycles are applied at 4 MHz to read out the store into the spectrum analyser. Readout takes only 25 μ s and therefore can be fitted in during an inter-pulse period of 250 μ s provided that less than 90% of the unambiguous radar range is being processed.

The time compression of 1000 (25 ms: 25 μ s) expands the bandwidth so that a spectral resolution of ~ 40 kHz, achievable with SAW processing, becomes adequate since it corresponds to 40 Hz for the real-time signal. The unwanted clock waveform components present in the CCD output are removed using a sample-hold circuit so that a reasonably smooth signal is presented to the spectrum analyser. The spectrum is derived using the principles given by Edwards and Withers (1), here using dispersive SAW filters both to replace the active swept oscillator and to provide the pulse compression which separates the spectral components of the signal.

An impulse to the first SAW filter produces a chirp signal at a convenient IF, starting at the same time as the CCD output. The mixer then outputs chirp signals offset by frequencies $\pm f$ for each frequency component f of the CCD output. The second SAW disperser, having an impulse response with the

same frequency-versus-time slope but opposite sign, acts as a pulse compression filter: each offset chirp giving rise to a peaked output with a time delay proportional to f .

Fig 3 makes this clearer for the case when only one component, at frequency f , is present and the second filter, chirp 2, has twice the bandwidth W of the generated chirp in order to accommodate frequency shifts due to input signals within a bandwidth W without amplitude loss. It will be seen that the time sidelobe levels are increased by the proximity of the image component peaks. This can be avoided by first mixing the baseband signal to an IF of at least W , enabling the lower sideband from the mixer to be suppressed by filtering as described by Edwards and Withers.

The present experimental system is below optimum in many respects but the means of improving its performance are at hand. The single range cell limitation can be overcome by adding more CCD storage elements and it should be noticed that the serial-to-parallel section can be extended indefinitely as in Fig 2 using suitably clocked tapped lines rather than a single longer one. The direct CCD output to the mixer will be replaced by a multipole analogue switch and the timing circuits elaborated to sequence the operations. Up to the present SAW filters designed for other purposes have been used: an amplitude weighted chirp 1 with 2 MHz dispersion over 20 μ s (not 25 μ s) has been combined with a similar but unweighted filter for chirp 2. The Taylor weighting is desirable to reduce the spectral sidelobes but its effect is vitiated by the inadequate bandwidth of chirp 2 which does not accommodate frequency shifted signals, thereby losing signal energy, worsening the spectral resolution and abruptly truncating the weighting function. A special purpose pair of filters will shortly be available to overcome these disadvantages.

Fig 4 illustrates the important waveforms in the existing system. Trace (a) shows a simulated video input to the analyser, a sinusoidal signal representing a target doppler frequency of 200 Hz. After the clocking-in sequence, each terminal of the tapped line holds an amplitude sample for a particular simulated range ready for input to the CCD store. Trace (b) shows the output from one such tap. The samples

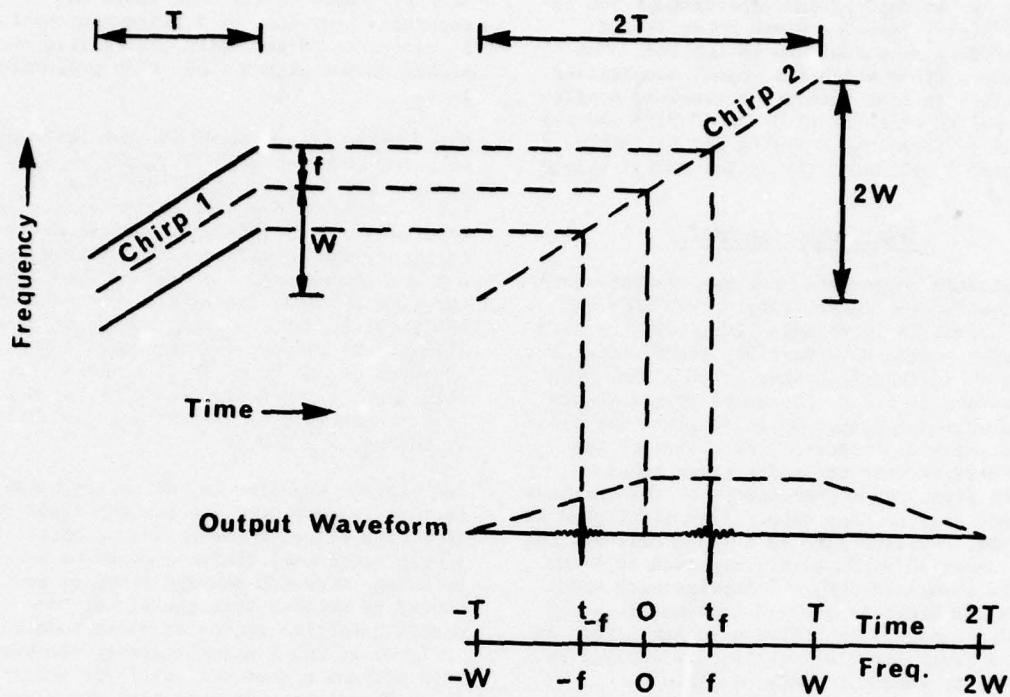


Fig 3 Time-Frequency relations for Spectrum Analyser

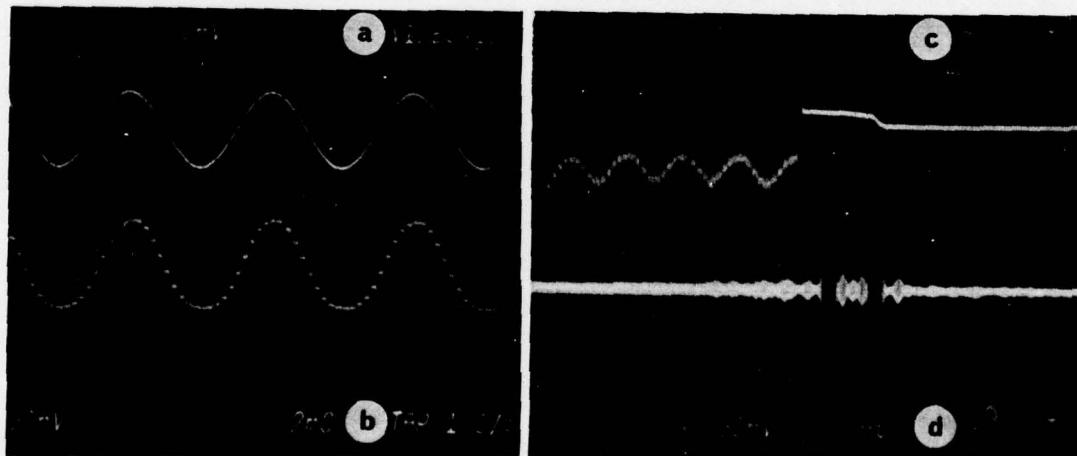


Fig 4 Waveforms in Experimental System

CONCLUSIONS

The experiments so far made with a skeleton system using a CCD of obsolescent type and SAW filters which were not designed for the purpose in hand have indicated that with predictable technological and design improvements, a pulse doppler processor can be built to suit real radar system requirements. A processor with 40 dB dynamic range, 30 dB spectral sidelobes and 10 MHz bandwidth seems capable of achievement and this, allied to the fact that standard components can be used to cover a range of radar parameters, should ensure its usefulness. The dynamic range limitation may be the most serious one since radar signals frequently contain clutter echoes of much greater amplitude than the wanted targets. However radar systems using swept gain (STC) and some clutter filtering prior to doppler processing should certainly be able to take advantage of the cheapness and flexibility of this relatively simple processor.

FURTHER DEVELOPMENT

We have described a processor conceived in terms of discrete component CCD elements combined to form an analogue storage matrix with orthogonal and dual speed input/output. This function is strongly reminiscent of the serial-parallel-serial CCD which suggests that an integrated circuit form of orthogonal input/output store might be possible. The difficulty is in building in sufficiently flexible clocking controls so that the contents of individual range stores can be accessed one by one without disturbing the others. The attractions of using such an integrated store are such that we are developing one storing data from 100 pulses and 10 ranges which will effectively do this by right-shifting the whole data matrix as indicated in Fig 5 so as to successively bring columns of data into a fast readout register with independent clock control. The freedom to move the matrix either vertically (during input) or horizontally (for output) demands a new type of clock line structure, a possible one using a two-level polysilicon process with an aluminium overlay being proposed elsewhere (2). The storage module will allow coherent processing of data from up to 100 radar pulses. If the requirement is smaller than this (it is usually limited by the number of pulses

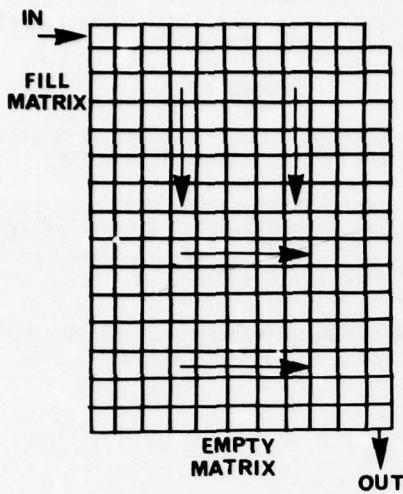


Fig 5 Integrated Storage Module Concept

corresponding to a particular range are transferred to the CCD store by a single cycle of the 4 kHz input clock. When the CCD store is filled, a burst of 100 clock cycles at 4 MHz is applied to empty it, producing the active section of waveform (c), the time-compressed range gated video in a form compatible with the SAW analyser. Some distortion of the ideal sinusoidal trace is evident. This is expected to improve in the next generation of devices but even this degree of distortion does not prevent the spectral peaks being easily distinguished in the spectrum output (d) from the SAW analyzer. The two main peaks correspond to the upper and lower sidebands of chirp 1, both are of equal amplitude because the up and down-shifted chirps have both moved partially outside the bandpass of the compression filter, by equal amounts in opposite directions. Zero frequency of the input spectrum corresponds to the point midway between the peaks. The first peak is in a region that would normally be suppressed by time gating in a real system context. The spurious frequency sidelobe levels arise from the signal distortions within the CCD and from the upsetting of the Taylor weighting of chirp 1 by the use of too short a compression filter (chirp 2).

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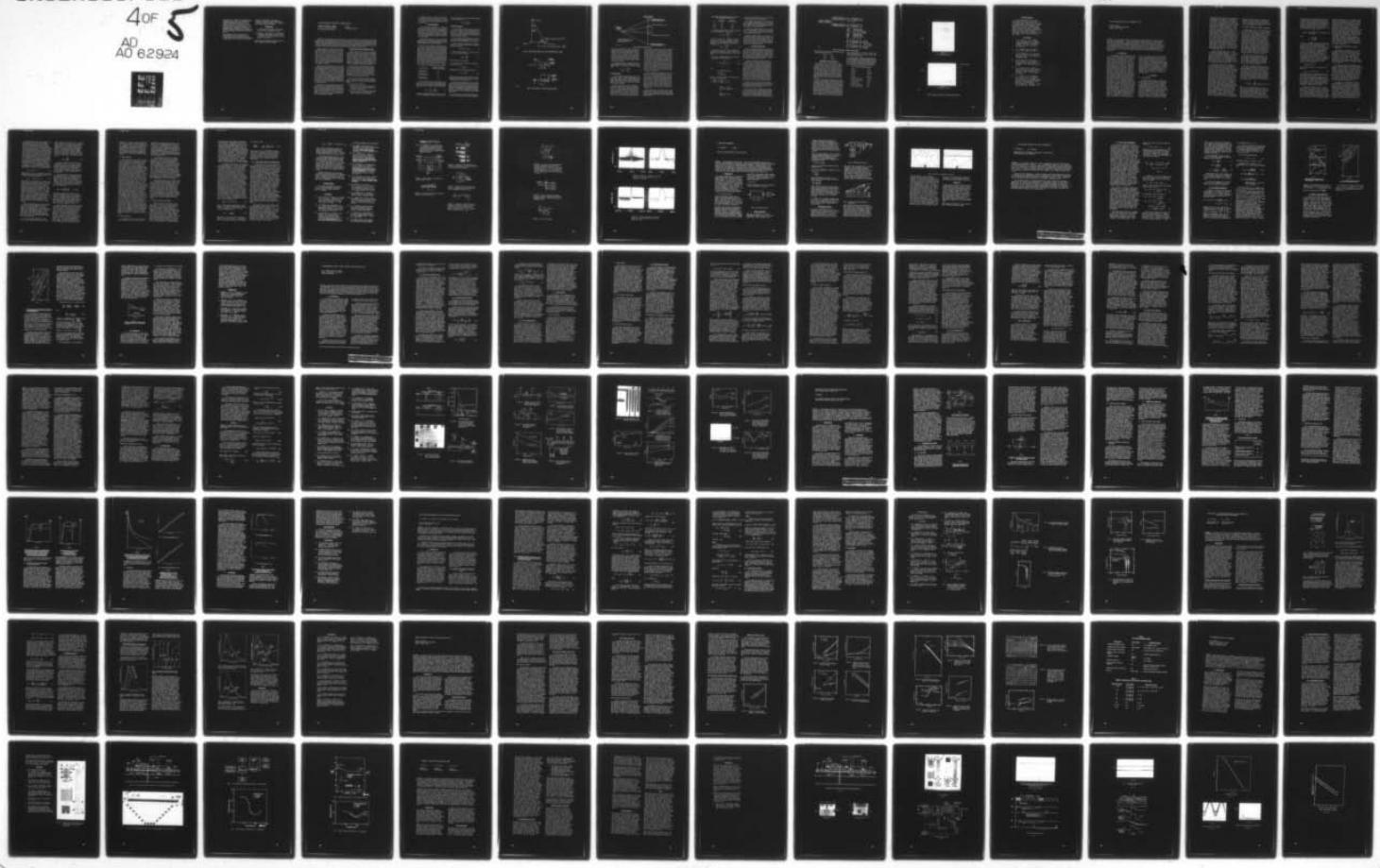
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directed on to a target by a scanning beam), storage capacity can be wasted merely by clocking the CCD output at a rate which matches the duration of the data to the length of chirp 1, and impulsing the chirp only when real data begins to appear. The required number of range cells is accommodated by using sufficient storage modules, each being clocked in sequence for input and output.

The integrated circuit architecture is incompatible with the interleaved input/output scheme described previously so that a duplicate store is required, one acquiring

data while the other is read out for analysis, nevertheless there should be a worthwhile saving in package count compared with the discrete CCD version.

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CCD APPLICATIONS TO SYNTHETIC APERTURE RADAR

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ABSTRACT. Radar imaging using side-looking synthetic aperture radar techniques is the best known approach for achieving high resolution imagery through atmospheric cloud cover. On-board processing for satellite and small aircraft applications has been prohibitive because of size, weight, and power constraints for digital processors. The powerful computational equivalency of a CCD transversal filter drastically alleviates these constraints, making a CCD image processor feasible for such applications. This paper contains an abbreviated discussion of synthetic aperture principles from which range and azimuth correlators can be defined for a given application. Discussions of CCD constraints, a CCD system design, and a breadboard system are included.

Radar imaging using side-looking synthetic aperture radar (SAR) techniques is the only viable means of achieving high-resolution imagery through atmospheric cloud covers. However, if the radar echo data are not processed into images onboard the spacecraft or aircraft, and if multiple looks are required to achieve acceptable quality, potentially large quantities of raw uncorrelated data must be sent to the ground for processing. Conversely, if images are produced onboard, the multiple-look images may be superimposed into single images and conventional data-compression algorithms may be applied to significantly reduce the data volume and rates transmitted to the ground.

During recent years, considerable effort has been devoted to developing onboard digital data processing of the radar echo data. Unfortunately, results to date indicate that the digital data processing required to produce correlated radar images onboard a spacecraft or small aircraft is normally impractical from cost, complexity, power, size, and weight standpoints. Since only limited compression by means of presumming and time expansion can be accomplished with the uncorrelated radar echo data, proposed radar mission requirements to date have implied the need for reliable high-speed and high-capacity tape recorders for storage, and have imposed potentially severe requirements upon the telecommunications link and ground data handling capabilities.

The discovery of the CCD transversal filter concept¹ has greatly simplified the complicated digital implementation of convolution. A CCD transversal filter of length N bits provides N bits of analog storage while performing N analog signal by weighting coefficient multiplications each clock period. By resolving the SAR processor into a range chirp correlator followed by an azimuth chirp correlator, a considerable reduction in on-board hardware is achievable.²

PRINCIPLES OF SYNTHETIC APERTURE RADAR

Generally speaking, when an image of some physical characteristics is needed, the resolution in the two orthogonal directions should be approximately equivalent. This presents a problem to conventional radar sets which could be used to produce an image of the radar cross section of a section of terrain. The resolution of the conventional radar in the radial direction depends directly on signal bandwidth. Pulse-compression techniques permit signal bandwidth to be expanded with negligible sensitivity loss so that adequate range resolution may be realized for many imaging applications.

Azimuth resolution is a more difficult matter, however. Conventional radar azimuth resolution depends ultimately upon the antenna beamwidth.³ The antenna beamwidth is reduced by increasing the size of the aperture, increasing the carrier frequency, or both. For long-range imaging, however, this approach cannot provide an azimuth resolution which is comparable to the range resolution that can be realized easily with modern pulse-compression techniques.

The solution to this dilemma is provided by synthetic aperture radars (SARs) in which data processing capability is traded for aperture size. In principle, there is no difference between:

An extremely large real antenna, and

A small real antenna that successively occupies all the positions that would be occupied simultaneously by the large real antenna, provided

The data that are successively collected by the small antenna are properly stored and subsequently combined in a simulation of the large real antenna.

Assuming this condition is satisfied, it is possible for a small antenna to move past a scene and record echo data to permit comparable range and azimuth resolution to be realized in an image of the scene after the recorded data have been properly processed.

RANGE PROCESSING

Linear FM chirp pulse compression is an example of spread spectrum techniques which have the properties that probability of detection and resolution are essentially independent quantities. The amount of energy which the transmitter puts into the pulse determines the probability of detection independently of signal bandwidth, assuming a matched-filter receiver. The signal bandwidth is the major factor which determines range resolution.

The principal signal parameter of interest is the RF signal chirp bandwidth, Δf . This parameter defines the compressed pulselength. Table 1 shows the compressed pulselength for three different weighting functions for the matched filter.

Table 1 shows that, in general, the 3-dB compressed pulselength is given by a constant divided by the signal chirp bandwidth, where the constant depends on the type of weighting used, if any, to reduce the range sidelobe level. Resolution is defined as the separation which must exist between two equally strong targets in order for their individual compressed pulse responses to intersect 3 dB below their peak response level. The compressed pulselength expressions in Table 1 also give the range resolution for an imaging system in the special case where the radar lies in the plane of the scene being imaged. Actually, the radar will be located above the plane being mapped. This means that the compressed pulselength expression of Table 1 must be projected into the plane of the scene in order to obtain the effective range resolution appropriate to the scene.

Table 1. Dependence of Compressed Pulselength on Type of Weighting^a

TYPE OF WEIGHTING	COMPRESSED PULSELLENGTH (MEASURED AT 3-dB POINTS)
Gaussian envelope (-40-dB time sidelobes)	$\frac{1.5}{\Delta f}$
Rectangular envelope (-13.5-dB time sidelobes)	$\frac{0.9}{\Delta f}$
Hamming weighting (-42.8-dB time sidelobes)	$\frac{1.3}{\Delta f}$

Figure 1 shows that the slant range resolution is $c\tau_c/2$ where c is the speed of light and τ_c is the compressed pulselength measured at the 3-dB points. Consequently, the range resolution in the plane of the scene is $c\tau_c/2 \sin \theta$ which reduces to

$$\delta_R = \frac{c\tau_c}{2 \sin \theta} = \frac{0.45 c}{\Delta f \sin \theta} \quad (1)$$

for the case of unweighted linear FM from Table 1. The range correlator's time-bandwidth (TW) product can be defined for a

given range resolution and look angle (or chirp bandwidth) and transmitted pulselength, T_p , as

$$TW_R = \frac{0.45 c T_p}{\delta_R \sin \theta} \quad (2)$$

AZIMUTH PROCESSING

The basic parameters relating to SAR geometrical relationships are shown in Figures 2 and 3. It is convenient in Figure 3 to think of a stationary radar with target motion being a straight line, as shown. Using conventional terminology, time t is zero when the target is at the point of closest approach. This minimum range value is called R_o .

Data are assumed to be available from the time that the target enters the 3-dB beamwidth point of the real aperture until it leaves the 3-dB beamwidth point on the other side.

At time t , the target is seen in Figure 3 to be displaced a distance Vt from the point of closest approach. The range as a function of time is given by

$$R(t) = (R_o^2 + V^2 t^2)^{1/2} \quad (3)$$

From geometrical considerations, the Doppler frequency can be found as a function of time to be

$$f_D(t) = \frac{-2V^2 t}{\lambda R(t)} \quad (4)$$

where λ is the radar carrier wavelength.

For most cases of interest, the distance Vt in Figure 3 is much less than R_o , so that

$$R(t) \approx R_o \quad (5)$$

The Doppler expression in Equation 4 is approximated by

$$f_D(t) \approx \frac{-2V^2 t}{\lambda R_o} \quad (6)$$

which shows the linear FM chirp characteristic of the Doppler shift between the transmitted and received pulse as a function of the relative position of a point reflector.

The major conceptual difference between the azimuth and range chirp signal is in the signal duration. The range chirp pulse has a rather well-defined start and stop duration. The azimuth chirp modulation has no such well-defined time epoch. The phase of this modulation is determined by the geometrical parameters, but the amplitude is determined by the antenna pattern. As a result, there is the arbitrary matter of azimuth signal duration.

As a practical matter, the effective azimuth signal duration is defined by the signal processor. The charge coupled device

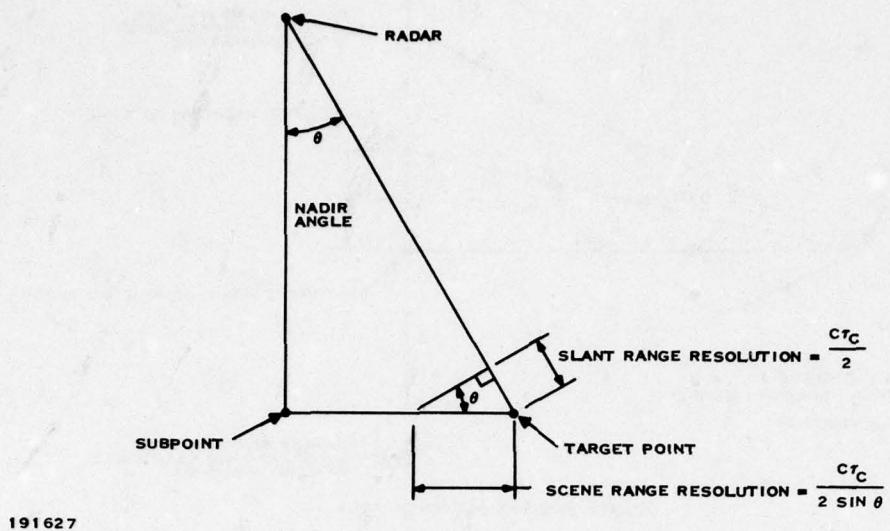
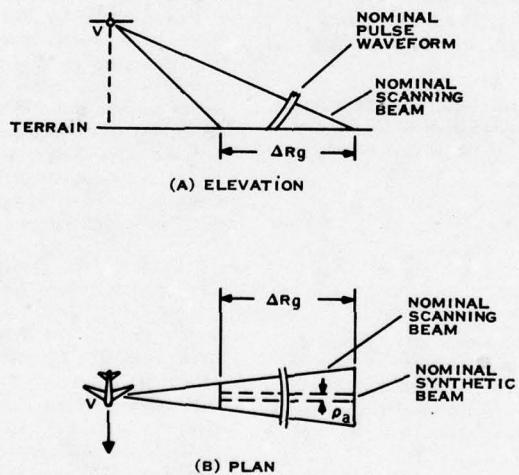


Figure 1. Range Resolution Dependence on Compressed Pulsewidth and Look Angle



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Figure 2. Typical Geometry of Synthetic Aperture Radar System

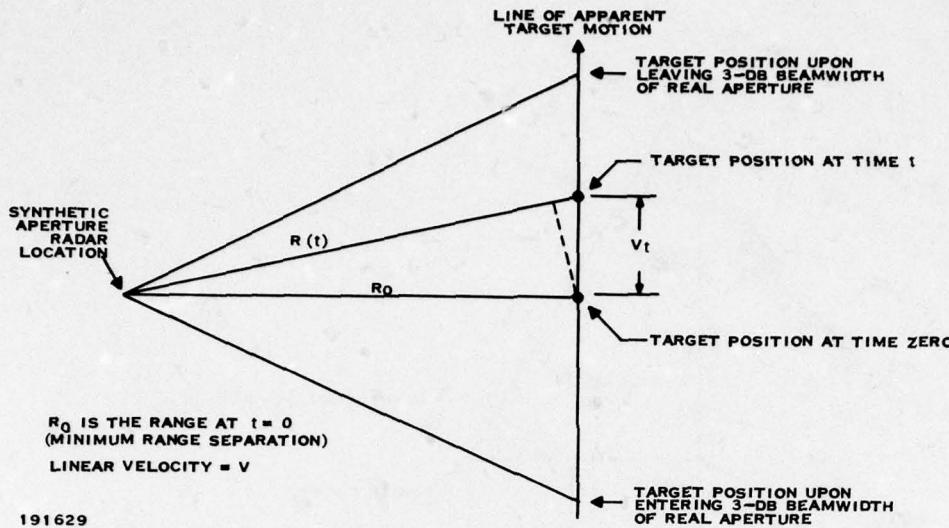


Figure 3. Basic SAR Azimuth Geometry

(CCD) processor functionally contains many azimuth correlation filters which are analogous to the range correlation filters. The azimuth Doppler modulation defined by Equation (6) is assumed to be the signal input to an azimuth correlation filter. The difference is that an azimuth correlation filter needs to process only those signals which correspond to reflectors at the same range. This requires that the echo pulse be divided into range bins following range compression with distinct azimuth correlation filtering provided for each range bin.

The relationships in Table 1 also hold for azimuth compressed pulsedwidth. Assuming an unweighted filter, the compressed pulsedwidth at the output of the azimuth correlation filter is

$$\tau_c = \frac{0.9}{\Delta f_{AZ}} = \frac{0.45\lambda R_0}{V^2 T_{AZ}} \quad (7)$$

CCD CONSTRAINTS

The above described resolution constraints as well as other radar system constraints provide physical guidelines for the system design. However, a number of CCD operational constraints⁵ which include data rates, charge transfer efficiency, leakage current, and device size are also key factors in determination of the system design.

Equation (1) indicates that chirp bandwidths of approximately 10 MHz may be expected for range resolution in the 10- to 50-meter category. Processing at the Nyquist rate for such a chirp waveform with CCDs represents a difficult implementation task due to feedthrough and bandwidth problems, potentially severe clock power requirements, and possible charge transfer efficiency problems. Since the modular concept allows each module to

process on the order of 200 range cells, it becomes possible to sample the radar video at a high rate during a small time window corresponding to the module's swath width once each PRI. The number of samples to be stored is the number of bits required to cover the swath plus the number of bits in the range correlator. While the input sampling rate is constrained by Nyquist considerations, the output data rate is constrained by the PRI making time expansion of the video possible in order to reduce the processor module's data rate. The use of low pass recursive presum filtering techniques offers further reduction in the data rate and storage requirements. Following time expansion, the samples are clocked into a complex (I and Q) CCD correlator which performs pulse compression on the received chirp radar returns at a clock rate of 1 MHz or less, avoiding the high-frequency video design requirements and possible high-frequency CTE degradation.

Charge transfer efficiency requirements for this SAR design does not represent a serious problem with the present state of the art. Table 2 indicates the effects of CTE upon range resolution for a Hamming apodized, Nyquist sampled correlator having a TW product of 62. The relative resolution is the ratio of the -3-dB correlation pulsedwidths for each CTE to the ideal transfer case. CTEs greater than 0.999 appear to result in minimal resolution degradation. In multiple-look SAR systems requiring cascaded azimuth correlators, CTE requirements are more demanding than indicated in Table 2. Also, leakage current problems appear to be more severe.

Equation (8) indicates the inverse relationship between azimuth correlation time and resolution. Since integrated leakage current can ultimately fill the potential well containing the charge signal sample, leakage current will ultimately limit azimuth resolution.⁶

Table 2. Resolution and Amplitude Degradation as a Function of CTE for a Correlator Having a TW Product of 62

CTE	RELATIVE RESOLUTION	RELATIVE ATTENUATION (dB)
1.0	1.000	0
0.999	1.005	-0.068
0.99	1.047	-0.673
0.99	1.679	-5.757

The azimuth resolution distance is obtained by multiplying this compressed pulselwidth by velocity to obtain

$$\delta_{AZ} = V\tau_c = \frac{0.45\lambda R_0}{VT_{AZ}} \quad (8)$$

for an ideal processor which is unweighted. Amplitude weighting has the effect of broadening the compressed pulselwidth and reducing the sidelobe level. Equations (7) and (8) define the azimuth correlator's TW product for the unweighted case as

$$TW_{AZ} = \frac{0.405\lambda R_0}{\delta_{AZ}^2} \quad (9)$$

Equation (8) shows that the azimuth resolution can be improved only by increasing the azimuth correlation time, assuming that the geometrical parameters R_0 , λ , and V are fixed.

The amount of integrated leakage current contributed to the charge packet at the k^{th} bit location is

$$\Delta Q_{KL} = \int_0^{T_c} J_{KL} A dt \quad (10)$$

where

J_{KL} = leakage current density

A = bit area

T_c = clock period.

The effect of the leakage current upon the transversal filter's output is seen from the relationship

$$\begin{aligned} V_{out} &\propto \sum h_K Q_K = \sum h_K (Q_{KS} + Q_{KL}) \\ &= \sum h_K Q_{KS} + \sum h_K Q_{KL} \quad (11) \\ &= \sum h_K Q_{KS} + \text{constant} \end{aligned}$$

where Q_{KS} is the signal charge and Q_{KL} is the integrated leakage current present in the k^{th} storage location.

The integrated leakage current at the k^{th} location for a constant clocking rate and temperature is a constant which, when multiplied by the weighting coefficient h_K (a constant) gives a constant. Therefore, the integrated leakage current has a first order effect of an output dc level shift.

Since the total integrated leakage current (Q_{KL}) increases linearly (excluding statistical variations) down the transversal filter, the transversal filter is much more tolerant of leakage current than other CCD device types.

Satisfactory correlator operation can be achieved with integrated leakage currents on the order of ten percent of a full well at the CCD output. Azimuth correlation times of 0.5 second have been achieved at room temperature. Longer correlation times, multiple looks in azimuth, or higher temperature environments may require improved leakage current characteristics or the use of thermoelectric coolers.

SYSTEM CONFIGURATION

The system represented in Figure 4 has been developed to avoid many of the operational difficulties experienced with CCDs. The input sampler stores samples of the appropriate swath width at the high frequency rate required by range resolution and Nyquist considerations. The sampler's output rate is constrained by the number of samples stored and the PRI. The optional presum filter permits reduction in the length of the azimuth correlators and in the data rate.

Following time expansion, the samples are clocked into a complex (I and Q) CCD correlator which performs range pulse compression on the received chirp radar returns. The output signal sequence is a complex (I and Q) representation of radar cross section (amplitude) versus range (time). By range sorting this output, it may be observed that returns in a given range bin on sequential PRIs are samples of the Doppler chirp from a target. Therefore, pulse compression in azimuth may be achieved by functionally feeding the range sorted samples into a bank of azimuth chirp correlators each PRI. The pulse compression performed by the correlators is responsible for the Doppler beam sharpening attendant with the SAR azimuth resolution improvement. The azimuth correlators also subtly perform the analog storage of sequential radar returns as required by basic SAR principles.

The I and Q outputs of the azimuth correlator bank are then multiplexed, squared, and summed to form a video line in the range direction. An additional line corresponding to subsequent azimuth positions occurs each PRI.

The system can easily be configured into a modular concept where modules may be stacked to provide additional coverage in the range dimension. This also facilitates the use of range correlators having different chirp slopes to avoid defocusing problems present in some applications. An estimate for such a module covering a 10-km swath width with 50-m resolution

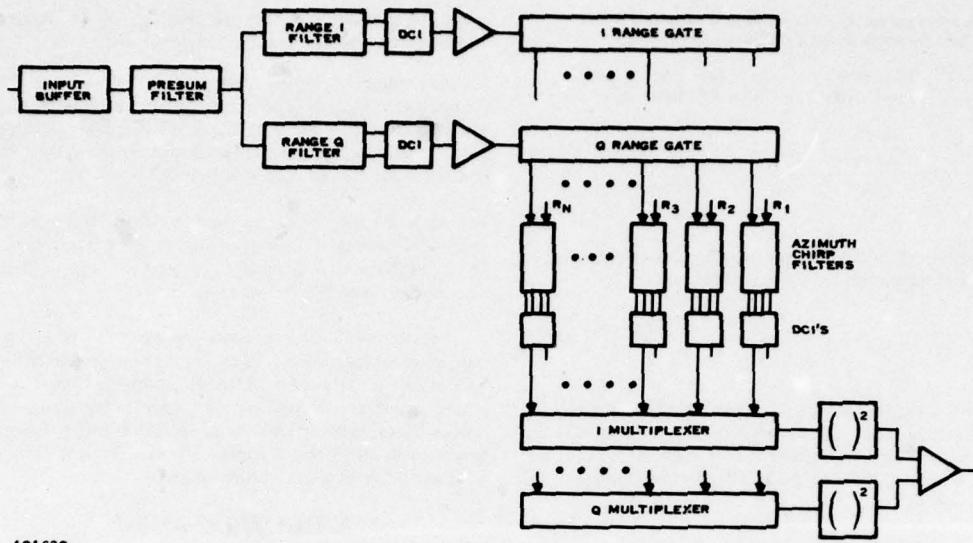


Figure 4. Synthetic Aperture Radar Functional Diagram

from an altitude of 800 km, indicates the following parameters are achievable with such a processor.

Weight	≤ 7 lb
Size	≤ 150 in ²
Power	≤ 7 watts

BREADBOARD AND TEST SYSTEM

A simplified version of the system shown in Figure 4 has been constructed to demonstrate the processor concept. A single azimuth correlator was constructed which is sequentially stepped through the 200 range bins with a minicomputer in order to minimize hardware construction. The radar/platform parameters for this breadboard system shown in Table 3 are relatively representative of an aircraft radar environment. Range and azimuth correlation is accomplished with Hamming weighted linear FM complex filter pairs having TW products of 62 and 16, respectively. Range and azimuth correlation times are 0.47 ms and 0.5 s, respectively.

In order to form a 200- by 200-element picture with this breadboard, a TI 960A computer with a 28K memory used in conjunction with a 1,100,000 word disk memory and a nine-track, 800-BPI magnetic tape unit were used. The simulated radar echo pulses were transferred from the tape to the disk. The simulated radar bursts correspond to radar returns from a swath of interest at sequential azimuthal locations. By recirculating this sequence of bursts to the breadboard while sliding the azimuth read-in time window across the swath time, a complete picture can be processed an azimuth column at a time. To reconstruct the picture, the output of the azimuth correlator is digitized and stored in memory. The memory can

then be used much as a scan converter to refresh a CRT display. Full implementation of the azimuth correlator bank would provide real time processing.

Figure 5(A) indicates a portion of the uncompressed video signal corresponding to 48 point targets arranged in four rows in the range dimension. The point targets have a random signal phase and increase in intensity along the azimuth direction in 2-, 4-, 6-, and 8-percent increments for each of the range rows. The compressed point target image is shown in Figure 5(B).

Table 3. Breadboard Radar/Platform Parameters

Altitude	5.0 km
Slant Range	10.0 km
Nadir angle	60.0 degrees
Velocity	320.0 m/s
Wavelength	32.0 cm
Frequency	936.84 MHz
Transmitted pulse duration	3.58 μ s
Transmitted signal bandwidth	17.32 MHz
Echo pulse duration	15.12 μ s
Slant-range resolution	8.66 m
Along-track ground resolution	10.0 m
Cross-track ground resolution	10.0 m

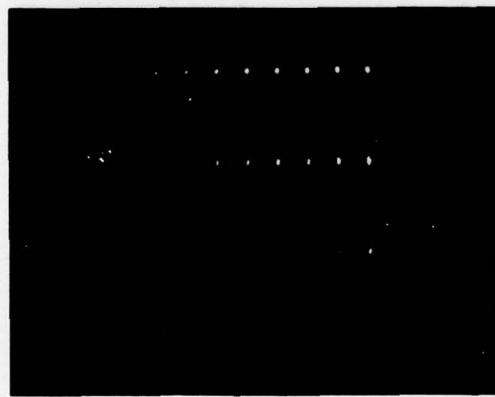
RANGE



AZIMUTH

(A) UNCOMPRESSED VIDEO

RANGE



INTENSITY STEPS

8%

6%

4%

2%

AZIMUTH

(B) PROCESSED PICTURE

191631

Figure 5. Image Processor Response to Varying Intensity Point Targets

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A SELF CONTAINED 800 STAGE CCD TRANSVERSAL FILTER

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ABSTRACT. CCD transversal filters are capable of high performance in a wide variety of filtering applications. To date the widespread application of CCD filters has been hampered by the complexity of peripheral external circuits required to operate the CCD. We have exploited the MOS/LSI compatibility of CCD's to fabricate a completely integrated and self-contained 800 stage CCD transversal filter. The device is designed as a tunable bandpass filter with a 3 dB bandwidth of 0.7% of the center frequency and 40 dB sidelobes. A novel concept employing CCD structures as voltage amplifiers has been utilized in this device. Preliminary measurements of the device performance are presented.

I. INTRODUCTION

The tremendous signal processing capability of CCD transversal filters has been demonstrated in applications such as spectral filtering,^{1,2,3} the chirp z transform,^{4,5,6} and correlators for radar⁷ and spread spectrum communication.⁸ The relative simplicity of the split electrode tap weight technique¹ is the major reason for the versatility of CCD filters. However, a serious drawback to CCD filters used to date has been the complexity of external peripheral circuits required to operate the CCD. The full potential of CCD filters can only be realized by taking advantage of the MOS/LSI compatibility of CCD structures and integrating the required CCD support functions on the chip with the CCD. This paper deals with the design and performance of a fully integrated, 800-stage transversal filter chip which contains the CCD filter, its clock generator and drivers, an input amplifier, and an output amplifier as shown in Figure 1. On this CCD chip the clock waveforms are derived from a single master clock signal. The input and output amplifiers employ a charge coupled structure to achieve voltage amplification with low noise, high speed, and low power consumption. The device is designed so that only DC voltages and one master clock signal are required to be supplied exter-

nally. To facilitate analysis and testing of this prototype design, five different DC biases are required, but some of these levels could be derived on the chip in future designs. The weighting coefficients were designed for a tunable narrow bandpass with a 3 dB bandwidth of 0.7% of the center frequency and a -40 dB sidelobes. A simple reprogramming of two photomask levels would convert the filter to other correlator functions or to transfer functions such as lowpass, highpass, Hilbert transform or notch filters.

II. DESIGN

A) CCD STRUCTURE

Although CCD transversal filters can be constructed with two phase, three phase, or four phase CCD structures, we selected a three phase structure as a compromise between charge handling capacity, fabrication difficulty, overall size of the CCD, and clocking complexity. The device structure is an adaptation of the three metalization level, three phase CCD described by Bertram, et al.⁸ In this case as illustrated in Figure 2 the device is fabricated with two polysilicon levels and one aluminum level. Each clock phase is on a sepa-

rate metallization level thus easing photolithographic requirements. As pointed out by Bertram et. al. this structure offers significant yield advantages for large CCD structures. Furthermore it simplifies layout of the electrode structure for the split electrode tap weighting technique. Each electrode is 0.3 mils by 6 mils with 0.05 mil overlap to adjacent electrodes. Thus each cell of the CCD is 0.9 mils by 6 mils. The packing density of this structure is higher than four phase and comparable to the packing density we could obtain with two phase structures of comparable charge capacity. Another advantage of the three level structure is that it allows the use of a four level sandwich consisting of the three metallization levels and an n+ diode diffusion to construct large capacitors in a minimum area. Two 300 pf capacitors were constructed in this way for use in the output circuit of the filter. The CCD is fabricated on 40-70 ohm cm p-type substrates with 1500A gate oxides.

The CCD has 800 stages and in order to achieve practical dimensions it is folded into four 200-stage segments. This technique of folding the CCD allows the CCD portion of the filter to be fabricated in a 200 by 60 mil area. The remainder of the 200 mil by 140 mil chip is devoted to the CCD support circuitry and test devices which are devoted to process monitoring.

Folding the CCD into four segments is made possible by the use of a diode and dc bias gate^{5,6} as shown schematically in Figure 2. The basic principle of operation is that the corner diode is preset to fixed potential during each clock period by spilling charge over the dc gate. Once each clock period a new charge packet is introduced onto the corner N⁺ diffusion from the preceding clock electrode Ø₃, thereby lowering its potential below the threshold of the DC gate. Current then flows under the DC gate until the diffusion is restored to the threshold point at which time essentially all of the signal charge is transferred to the following clock electrode Ø₁ and the diode is left at the same potential it had at the beginning of the cycle. Great care is taken to minimize the capacitance of the corner diffusion and minimize its charge transfer loss. Analysis of the corner leads us to expect the fractional transfer loss to be less than 1% at frequencies up to 10 MHz if a fat zero charge equal

to 10% of a full CCD well is maintained.⁶ Computer simulations of the transversal filter show that the effects of the corner loss at this level and below are negligible in the performance of the filter.

B) OUTPUT DIFFERENTIAL CURRENT INTEGRATOR

Realization of the full performance capabilities of CCD transversal filters places difficult requirements on the output amplifier circuit. As reviewed below, the split electrode tap weight technique requires a differential voltage amplifier having a high common mode rejection, high dynamic range, wide bandwidth, and good linearity. Low power consumption is also desirable particularly for very low frequency operation where chip heating would increase dark current and limit the useful delay time in the filter. Conventional linear MOS circuits are inadequate to meet these requirements and a new concept has been incorporated in this CCD filter design. The new concept utilizes a CCD structure as a differential voltage amplifier as described below.

We shall review the operation of the transversal filters constructed with the split electrode tap weighting technique. This review is followed by a discussion of the output amplifier circuit requirements. The amplifier design integrated on our chip is then presented.

The split electrode tap weighting technique¹ takes advantage of the fact that as signal charges are transferred along a CCD an image charge must flow into the clock electrodes. By splitting all of the phase two electrodes at various lateral positions along the CCD and measuring the difference in charge required by the clock lines driving the split electrodes we obtain the output signal. The differential charge at time nT_c is given by

$$q_{out}(nT_c) = \sum_{m=1}^N h_m C_{e\text{vin}}(nT_c - mT_c) \quad (1)$$

where T_c is the clock period, N is the number of delay stages, and the sign and magnitude of each weighting coefficient h_m is determined by the position of the split in the electrode. The signal charge packet which is introduced at the input at t=nT_c is q_{in}=C_evin(nT_c) and C_e is the gate oxide capacitance of one CCD electrode. As illus-

trated in Figure 3 the differential charge is measured by integrating the clock line current in series capacitors C_i^{\pm} and amplifying the resulting differential voltage variations on the capacitors. The differential output voltage of the CCD filter which appears at the input of the voltage amplifier is related to the input signal by

$$v_o(nT_c) = \frac{1}{R N C_e} \sum_{m=1}^N h_m C_e v_{in} (nT_c - mT_c) \quad (2)$$

where

$$R = \frac{C_i^{\pm} + C_{\theta 2}^{\pm}}{N C_e},$$

$-1 < h_m < +1$, and $C_{\theta 2}^{\pm}$ is the total capacitance of each of the split phase clock lines. The gain required of the voltage amplifier depends on the gain factor of the CCD filter which is less than unity. This attenuation of the filter depends on the capacitance ratio R and the weighting coefficients or transfer function used in the filter. A small value of the integrating capacitors C_i increases the gain of the filter but attenuates the clock amplitude. We selected a compromise value of $C_i = 300$ pf to obtain a ratio $R = 2.2$. This value of R and the narrow bandpass weighting coefficients result in a filter gain of

$$\left| \frac{V_o}{V_{in}} \right| \approx 0.14 \quad (3)$$

when the input signal at the passband frequency is

$$v_{in}(t) = V_{in} \sin(\pi f_c t / 2). \quad (4)$$

The designed gain of the differential voltage amplifier on this chip is $G = 10$ resulting in an overall gain $|V_{out}/V_{in}| = 1.4$. Note that the differential voltage amplifier must reject the common mode 15V clock waveform. Also, if the filter is to be operated at frequencies up to a few megahertz the differential amplifier must have sufficient bandwidth to operate in this range.

The overall dynamic range is largely determined by the noise level of the output amplifier. The reason is that the CCD filter is an inherently low noise device. Furthermore, noise introduced at the filter input or internally generated in the CCD is filtered by the device. Stated differently, charge packets in the CCD due to the matched signal

waveform add coherently in the filter output while noise charges do not. However, noise inherent in the output amplifier is not filtered by the CCD. The expected noise level of the CCD filter is on the order of $10 \mu V$ rms referred to the input of the output amplifier. This estimate includes input noise of the CCD, fast interface state noise, and the preset noise associated with driving the clock line capacitance. Therefore the wideband noise introduced by the output amplifier should be less than this level if the full dynamic range of the CCD is to be exploited. Assuming a signal bandwidth of 1 MHz the noise level corresponds to a spot noise spectral density of a few nanovolts/ $Hz^{1/2}$. This goal is difficult to meet and as we shall see the output amplifier determines the output noise level.

C) CHARGE COUPLED DIFFERENTIAL VOLTAGE AMPLIFIER

The amplifier integrated on our IC was designed with the previously discussed requirements in mind. The amplifier is shown schematically in Figure 4. The amplifier is basically a one delay stage CCD with a differential input circuit and a standard precharge output circuit. The inputs are applied to the gates labeled v^+ and v^- which correspond to the nodes with the same designation in Figure 3.

The input circuit of the amplifier utilizes a floating diffusion structure¹⁰ which operates on a "fill and spill" principle^{10,11,12} which is reviewed below. The amplifier described here makes use of the fact that the floating diffusion structure can be used with an inverting and a non-inverting input simultaneously to achieve a differential input. Also a metal gate was placed over the floating diode to increase its capacitance and minimize the contributions of the diode's nonlinear depletion capacitance.

Voltage gain is achieved by differentially presetting a large floating diffusion capacitor (C_1) with the input voltages and then transferring the charge to a smaller capacitance (C_2) at the output. The operation of differential input is illustrated in Figure 5. At the beginning of the input cycle the input diode is at a high positive potential (down on the potential energy plot in Figure 5b). When charge transfers under the θ_2 electrodes of the CCD filter, the differential output signal appears at v^+ and

v^- superposed on the θ_2 clock voltage. The input diode is pulsed to a low potential and then returned to its initial state. During this process electrons flow under the v^+ gate and fill the surface under the v^+ gate and the capacitor C_1 (which is formed by diode diffusion under a dc biased gate). As the input diode is returned to the initial state electrons flow back to the input diode until the surface potential on C_1 reaches the threshold of gate v^- and current stops. The surface potential profile at this time is illustrated in Figure 5b. Next the gate θ_2' is turned on, and electrons flow into the CCD well formed by the θ_2' electrode until the threshold of the v^+ gate is reached resulting in the surface potential profile of Figure (5c). This charge packet is then transferred in the normal way to the output node shown in Figure 4. The input charge is

$$Q_{in} = C_{in}(v^+ - v^-) \quad (5)$$

where $C_{in} = C_1 + C_{v^+}$ is the sum of the floating diffusion and the gate capacitance of the v^+ gate. The output voltage is

$$v_{out} = C_{in}/C_2 (v^+ - v^-). \quad (6)$$

Thus the gain of the amplifier is simply the capacitance ratio C_{in}/C_2 . The amplifier was constructed with nominal values of $C_{in} = 3 \text{ pF}$ and $C_2 = 0.3 \text{ pF}$ for a gain of 10. Small non-linearities due to the depletion layer charge were neglected in (5) and (6). These non-linearities are small because: (a) the maximum signal swing for $(v^+ - v^-)$ is about 1V for the maximum signal level in the CCD filter. (b) these voltage changes are small relative to the back gate bias ($\sim 15\text{V}$) which minimizes changes in the threshold due to changes in depletion charge under the gates, and (c) the high resistivity substrates used minimize the depletion charge effects.

Note that the operation of the amplifier requires a dc offset between v^+ and v^- so that a bias change of 50% of the charge capacity of the amplifier is injected in the absence of a differential signal. The amplitude of the clock waveform applied to θ_2' electrode in the amplifier must be a few volts greater than the waveform applied to θ_2 of the filter. We used 20V pulses on θ_2' and 14V pulses on θ_2 .

All of the clock waveforms for the amplifier were derived from the clock wave-

forms required by the CCD filter. The total power required for the amplifier is approximately 20 mW. The speed of operation is determined by the rate at which the input capacitor C_1 can be preset by the gates v^+ and v^- . Following the results of Emmons and Buss⁷ and using the standard MOSFET equation $i = \frac{q}{2} (V_{gs} - V_T)^2$, we can determine the time required to achieve the full gain of the amplifier. The condition to be met is

$$\tau q \gg \frac{C_1^2}{B/2} \quad (7)$$

We shall assume a sufficient offset bias between v^+ and v^- such that $q \approx 6 \times 10^{-13}$ coulombs is the minimum charge injected. We have designed the input such that $B/2 = 5 \times 10^{-4}$. Evaluation of 7 reveals that $\tau \gg 30 \text{ nsec}$ is required. This condition is easily met at clock frequencies of 1-2 MHz or below.

The noise level of the charge coupled differential amplifier is dominated by the preset noise of the input capacitance C_{in} . There are two presets per input charge packet; one for the v^- gate and one for the v^+ gate. Each preset results in a variance of $(2kT/3C_{in})$ in the capacitor voltages.⁹ The resulting rms noise voltage at the output of the amplifier

$$v_{out}^n = 10 \left(\frac{4kT}{3C_{in}} \right)^{\frac{1}{2}} = 410 \mu\text{V}$$

The maximum usable output signal of the amplifier is approximately 2V rms. Therefore we expect a dynamic range of approximately 74 dB. The expected noise level of the amplifier is about 4 times greater than the noise generated in the CCD filter itself. Thus we have lost 12 dB of dynamic range due to the output amplifier noise.

Several advantages of the charge-coupled differential amplifier (CCDA) over a conventional differential MOSFET amplifier are summarized below. First the nature of the input circuit of the CCDA automatically performs a differential sample and hold operation. Use of an MOSFET amplifier would require sampling and holding of the v^+ and v^- voltages to avoid saturating the MOS amplifier with the large common mode clock signal. The gain of the CCDA is stable since it is determined by the ratio of two capacitances and is insensitive to

temperature or supply voltage fluctuations. Similar gain stability with an MOSFET circuit requires the use of high gain amplifier with feedback. The power requirement for the CCDA is approximately 20 mW as it is implemented in this filter. An MOS differential amplifier with similar bandwidth would require considerably more power particularly if the gain were feedback stabilized.

D) INPUT AMPLIFIER

Since the output noise level is dominated by the noise in the output amplifier, it is desirable to introduce gain at the input of the CCD filter for low signal level applications. This procedure of course does not increase the dynamic range but rather scales both the minimum and maximum signal levels by the same amount. On this CCD filter we have included a charge-coupled input amplifier which operates similarly to the output amplifier. The gain of 10 preamplifier can be bypassed if the input gain is not needed. If gain is required at the input of a transversal filter it is necessary to use linear voltage gain before the input of the filter. It is not desirable to achieve gain directly in the input of the CCD filter by the use of a large input capacitance such as the floating diffusion. The reason is that transversal filters utilizing split electrode tap weights require the use of an input in which the nonlinear contribution of the bulk charge under the tapped electrodes is exactly cancelled by the introduction of compensating charge at the input of the filter.^{1,5} This compensation is accomplished by the use of the diode input scheme shown in Figure 6, in which the signal is applied directly to the input diode. A dc gate isolates the input circuit from the clock transients and the input is gated on and off by the θ_1 clock voltage which is applied to the first CCD transfer electrode. This input scheme results in a linear relationship between the input signal voltage and the filtered output signal voltage appearing on the integrating capacitors. Therefore, we drive the input diode of the CCD filter with the voltage amplifier when gain is required at the filter input.

E) CLOCK CIRCUITRY

An important step in fully integrating a CCD transversal filter is efficiently

generating the clock voltages on-chip. The logic for our three-phase drivers is shown in Figure 7. The master clock C operates at twice the clock frequency and toggles the bistable flip-flop on each positive transition, generating Q and \bar{Q} . C is inverted and delayed through two series inverters to generate \bar{C}' . The clock phases θ_1 through θ_3 are generated by NOR-ing appropriate combinations of Q, \bar{Q} with C, \bar{C}' .

The NOR gates and drivers are shown in Figure 8. When both inputs to the NOR gate are low, T_4 is on and the bootstrap capacitor C_B (≈ 2 pF) becomes charged positively, thereby turning on the driver T_6 and pulling θ_p toward 15 V. The bootstrap capacitor remains charged and keeps the pullup driver on even after the clock line reaches 15 V. When the following phase θ_{n+1} goes positive, the voltage on the bootstrap capacitor is discharged through T_5 , thereby turning off the pullup driver; and the pulldown transistor T_7 is activated, thereby returning θ_p to ground. All clock circuitry is n-channel MOS with depletion loads and switching thresholds obtained by means of ion implants.

Advantageous properties of these drivers are (1) they provide three-phase clocks that overlap slightly at the crossover point; (2) they draw small quiescent power when they are not switching; (3) they present a low impedance to the clock line capacitance C_1 in both the ON and OFF state; and (4) they provide a 25%, 50%, 25% duty cycle for θ_1 , θ_2 , and θ_3 respectively. This last characteristic is advantageous for transversal filtering because when the θ_2 electrodes are tapped, the 50% duty cycle of the θ_2 clock gives a longer time to sense and sample the filter output.

F) WEIGHTING COEFFICIENT DESIGN

Another important design goal of this filter was to obtain a very narrow bandpass characteristic. In order to achieve this goal a large number of delay stages is required since the sharpness of passband to stopband transitions is inversely proportional to the length of the transversal filter. As a compromise between a very narrow response and a practical CCD size, a length of 800 delay stages was selected. A number of design techniques¹³ have been developed for determining the weighting coefficients of digital finite impulse response (FIR) linear phase filters. These digital filter design techni-

ques are directly applicable to CCD transversal filters. The weighting coefficients for the 800 stage bandpass filter were designed using a computer program¹⁴ which optimizes the weighting coefficients under the criteria of minimum sidelobe amplitude for a specified transition bandwidth from passband to stop band. This design algorithm results in equiripple sidelobes. The parameters used in our design resulted in a narrow bandpass filter with a center frequency at $f_c = f_o/4$. The width of the bandpass is $0.007 \times f_o$ at -3 dB and $0.017 \times f_o$ at -40 dB. The peaks of the sidelobes are uniform at -40 dB. Higher stopband attenuation could have been obtained at the expense of a broader bandpass.

The weighting coefficients are quantized in the photomasks due to the use of computer generated photomasks. In this CCD design, the weighting coefficients are coded into the channel stop level by placing a small region of $p+$ diffusion under the gap in the split electrode clock phase. With this technique, the weighting coefficients are defined with the resolution of the channel stop photomask and are therefore insensitive to small offsets in alignment of other photomask levels during the fabrication process. The expected resolution of the weighting coefficients is 0.3 to 0.6% of the maximum value. The filter with weighting coefficient quantization can be modeled as two filters in parallel one of which is the ideal filter and the other is an error filter having weighting coefficients equal to the difference between the quantized weighting coefficient values and the ideal values.⁵ Because the quantization errors are random, a good qualitative model of the spectral response of the error filter can be obtained by assuming a flat spectrum. The magnitude of the error filter frequency response has an expected rms value proportional to

$$\Delta H_{rms} = (\delta^2/12)^{1/2} \times N^{1/2} \quad (9)$$

where δ is the relative quantization increment of the weighting coefficients ($\Delta h/h_{max}$). The peak response of the ideal bandpass filter is proportional to

$$H_0 = \frac{1}{2\Delta f/f_c} \quad (10)$$

where $\Delta f/f_c$ is the ratio of the 3 dB bandwidth to the clock frequency. Combining (9) and (10) we obtain the relative contribution

of the error filter

$$\frac{\Delta H_{rms}}{H_0} = \frac{\delta}{\sqrt{3}} \left(\frac{\Delta f}{f_c} \right) N^{1/2}. \quad (11)$$

Evaluating (11) for the 800 stage bandpass filter with a weighting coefficient quantization of $\delta = 0.5\%$ yields an expected error response of -76 dB. Thus we do not expect to see the effects of weighting coefficient quantization in the transfer function of this filter.

III. EXPERIMENTAL RESULTS AND CONCLUSIONS

Preliminary evaluation of the performance of these devices is presented here. The frequency response of the filter is very close to the design as presented in Figures 9 and 10. The response curves shown in Figure 9(a) and 9(b) were obtained with clock frequencies of 100 kHz, where the bandpass center frequency is 25 kHz and the 3 dB bandwidth is 0.7% of the bandpass or 175 Hz. The highest sidelobe response is about -37 dB which is 3 dB higher than the design value of -40 dB. The small deviations in the sidelobe response from the design level is caused by a spurious feedthrough of the input signal to the output at a level about -55 dB below the bandpass peak response. The feedthrough response has a different phase relationship to different sidelobes, thus it adds constructively to some and destructively to others. The path of this feedthrough signal is being investigated. Similar performance is observed at a clock frequency of 1 MHz as shown in Figure 10. As expected the bandpass center frequency scales to 250 kHz and the bandwidth to 1.75 kHz. The highest sidelobes are -36 dB and as above the deviation from the ideal characteristics results from the spurious direct feedthrough of the input signal to the output.

The measured gain of the overall filter is approximately 0.56 (+5 dB insertion loss) at the bandpass center frequency. As described in Section II a gain of 1.4 (+3 dB) was expected for the ideal filter. Part of the attenuation can be accounted for by the effects of charge transfer inefficiency. Measurements indicate that these devices typically have charge transfer inefficiency ranging from $\epsilon = .00025$ to $\epsilon \approx .0003$. The effect of transfer inefficiency is to attenuate the frequency response by the factor⁶

$$A(f) = e^{-\frac{Ne}{2}} (1 - \cos 2\pi f/f_c) \quad (12)$$

which reduces the bandpass frequency by about 3 dB with the observed values of ϵ . Another 3 dB attenuation results from a measured capacitance ratio of $R = 3$ instead of the design value $R = 2.2$ used in (12).

The measured voltage gains of the differential voltage amplifier and the input voltage amplifier were each approximately $G = 9$ at both $f = 100$ kHz and $f_c = 1$ MHz. At a signal voltage level of 1 V_{rms} at the output of the input amplifier, the second and third harmonics were -40 and -50 dB respectively. Since the two amplifiers are constructed identically the same characteristics should apply to the output amplifier as well.

Detailed measurements are under way to determine the noise, linearity, frequency range, and power requirements of the entire filter. The preliminary results above indicate that performance consistent with design goals will be achieved.

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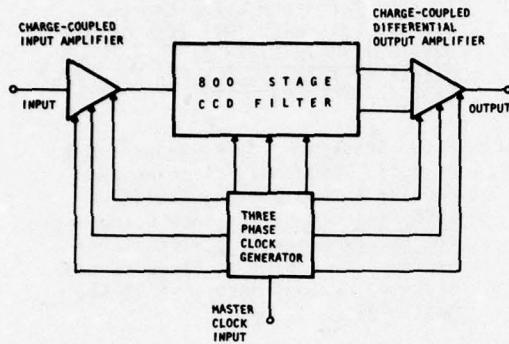


FIGURE 1. Block diagram of the 800 stage CCD transversal filter.

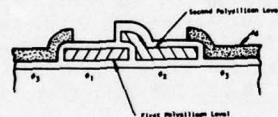


FIGURE 2. Electrode structure of the three metallization three phase CCD.

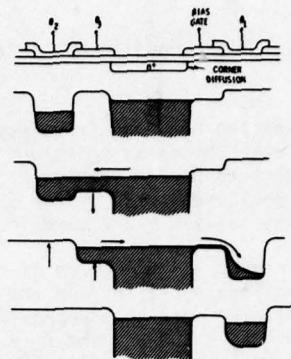


FIGURE 3. Schematic of the operation of the CCD corner showing the surface potential at various stages in transfer.

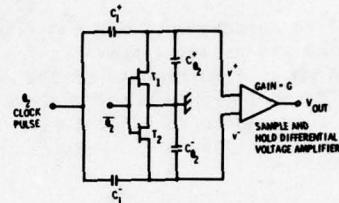


FIGURE 4. Schematic of the differential current integrator showing the clock line current integrating capacitors C_1^{\pm} .

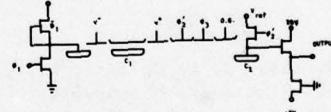


FIGURE 5. Schematic of the charge-coupled differential amplifier (CCDA). A large capacitor C_{IN} is used to transfer an amount of charge $C_{IN} (v^+ - v^-)$ to capacitor C_2 giving a gain $G = C_{IN}/C_2$.

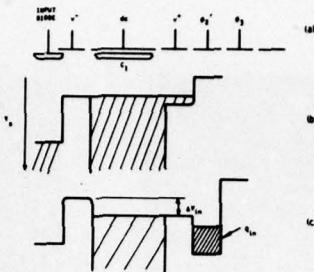


FIGURE 6. Potential energy diagram demonstrating the operation of the charge-coupled differential amplifier. An amount of charge $Q = C_{IN} (v^+ - v^-)$ is transferred into an output diode having capacitance C_2 , thereby resulting in an output voltage $V_{out} = C_{IN}/C_2 (v^+ - v^-)$.

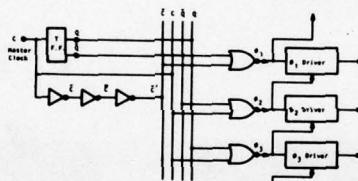


FIGURE 7. Timing and logic to generate three-phase clocks. Phase 2 has a 50% duty cycle while Phase 1 and Phase 3 each have a 25% duty cycle.

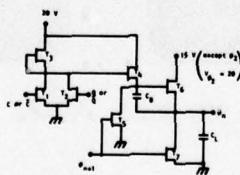


FIGURE 8. Clock Line Drivers

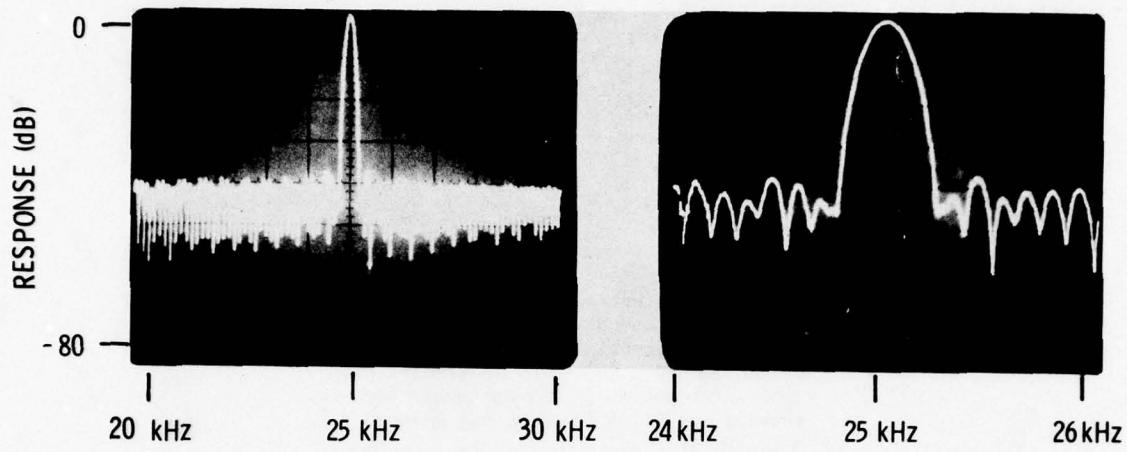


FIGURE 9. Frequency response of the 800 stage CCD filter operated at a clock frequency of 100 kHz.

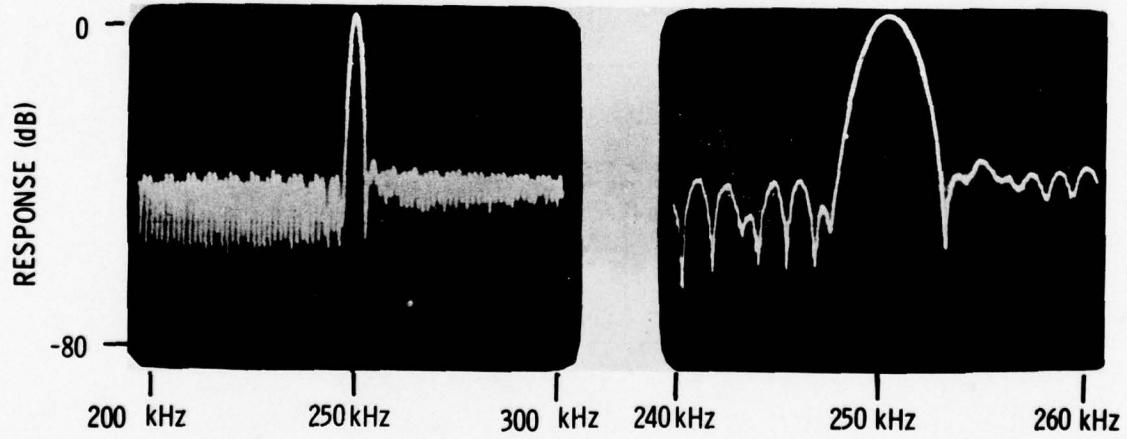


FIGURE 10. Frequency response of the 800 stage CCD filter operated at a clock frequency of 1 MHz.

A SWEEP DELAY CORRELATOR

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ABSTRACT Charge-transfer devices can be used as low-loss analogue delay lines of variable length extending up to many msec. This can be exploited to provide a very simple auto-correlator suitable for examining stationary signals. By controlling the clock frequency so that its period is swept linearly, a gradually increasing delay can be inserted into the signal path. The mean product of the delayed and undelayed signal represents the estimated auto-correlation (strictly the autocovariance) function of the signal and this can be obtained very simply using an analogue multiplier followed by a integrator with a time constant chosen to match the sweep rate of the delay.

INTRODUCTION

It is sometimes important to establish the decorrelation times of random or quasi-random signals, for instance radar echoes from sea waves. In other cases it may be required to detect and measure the period of repetitive components in a signal without foreknowledge of their shape and when they may be masked by other, perhaps larger, components. Problems of this type call for a knowledge of the auto-correlation properties of the signal s , expressed by the autocovariance function

$$\phi(\tau) = \int s(t) s(\tau+t) dt$$

which if normalised to make $\phi(0) = 1$, becomes the auto-correlation function (acf). In practice the integral is over a finite interval of time, t so that ϕ is statistically estimated only. τ specifies the time displacement or lag across which the signal correlation is measured.

When the signal statistics change slowly enough for stationarity to be assumed, sequential methods of estimating ϕ for different values of τ are applicable with consequent savings in hardware compared with systems which simultaneously measure ϕ for all time lags of interest. A simple real time implementation of this approach

is possible using charge transfer devices (CTD). Fig 1 shows how a CTD can be used to provide the time displacement τ and a four-quadrant analogue multiplier to derive the product

$$s(t) s(t+\tau)$$

which is integrated to form an estimate of ϕ using a simple time constant.

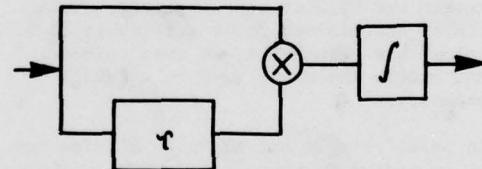


Fig 1 CTD Autocorrelator

DESIGN CONSTRAINTS

Some care is necessary in obtaining meaningful estimates of $\phi(\tau)$ for a fluctuation $s(t)$. The integrator time

constant T must be long enough for sufficient independent samples of the product $s(t) s(\tau+t)$ to be integrated to allow a given fractional accuracy f to be obtained. The sweep rate of the clock period P must also be low enough for the change $\Delta\phi$ due to the changing τ ($= NP$ for an N -sample delay) also to be kept smaller than $f\phi$.

If the variable sampling rate of the CCD is always kept below Nyquist, all the products integrated will be independent and the attainment of a fractional accuracy f requires approximately $1/f^2$ samples to be integrated so that

$$T = P/f^2 > 1/(2Bf^2)$$

fixes a lower bound for T where B is the bandwidth of s .

The sweep rate $\frac{dP}{dt}$ causes a change in ϕ over a time T of

$$\phi' N \frac{dP}{dt} T$$

where ϕ' represents the slope of $\phi(\tau)$. Keeping this error also down to the fraction f requires

$$\frac{dP}{dt} < \frac{f}{NT} / \left(\frac{\phi'}{\phi} \right)$$

which becomes important with the sharply peaked acf's exhibited by wideband signals. These arguments apply only if we do not exceed the Nyquist sampling rate. This limits the minimum delay attainable to $N/2B$. Below this value of τ , we must increase T and reduce the sweep rate to maintain accuracy.

In practice ϕ' is not known in advance and it is easier to experiment with the integration time constant and sweep rate to make sure that sensible measurements are being obtained.

EXPERIMENTAL RESULTS

The hardware equivalent of Fig 1 was realised as in Fig 2 using a pair of bucket brigade circuits connected in series to form the delay element. A total of 26 samples were stored at any time and a sample-hold circuit was used to derive a

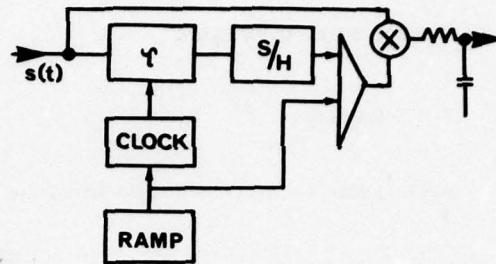


Fig 2 Compensated correlator

staircase output waveform, free of clocking transients. The two-phase clock was arranged to have a period increasing linearly with time by deriving it from two ramp functions, the faster of which is reset when it crosses the slower as indicated in Fig 3. The end points and sweep rate of the clock frequency are set by suitably choosing the slopes of the two voltage ramps. The bipolar bucket brigades,

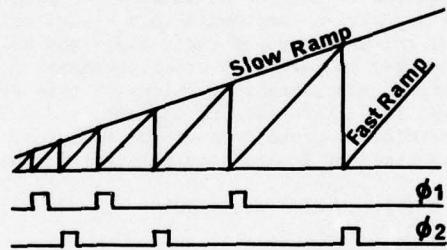


Fig 3 Linear clock period generator waveforms

normally used with MHz clock rates, were here required to store data for delays τ as long as 120 ms and under these circumstances the output showed a τ -dependent voltage offset which caused a significant error in the correlation output. This was approximately corrected by adding to the bucket brigade output a fraction of the slow ramp signal which determines the sweep rate of

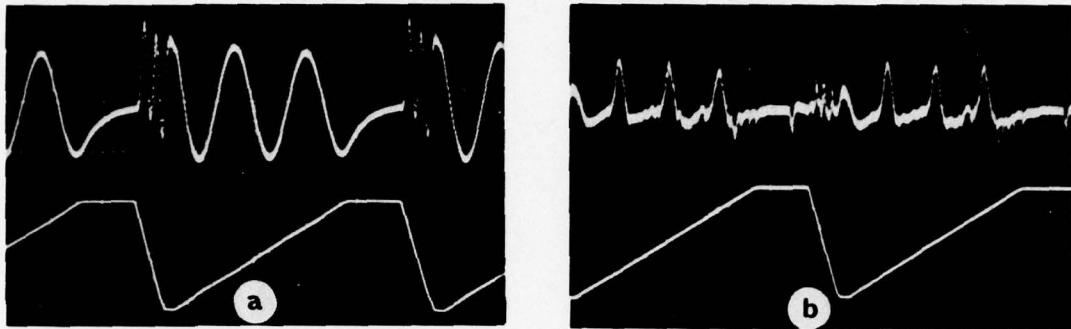


Fig 4 Correlator waveforms (2.5 s/div)

the clock period. Fig 4 shows some representative waveforms on simple test signals. In each case the integration time constant is 1s and the auto-correlation lag τ is swept from 6ms to 120 ms (with extreme clock frequencies of 4 kHz and 200 Hz) in a time of approximately 8 sec. 4(a) shows the approximately cosinusoidal acf obtained with a 20 Hz sine wave input. The lower trace shows the ramp controlling τ . During the ramp flyback the acf is retraced in reverse with poor accuracy because of the high sweep rate. Fig 4(b) illustrates the auto-correlation of a 30 Hz pulse waveform with 15% duty ratio. In both cases the measured acf is substantially correct, the chief distortion being due to the voltage offset error in the bucket brigade. Because this varies non-linearly with storage time it is difficult to remove completely. The effect is to contribute a proportion of the undelayed signal to the multiplier output.

In spite of this effect, the correlator is adequate for certain purposes even when time lags of the order 100ms are required.

CONCLUSION

A simple auto-correlator, which can readily be generalised to cross-correlate different signals by supplying the separate signals to the delayed and undelayed channels, can be built around a charge transfer device used as a variable delay line. Its chief restriction, apart from being applicable only to stationary signals, is the requirement that samples stored for times up to the longest lag to be measured are not appreciably attenuated or offset in voltage compared with those stored for the shortest lags.

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A TIME DOMAIN ANALYSIS OF VIDEO INTEGRATORS

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ABSTRACT. It has been shown that video integrators can be realised with charge coupled devices (CCD's). Such a realisation exploits the advantages of a CCD in that it is a sampled data device and combines analogue operation with the flexibility of digital techniques including the precise control of delay time. A video integrator serves to improve the signal-to-noise ratio of repetitive signals by integrating the signals in a recirculating delay line.

Unfortunately smearing or charge transfer inefficiency places a serious limitation on the performance of such integrators. The effect of smearing is to generate and feed the growth of secondary signals in the elements of the CCD following that containing the primary or wanted signal.

This paper presents a detailed analysis of the growth of secondary signals in CCD delay line integrators. Calculated values of the relative magnitudes of the primary and first two secondary signals are given as functions of the loop gain, transfer efficiency and number of transfers. On the basis of this analysis several techniques are proposed for reducing secondary growth whilst maintaining the required loop gain and hence the desired signal-to-noise ratio improvement.

1. THE VIDEO INTEGRATOR

If a simple recursive filter is operated at a frequency at which signal build up occurs, it can be considered as an integrator. Of particular importance is the processing of repetitive pulsed signals, as may be obtained in a radar system. If the time between pulses is equal to the delay time, τ , the recirculated and incident pulses will add. The similar growth of noise is slower because it adds in a root mean square manner so there is enhancement of the signal to noise ratio. The advantage of a CTD system is that the precise control of the delay time, inherent in the present digital techniques, is retained, but there is a simpler compatibility between pulsed signals and the sampled data, analogue operation of the CTD(1). It can be shown that charge transfer inefficiency modifies the transfer function of the recursive filter but in this system the steady state frequency domain representation of the filter is no longer useful, rather it is the growth of signals in time and the understanding of charge transfer inefficiency effects in the time domain that is of interest.

The effect of charge transfer inefficiency is to generate and feed the growth of secondary signals(2) in the elements of the CTD following that containing the primary or wanted signal so that an error is added to any signal contained in the next time cell. Once the secondary signal grows above the noise level in that element of the device, it effectively destroys some of the signal to noise ratio enhancement obtained through integration. The secondaries can be reduced by decreasing the loop gain but this in turn also reduces the possible signal to noise ratio improvement.

Consider the build up of signals in the time domain when the network of Fig. 1 is fed with a train of equal height pulses with a pulse repetition frequency equal to the inverse of the delay time. The

delay line has an impulse response given by

$$A + BZ + CZ^2 + \dots \quad (1)$$

where Z is a delay operator, $e^{-j\omega T_1}$ representing one stage of delay, T_1 in the CTD delay line (one stage contains p elements in a p phase CTD) and A, B, C etc. are amplitudes of the spurious signals.

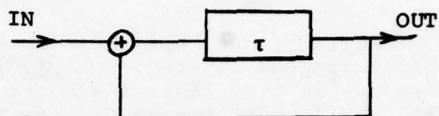


FIG. 1

A fraction, K , of the output from the first input pulse is then fed back to the input so that the input signal becomes

$$(1 + KA) + KBZ + KCZ^2 \dots$$

After m such circulations the primary signal builds up as

$$\begin{aligned} S_A = & A(1 + KA + (KA)^2 + (KA)^3 \\ & + \dots (KA)^{m-1}) \end{aligned} \quad (2)$$

the secondary and tertiary as

$$\begin{aligned} S_B = & B(1 + 2KA + 3(KA)^2 \\ & + \dots n(KA)^{m-1}) \end{aligned} \quad (3)$$

$$\begin{aligned} S_C = & C(1 + 2KA + 3(KA)^2 \\ & + \dots n(KA)^{m-1}) + \\ & KB^2(0+1 + 3KA + 6(KA)^2 \\ & + \dots \frac{m(m-1)}{2} (KA)^{m-2}) \end{aligned} \quad (4)$$

For positive values of K any one spurious output builds up faster than the ones leading it, although the magnitude is controlled by the factors A, B, C , because it feeds on all the leading outputs. In the

case of the primary and secondary for example, the primary builds up at a rate which is dependent on the fact that the increasing pulses are of unit amplitude, whilst the secondary build up depends on the amplitude of the primary which is continually growing to a value which is greater than unity.

The magnitudes of the signals after an infinite number of circulations can be written

$$S_A = \frac{A}{1-KA} \quad (5)$$

$$S_B = \frac{B}{(1-KA)^2} \quad (6)$$

$$S_C = \frac{C}{(1-KA)^2} + \frac{KB^2}{(1-KA)^3} \quad (7)$$

Equations 5 and 6 are similar in form to those derived by Urkowitz⁽³⁾ for secondary responses in conventional analogue delay line integrators.

An infinite number of circulations will be considered as these give the 'worst case' results.

2. CTD IMPULSE RESPONSE

In order to compare the relative magnitudes of the output signals it is necessary to determine the coefficients A, B, C. For a CTD delay line the impulse response can be written as (4)

$$\delta^n + z(ne\delta^n) + z^2 \left(\frac{n(n+1)}{2}\right) \epsilon^2 \delta^n \dots \\ z^j c_j^{j+n-1} \epsilon^j \delta^n \quad (8)$$

where $\delta = 1-\epsilon-\ell$, δ is the charge transferred at each stage, ϵ is the charge residual, ℓ is the charge loss per transfer, c_j^{j+n-1} is the binomial coefficient, and n is the number of transfers (elements or stages in a single phase device). The first three terms correspond to

the coefficients, A, B, C.

In order to simplify this equation assume that the device is operated at a clock frequency where the loss of charge can be neglected (i.e. $\delta = 1-\epsilon$, this then is strictly only true for a CCD).

To a good approximation

$$\delta^n = 1 - ne \quad (9)$$

provided that ne is small (< 0.1).

Assuming that $(n)(n+1) = n^2$, equations 5, 6, 7 may now be written as

$$S_A = \frac{1-ne}{1 - K(1-ne)} \quad (10)$$

$$S_B = \left[\frac{ne}{1 - K(1-ne)} \right] \cdot S_A \quad (11)$$

$$S_C = \left[-\frac{(ne)^2}{2(1 - K(1-ne))} + \frac{K(ne)^2(1-ne)}{[1 - K(1-ne)]^2} \right] \cdot S_A \quad (12)$$

The magnitudes of the output signals, $S_{A,B,C}$ are shown in Fig. 2 as functions of ne for given values of K . If the device was perfect ($ne=0$) then S_B , S_C would be zero and S_A reduces to $1/(1-K)$. Consider the curves for $K = 0.99$ in Fig. 2. For low values of ne , S_A approaches the ideal value and the amplitudes of the secondaries are low. As ne increases two effects can be observed. Firstly the secondaries build up to magnitudes close to that of the primary. The secondary-primary ratios approach unity. Secondly the magnitude of the primary becomes increasingly lower than the ideal value. With reference to equation 10 this can be attributed to an effective reduction in the loop gain. The gain has fallen from K to an effective value $K' = K(1-ne)$. These

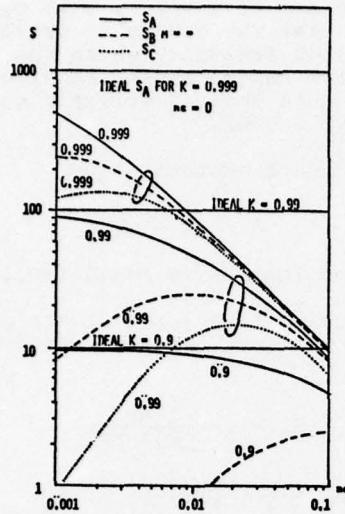


FIG. 2

The magnitudes of the primary S_A and the first two secondary signals S_B, S_C as a function of the loop gain K and the overall transfer efficiency for an infinite number of circulations.

effects are exaggerated as K approaches unity. For increasing K an even smaller n is required to maintain the same level of $(\frac{S_B, C}{S_A})$.

3. DESIGN CONSIDERATIONS

In practice to achieve a desired signal to noise ratio improvement, S_A has to grow to the required magnitude. The loop gain must be maintained. Equation 10 can then be rewritten in terms of K' . This is perhaps a more useful form of the equations for design purposes as it is K' that sets the performance of the integrator. The ratios $S_B, C/S_A$ are shown plotted in Fig. 3 as functions of the effective loop gain. Note that the ratios can now exceed unity because for a given K' and $n\epsilon$, K may be greater than unity.

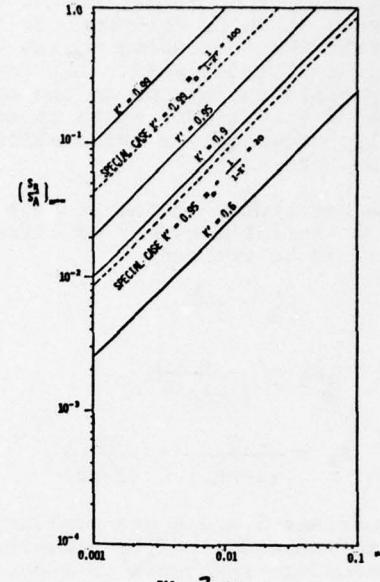


FIG. 3 (a)

The broken lines indicate the results for a finite number of circulations which give an integration time equal to the time constant of the integrator.

The results for $\frac{1}{1-K'}$ circulations (the filter time constant) are shown in Fig. 3 for comparison with the case of $m = \infty$.

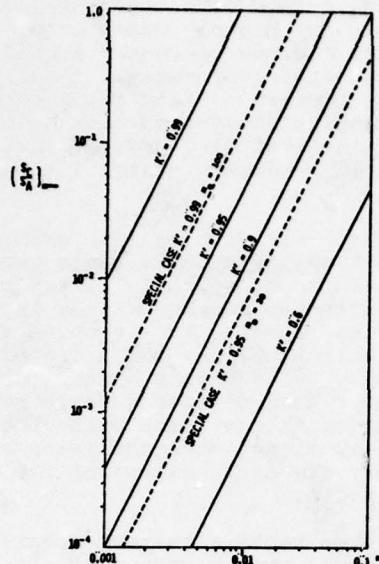


FIG. 3 (a)

4. TECHNIQUE FOR MINIMISING EFFECTS OF SECONDARIES

It is evident that for devices with poor transfer efficiencies or for devices with a large number of stages, the required value of K for a given improvement in signal to noise ratio may not be attained if S_B/S_A is to be kept sufficiently low, say below the built up noise level in that stage. In a practical situation some way has to be found of maintaining a low S_B/S_A ratio whilst keeping K as high as required.

CTD delay lines differ from conventional analogue delay lines in one important respect. They are sampled data devices, and hence adjacent signals are contained in adjacent elements of the CTD, precisely defined in time and synchronised to some clock waveform. Similarly the secondary and subse-

quent signals resulting from one primary are also precisely defined and can therefore be manipulated electronically.

Improvements may be obtained by sampling the input only once every two clock cycles so that an element containing the primary signal is always followed by an initially empty element. As integration proceeds, secondary signals will grow in the empty elements and tertiaries in following elements. As the output of the CTD, the primary is sampled and held, and added to the secondary to produce the output signal. In this way it is the growth of the tertiary that is the limiting factor rather than the secondary. As the tertiary can, for lower values of K and $n\epsilon$ be an order of magnitude smaller than the secondary this allows a significantly higher value of K to be used and hence a higher signal to noise ratio improvement.

Equations 10, 11, 12 and 13 give

$$\frac{S_C}{S_A} = \frac{n^2 \epsilon^2}{2(1-K')} \cdot \left(\frac{1+K'}{1-K'} \right) \quad (15)$$

and

$$\frac{S_B}{S_A} = \frac{n\epsilon}{(1-K')} \quad (16)$$

There is a decrease of spurious signals by a factor of $\frac{n\epsilon}{2} \cdot \left(\frac{1+K'}{1-K'} \right)$.

Little improvement occurs if the effective loop gain, K' , is large enough to be comparable with $(1-n\epsilon)$ but smaller loop gains give considerable improvement. For example

with $n\epsilon = 10^{-3}$ and $K' = 0.99 \frac{S_B}{S_A} = 10^{-1}$ for the simple system whereas a 10-fold improvement occurs in the modified system. No improvement occurs for $K' = 0.999$ but for $K = 0.9$ approximately 100 times improvement would occur.

The dependence of the spurious

signal suppression on loop gain can be removed if the secondary signal in the nominally empty element is returned to zero after each pass through the CCD. The improvement factor over the simple system will be discussed in the oral presentation.

A third but slightly more complicated modification of the simple integrator is illustrated in Fig. 4. The input pulses to the CTD are sampled, inverted, multiplied by a factor $\beta (< 1)$, held for one clock period and then added to the input. Assuming that the spurious signal smearing is a linear process the total signal output will be the sum of the two output signal trains shown in Fig. 4. Although the primary is unaffected, the smeared outputs will tend to cancel. Again the improvement factors will be discussed in the oral presentation.

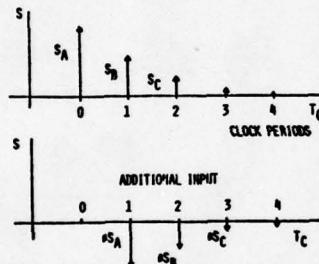


FIG. 4

Outputs after 2 circulations from the integrator resulting from (a) unit height pulse train (b) the unit height pulse train delayed by one clock period, inverted and multiplied by a factor β .

5. DISCUSSION

A detailed analysis of the build up of spurious signals in CTD integrators has been considered. Computed values of the relative magnitude of primary, secondary and tertiary outputs from the integrator have been presented as functions of K , the loop gain, and $n\epsilon$, the over-

all transfer inefficiency of the CTD.

The growth of secondaries is more severe for higher values of K . As higher K gives increased signal to noise ratio improvement, the limitation imposed on K by the necessity of keeping the secondaries below a certain level also reduces the possible improvement in signal to noise ratio.

The limitation on loop gain will be set by the dynamic range required for the input signal. If the smallest detectable signal after integration is equal to the noise voltage at the output, the ratio of primary and spurious signals must be greater than desired dynamic range in order that a large preceding primary signal does not leave a secondary signal in excess of the output noise.

Three techniques were suggested for reducing the effect of secondaries and hence permitting a higher loop gain to be used for a given value of $n\epsilon$. The first technique, basically the addition of the primary and secondary signals to give the output signal, is simple and effective for lower K and $n\epsilon$ values. It also has the advantage of improving the signal to noise ratio even if K is not increased.

The second technique reduced the spurious signals by periodically removing the secondaries while the third technique continuously cancelled the secondaries. The improvement in both is equally effective at all values of loop gain and particularly so at low $n\epsilon$. The second technique is 4 times less effective at reducing smeared signals than the more involved third one. The third technique involves some loss in signal to noise ratio improvement which reduces that gained from the increase in K that it makes possible.

In the analyses discussed, the signal transfer processes within the CTD have been assumed linear with signal amplitude. Normally this is

a good approximation, but in this case signal amplitude may vary over several orders of magnitude, from that of the built up primary to the noise level. Consequently it may no longer be justified to use the linear approximation for very high gain systems. In practice the performance of CCD video integrators was found to be limited by non-linearities associated with the input to the device. These prevented very accurate measurements of secondary growth from being made and also restricted the operation of the integrator to low loop gains where the growth is small.

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THE MEASUREMENT OF NOISE IN BURIED CHANNEL CHARGE COUPLED DEVICES*

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ABSTRACT. The noise in buried channel charge coupled devices was measured and was found to be composed of noise from four sources, output amplifier noise, dark current noise, electrical input noise and bulk state trapping noise. Because of the low levels of noise achieved in the output amplifier and in the electrical input of signal it was possible to make direct measurements of the dependence of bulk state trapping noise on input signal, clock rate and spectral frequency. The measured results for all the noise sources were found to be in satisfactory agreement with theoretical expectations.

I. INTRODUCTION

In this paper an investigation is made of the noise sources which limit the dynamic range of a buried channel charge coupled device (CCD) linear shift register. There were four sources of noise which were observed; output amplifier noise, dark current noise, electrical input noise and bulk state trapping noise. The noise level of each of these sources was found to be in reasonable agreement with the theoretical expectations.

A procedure was developed and will be presented in Section V which made it possible to separate the relative contributions of each of the above four components of noise. However, in order to perform this separation, an output amplifier was needed which had a very low noise level. It was found that satisfactory noise levels could be obtained by the use of correlated double sampling¹ (CDS) if very careful optimization of band limiting and pulse timing was employed. A noise analysis will be given in Section VI which identifies the tradeoffs involved in this optimization. Using the results of this analysis it was possible to obtain noise levels of less than 30 e⁻ (rms noise electrons).

In Section VII the dark current noise as expected was found to be well characterized by shot noise and for our devices

at a 500 kHz clock rate, a typical value of noise due to dark current was 20 e⁻.

A low noise design of the "fill and spill" type input was used which will be described in Section VIII.^{2,3,4} This input structure made it possible to electrically inject very low noise signals. The dependence of this noise on signal size was found to be in satisfactory agreement with a simple phenomenological theory.

Because of the low noise levels which were obtained for the previous three noise sources, it was possible to make extensive direct measurements of the noise due to bulk state trapping, the level of which ranged from less than 10 to greater than 100 noise electrons. In Section IX measurements of the spectral density of bulk state trapping noise will be presented as well as its dependence on input signal and clock rate.⁵ The most abundant bulk trap was identified as being introduced by gold impurities which had a density on the order of 10¹¹ cm⁻³.

In Sections II-V general information is given about the test device, measurement procedures and data presentation. In particular, in Section II a description of the device will be given as well as some of its performance characteristics. In Section III a few definitions will be

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presented and in Section IV the test instrumentation will be described.

In Section V a summary is given of the characteristics of the four observed noise sources, which are described in detail in Sections VI-IX.

II. TEST DEVICE CHARACTERISTICS

A portion of the 150 stage linear shift register which was used exclusively in these noise measurements is shown in Figure 1. It makes use of overlapping gate, four phase clocks (600 charge transfers) with an electrode size of $7.5 \mu\text{m} \times 125 \mu\text{m}$. The metallization masks were compatible with both $\text{Al-Al}_2\text{O}_3-\text{Al}$ ⁶ and poly-silicon-aluminum double level metal systems.⁷ Both of these metallization methods were used in fabrication without noticeable effect on device operation. The thermally grown oxide under the metal gates was typically 1300 Å thick and it was grown on $\langle 100 \rangle$ oriented, p-type substrates with a typical resistivity of about $30 \mu\text{-cm}$. The n-type layer in the active CCD area which when depleted forms the buried channel⁸ was introduced by ion implantation followed by a short drive-in diffusion. The ion implantation dose was typically $1.5 \times 10^{12} \text{ cm}^{-2}$ of phosphorus ions and the resulting depth after diffusion of the buried channel ranged in depth from 2000-3000 Å from the SiO_2 -Si interface.

The CCDs were selected so that only those devices which exhibited low transfer inefficiency and dark current were used in the measurements. The transfer inefficiency was less than 1×10^{-5} (fraction of the signal packet lost each transfer) in the best devices but was more typically on the order of 2×10^{-5} . The dark current ranged from 3-8 nA/cm^2 and the devices were also checked to eliminate those which exhibited points of localized avalanching (spikes). Measurements were made using gate controlled diodes on the same I.C., to separate the bulk and surface contributions to the dark current and in this way bulk lifetimes of $200 \mu\text{s}$ were determined with surface recombination velocities of less than 5 cm/sec .

An important characteristic in determining the performance of a buried channel device is the distribution of the signal charge in the buried channel.⁹ This distribution is controlled by the profile of the n-type buried channel layer and for use

in later sections the calculated distribution of signal charge is shown in Figure 2 for the impurity profile, $N_{IM}(X)$, (shown as the dashed line in Figure 2) given by

$$N_{IM}(X) = \frac{2 N_{DOSE}}{\sqrt{\pi} X_g} e^{-\left(\frac{X}{X_g}\right)^2} - N_A \quad (1)$$

where $X_g = .2\mu$, $N_A = 5 \times 10^{14} \text{ cm}^{-3}$ and $N_{DOSE} = 1.0 \times 10^{12} \text{ cm}^{-2}$. In this figure a one dimensional plot of the charge distribution is shown in the direction from the Si-SiO₂ interface ($X = 0$) into the silicon. The charge is shown in Figure 2 to be located in a layer which extends from $.11 \mu\text{m}$ to $.16 \mu\text{m}$ for a signal charge of $7.3 \times 10^9 \text{ e}/\text{cm}^2$. This layer is observed to increase in width and move closer to the surface as the quantity of signal charge is increased. This property of the signal charge in buried channel devices will be found to significantly affect their noise characteristics.

III. DEFINITIONS AND NOTATION

Throughout this paper the measured rms noise voltage levels will always be presented as the number of rms noise electrons referred to the charge packet in the CCD channel.

In order to simplify comparisons between the spectral density and rms voltage measurements and to facilitate comparison of measurements at different clock rates, the units which will be used in the spectral density measurements will be the "equivalent" number of rms noise electrons, $n(f)$, which is defined by

$$n^2(f) = \frac{1}{R^2} \frac{V_{WA}^2}{B} \frac{1}{G^2(f)} \left(\frac{f}{2}\right) \quad (2)$$

in which R (volts/electron) is the responsibility of the entire output circuit which includes source follower, CDS circuit and high gain amplifier, $V_{WA}(f)$ is the wave analyzer reading over a bandwidth, B , which is centered at a frequency f . The function $G(f)$ characterizes the sample and hold output waveform and for a sample pulse which is much shorter than the clock period, $G(f)$ is given by

$$G(f) = \frac{\sin(\pi f T_c)}{\pi f T_c} \quad (3)$$

To calculate the actual number of rms noise electrons, n , from the wave analyzer reading the following expression should be used:¹⁰

$$n^2 = \frac{1}{R^2} \int_0^{f_c/2} \frac{V_{WA}^2(f)}{B} \frac{1}{G^2(f)} df \quad (4)$$

Therefore, $n(f)$ is equal to n when the spectrum is white (independent of frequency) but for a general non-white spectrums (e.g., the noise from bulk state trapping), n and $n(f)$ are related by

$$n^2 = \frac{2}{f_c} \int_0^{f_c/2} n^2(f) df \quad (5)$$

The notation which will be used is that actual rms noise electron values (Eq. 4) will be denoted by n_i in which the subscript, i , will denote the particular noise source. To denote the spectral density as the equivalent number of rms noise electrons (Eq. 2) the argument, f , is added, $n_i(f)$, which identifies the frequency at which the spectral density is being evaluated.

In order to provide a noise source "standard" to check the accuracy of the overall measurement setup an optical input was introduced by a simple light bulb placed in a light tight box over the CCD (as shown in Figure 3). By monitoring the average current out of the device using the ammeter in the drain of T_1 , it is possible to calculate the number of optically introduced electrons, N_{opt} from which can be calculated the expected shot noise level of $(N_{opt})^{1/2}$. This calibration procedure gave confidence that the noise measurement accuracy was within $\pm 10\%$.

IV. TEST INSTRUMENTATION

The test setup used for the noise measurements is shown in Figure 3. A standard floating diffusion output was used (which will be discussed later) which is composed of the on-chip MOSFETs T_1 and T_2 . In the drain of the reset transistor T_1 an ammeter is shown which is used to determine the responsivity, R (volts/electron), of the CCD output by measuring the change in current corresponding to a change in the output voltage. The output of the CCD I.C. at point B is then processed using a circuit which implements correlated double sampling (CDS)¹¹. The CDS circuit performs two functions; first, it removes the noise

introduced by the preset of node A by T_1 , and it also converts the output into a sample and hold format which can be amplified without saturating a high gain amplifier. The amplifier which was used had a gain of 200, and an equivalent input spot noise level of $3 \text{ nv}/\text{Hz}^{1/2}$. The output of this amplifier was then fed into either a wave analyzer (HP 310A) which has a 3000 Hz bandwidth for spectral density measurements or into a multi-channel analyzer (MCA) for rms voltage measurements. The MCA was operated in the mode which provides a visual display and storage of the amplitude distribution of the noise which is Gaussian for all the CCD noise sources (as expected for most physical noise sources). An advantage of this approach for rms voltage measurements is that spurious non-Gaussian signals (e.g., 60 Hz) can be easily identified and then eliminated.

V. NOISE SOURCES

As discussed in the introduction, an important purpose of this investigation was to determine whether the theoretical understanding of the CCD noise sources is consistent with experimental evidence. The four types of noise which were observed were due to; 1) Output amplifier, 2) Dark current, 3) Electrical input and 4) Bulk state trapping.

A brief description will now be given of each of the above contributions along with a procedure which makes it possible to investigate individually the noise from each of the four sources.

1) OUTPUT AMPLIFIER

Output amplifier noise will be described in Section V and will be defined as the noise generated after the last CCD transfer has taken place. In the experimental setup shown in Figure 3 the largest contribution to the noise of the output amplifier was generated by the thermal or Johnson-Nyquist noise in the source follower, T_2 . A small amount of additional noise was generated in the CDS circuit following T_2 . The output amplifier noise could be separated from the other three noise sources by simply reversing the direction of the CCD clocks. All dark current (thermally generated minority carriers) will then be clocked out the input diode (which is biased with a high D.C. voltage) so that any noise measured at the wave analyzer (or MCA) is due only to the output circuits.

2) DARK CURRENT

Dark current noise will be briefly discussed in Section VII and is due to the thermal generation of electrons at the $\text{SiO}_2\text{-Si}$ interface and in the bulk material.¹⁸ Since this generation is totally random, the collection of these carriers into the buried channel results in full shot noise on the number of generated electrons.¹¹ This is a white noise source, the amplitude of which can be determined by measuring the noise while the device is being clocked forward without electrical input of charge and then subtracting the output amplifier noise which was measured when the device was being clocked in reverse. As usual in subtracting (or adding) noise voltage, the subtraction (or addition) is in quadrature, i.e., the measured noise voltages must be converted to power (voltage squared) before the two noise levels are subtracted (or added).

3) THE ELECTRICAL INPUT NOISE

The electrical input noise was measured on a "fill and spill" type input (see Section VIII) which was especially designed for low noise operation. The separation of this noise from the output amplifier and dark current contributions can be performed by simply subtracting out in quadrature the noise measured without any introduced signal. The separation of input noise from the bulk state trapping contribution is somewhat more difficult in that it is necessary to make use of their characteristic spectral distributions. This is possible because the correlated nature of bulk state trapping noise¹² results in a suppression of the noise at low spectral frequencies so that the noise measured at these frequencies is due only to the spectrally flat input noise.

4) BULK STATE TRAPPING NOISE

Bulk state trapping noise was found to account for all the remaining noise after the noise due to the above three sources were subtracted out in quadrature from the measured readings. It is easily identifiable because of the above mentioned spectral density frequency distribution resulting from the correlated aspect of this noise.¹² This noise source also has a relatively strong dependence on clock rate and input signal⁶ and in Section IX measurements will be presented which will explore these dependences.

VI. OUTPUT AMPLIFIER NOISE

A critical aspect of noise measurements (and operation in general) of CCDs is the performance of the charge detection circuitry. The method used in these measurements was correlated double sampling (CDS) which was developed by M. White, et. al,¹ for low light level image arrays. This technique not only has the capability if properly implemented to achieve very low noise levels but has the additional advantages of being linear, stable and that implementation can be easily performed off chip (or on-chip) with only a few MOSFETS. Also, the final output is in a sample and hold format which is important for noise measurements because it minimizes signal power at the clock rate and therefore allows high gain amplification.

In spite of the apparent simplicity of this technique it was found that only by careful optimization of the timing of the sampling pulses as well as introduction of appropriate filtering was it possible to achieve noise levels below 30 noise electrons. In order to understand the trade-offs involved in this optimization a large part of this section will be devoted to a noise analysis of this output. Also the contributions of the various noise sources in the circuit which was implemented will be discussed. First, however, a brief review will be given of the operation of CDS, as well as discussion of the circuits used for the implementation.

IMPLEMENTATION OF CORRELATED DOUBLE SAMPLING

Figure 4 is a schematic representation of the circuit which was used to implement CDS. The portion of this circuitry which was on the CCD I.C. (on chip) is composed of two MOSFETS, T_1 and T_2 . The purpose of transistor T_1 (shown as a switch) is to preset the output capacitance, C_o , (the capacitance of node A) to a voltage sufficiently high to deplete the buried channel. The signal packet is then transferred onto this capacitance and discharges it towards ground. The resultant change in voltage is sensed by the source follower amplifier T_2 and is brought off the chip at point B. The voltage waveform which is observed at point B is shown in Figure 5. The preset takes place in the time interval from t_0 to t_1 and the signal transfers onto node A at time t_2 . It is well known that because of the thermal noise in the channel of T_1

there is a noise due to the preset operation given by^{1,11}

$$n_1 = \frac{1}{q} (kTC_o)^{\frac{1}{2}} = 400e^- C_o (\text{pf})^{\frac{1}{2}} \quad (6)$$

The output capacitance of the device used in these measurements was $C_o = .25 \text{ pf}$ which would yield the unacceptably high noise level of $200 e^-$ if the output were taken at this point without further processing.

The CDS technique provides an approach for removal of this preset noise.¹ As discussed by White, et. al.¹, when the preset switch is opened node A has a time constant given by $R_{\text{off}} C_o$ where R_{off} is the resistance to A.C. ground of node A when transistor T_1 is off and is typically $> 10^{10} \Omega$. The preset noise, n_1 will therefore be correlated between any two samples which are taken after the preset at t_1 . A discussion of this correlation is given in Appendix A. Therefore if the output is taken to be the difference in voltage of the samples at times t_2 and t_4 (shown in Figure 5) subject to the constraints $t_1 < t_2 < t_3 < t_4 < t_5$, the preset noise will approximately cancel and only the change in voltage due to the transfer of the signal charge will be observed. If the time between the two samples (t_4-t_2) is too long compared to the time constant $R_{\text{off}} C_o$ then the correlation of the noise is decreased and the noise level, n_A , will be measured³ (see Appendix A)

$$n_A = n_1 \left[2(1 - e^{-\frac{-(t_4 - t_2)}{R_{\text{off}} C_o}}) \right]^{\frac{1}{2}} \quad (7)$$

where n_1 which is given by Equation 6 is the preset noise without CDS. The effective value of R_{off} which was observed was on the order of $10^8 \Omega$ which required the interval t_4-t_2 to be less than $5 \mu\text{sec}$ for suppression of the preset noise. The reason for this low value of R_{off} is thought to be due to surface leakage. Therefore, if very low frequency operation is desired then care should be taken to reduce this leakage.

If the interval t_4-t_2 is much greater than $R_{\text{off}} C_o$ the preset noise will actually be increased by the use of CDS.³ This increase occurs because the noise voltage sampled at the times t_2 and t_4 are then totally uncorrelated and when the difference

in voltage is taken between these two samples the noise, n_1 , from each sample adds in quadrature and yields a resultant noise level of $\sqrt{2} n_1$ which can be seen from Eq. 7.

The circuit which was used to take the difference in the two samples is shown in Figure 4. The signal was capacitively coupled at point B by capacitor C_c and the clamped to a D.C. voltage at time t_2 . The voltage difference was sampled and held on capacitor C_{SH} by briefly closing MOSFET switch T_5 at time t_4 . The buffer amplifiers T_4 and T_6 were both MOSFET source follower circuits.

NOISE OF CLAMP AND SAMPLE CIRCUITS

In this and the following sections expressions will be obtained and evaluated for the various noise sources which contribute to the total output noise and they will be evaluated and compared with the measured results.

The clamping of capacitor C_c and the sampling by T_5 which sets C_{SH} are subject to the same considerations applied to the preset of node A (Eq. 6) with respect to the uncertainty of voltage on capacitors C_c and C_{SH} except there is no suppression by the double sampling. Therefore, the equivalent number of rms noise electrons referred to the CCD channel, n_D , resulting from the clamping operation at time t_2 is given by,

$$n_D = \frac{1}{q} \frac{C_o}{A_2} \frac{(kT)}{C_c} \approx \frac{400 e^-}{A_2} C_o (\text{pf}) C_c (\text{pf})^{\frac{1}{2}} \quad (8)$$

in which A_2 is the gain of MOSFET amplifier T_2 . A similar expression can be obtained for noise due to the sample and hold,

$$n_E = \frac{1}{q} \frac{C_o}{A_2 A_4} \frac{(kT)}{C_{\text{SH}}}^{\frac{1}{2}} \approx \frac{400 e^-}{A_2 A_4} C_o (\text{pf}) C_{\text{SH}} (\text{pf})^{\frac{1}{2}} \quad (9)$$

in which A_4 is the gain of amplifier T_4 .

Choosing suitably large values of C_c and C_{SH} will result in a negligible contribution of noise from the clamp and sample operations. For the circuit which was actually implemented the calculated noise levels from these sources are $n_D = 7 e^-$ and $n_E = 9 e^-$.

The noise contributed by the buffer source follower amplifiers T₄ and T₆ can also be made acceptably small by proper choice of components. In the realization used in these measurements standard n-channel MOSFETs were used which had a low white noise (thermal noise) component but unfortunately had a rather high 1/f noise which was characterized by a corner frequency near 100 kHz. An increase in the output noise at low frequencies was observed due to this excess noise but it was not sufficiently large to significantly degrade the subsequent measurements of other noise sources.

1/f NOISE OF SOURCE FOLLOWER, T₂

The rms noise contributed by the amplifiers T₄ and T₆ is unaffected by the CDS operation, however, the noise generated by amplifier T₂ is substantially modified because the noise is generated before the CDS circuit. One effect on the noise of T₂ which was pointed out by White, et.al.¹ is that noise at frequencies that are much less than $(t_4-t_2)^{-1}$ is substantially suppressed. This characteristic of CDS is especially effective in suppressing the 1/f noise of T₂ as long as the 1/f corner frequency of T₂ is sufficiently low. If on the other hand the 1/f noise corner is significantly greater than $(t_4-t_2)^{-1}$ then excess noise will be measured at the output. Since 1/f noise in MOSFETs is believed to be due to trapping in surface states, substantial reduction in 1/f noise can be obtained if these transistors are operated in a buried channel mode (i.e., the signal is away from the Si-SiO₂ interface). In Figure 6 the spectral density of the noise for several surface and buried channel transistors shows the improvement obtained with the buried channel devices. To fabricate a buried channel transistor it is only necessary to implant the MOSFET with the same dose which was used to make the buried channel CCDs and to then operate at sufficiently low current levels to keep the channel buried. These devices have a 1/f corner around 50 kHz which is seen to be well over an order of magnitude lower than the surface channel device which are identical to the buried channel devices in all respects except they did not receive the implant.

For reasons which will be discussed below, the time interval $(t_4-t_2)^{-1}$ should be set to $2 f_c$, so that for clock rates greater than 25 kHz substantial suppression

of the 1/f noise will occur for a buried channel MOSFET, while a large amount of excess noise will be introduced at the lower clock rates if a surface channel MOSFET were used.

THERMAL NOISE OF SOURCE FOLLOWER, T₂

Besides suppressing the 1/f noise of transistor T₂, the CDS circuit also affects the white (thermal) noise component generated by this device. In Figure 7 the level of this noise is typically seen to be approximately 9 nV/Hz^{1/2}. Unfortunately the effect of CDS is to increase the contribution from this source instead of suppressing it. In fact it will be shown that this noise component is the dominant source of noise in the entire output amplifier. The optimization of timing and band limiting which was referred to in the introduction, which will now be discussed, is an attempt to decrease the contribution of noise from this one source.

The purpose of the single pole low pass filter with time constant R₁C₁ which follows T₂ in Figure 4 is to band limit the thermal noise of transistor T₂ and thus to reduce its contribution to the rms noise. The effect of this bandlimiting is to introduce correlation of this noise between the two samples at t₂ and t₄. Taking this correlation into account the resultant rms noise after band limiting and double sampling is given by (see Appendix A),

$$n_B = \frac{C_0 V_{T2}}{qA_2} \left(\frac{1}{4R_1C_1} \right)^{\frac{1}{2}} \left[2(1 - e^{-\frac{(t_4-t_2)}{R_1C_1}}) \right]^{\frac{1}{2}} \quad (10)$$

in which V_{T2} is given by¹⁸

$$V_{T2} = A_2 \left[4kT \left(\frac{3}{2} g_m + \frac{1}{R_L} \right)^{-1} \right]^{\frac{1}{2}} \quad (11)$$

where $A_2 = g_m R_L / (1 + g_m R_L)$, R_L is the load resistor of the source follower and g_m is the transconductance of the MOSFET T₂. From Eq. 10 it can be seen that either decreasing the bandwidth of the R₁C₁ filter (increasing the band limiting of the wide band noise V_{T2}) or decreasing the ratio (t_4-t_2/R_1C_1) , (increasing the correlation between the two samples), will result in a decreased noise level. Therefore, it would appear desirable to increase R₁C₁ while

decreasing the time between the clamp and sample pulses. However, as the time constant $R_1 C_1$ of the filter is increased the voltage swing which represents the signal is attenuated by the factor, $[1 - e^{-(t_4 - t_3)/R_1 C_1}]$.

To maximize this factor the largest possible amount of time should be given for the signal transient to occur. Therefore, the sample at t_4 should occur just before the following preset occurs at t_5 (see Figure 5).

Another consideration which also limits the maximum size of $R_1 C_1$ is that a fraction $e^{-(t_2 - t_1)/RC}$ of the preset noise, n_A , will remain after the clamp has occurred because of the correlation effects introduced by the bandlimiting.¹⁴ This fraction can be decreased by minimizing the width of the preset pulse ($t_1 \approx t_0$) and by clamping (i.e., the sample at t_2) just before the signal is transferred at t_3 . Therefore, the tradeoff involved in choosing the bandwidth of the low pass filter; $R_1 C_1$, is that the wide band noise of T_2 should be band-limited to as low a frequency as possible which implies a long time constant; however, this long time constant attenuates the signal swing as well as decreases the preset noise suppression.

A suitable compromise of the above considerations is to allow three to four time constants ($R_1 C_1$) between the preset and clamp pulses as well as between signal transfer and the sample pulse. The optimum timing subject to this constraint is given by

$$t_1 - t_0 \ll T_c \quad (12)$$

$$t_2 - t_0 \approx t_3 - t_0 \approx \frac{T_c}{2} \quad (13)$$

$$t_4 - t_0 \approx T_c \quad (14)$$

and to obtain four time constants for the above mentioned intervals the low pass filter should have a bandwidth, $f_{3dB} = 1/2\pi R_1 C_1$, given by

$$f_{3dB} \approx \frac{4}{3} f_c \quad (15)$$

From Equation 14 it is found that with this band limiting and timing sequence that the effect of CDS on the noise, $\sqrt{T_2}$, (Eq. 11) generated in T_2 is to increase the rms level by a factor of $\sqrt{2}$ over the noise level which would be obtained without CDS. This increase

in noise is due to the lack of correlation which exists between the clamp and sample pulse because the band limiting (which has been optimized taking this effect into account) is too wide to provide correlation between the two samples. The effect is similar to that discussed in Section VI in which the preset noise could also be increased by a factor of $\sqrt{2}$.

Evaluating Eq. 10 for the rms noise due to the thermal noise of T_2 at a clock rate of 500 kHz, including processing by the CDS circuit (with timing and bandlimiting given in Eqs. 11-14) yields a rms noise level of $n_B = 21 e^-$, which as pointed out previously is the largest noise source in the output amplifier.

OUTPUT AMPLIFIER NOISE MEASUREMENTS

Evaluating Eqs. 8, 9 and 10 and summing the results (in quadrature) results in a total expected output amplifier noise level of $25 e^-$. In the lower curve in Figure 7 the measured output amplifier noise is shown for a CCD which is being clocked in reverse so that all dark current will be clocked out the input which isolates the noise due to the output circuit. The measured value of $27 e^-$ agrees very well with the expected value. At low frequencies the noise is seen to increase and this is due to 1/f noise of the off chip MOSFETs T_4 and T_6 as discussed earlier in this section. The simplest method to decrease the noise level of the output amplifier is to decrease the capacitance, C_o , of the output node. This procedure linearly increases the responsivity of the output without increasing the noise voltage of any of the sources which have been considered. Since the noise is referred to the CCD channel the equivalent number of noise electrons, therefore, decreases linearly with this capacitance. It is expected an overall noise level of $10 e^-$ could be achieved with a design of the output node which minimizes C_o .

VII. DARK CURRENT NOISE

In the last section the noise which was analyzed was the observed noise when the device was clocked in reverse. In this section will be discussed the origin of the additional noise which is measured when the device is clocked normally. There is, however, not yet any intentionally introduced signal charge.

Since a CCD (buried or surface channel) is operated in deep depletion there exists a thermal generation of carriers which is attempting to re-establish an equilibrium condition.⁵ The electrons generated in this way are collected in the buried channel along with the signal charge. The variation in the amount of electrons generated and subsequently collected is characterized by shot noise, i.e., the number of rms noise electrons is the square root of the mean value of the collected electrons. For a dark current level of J_D (amp/cm²) the number of rms noise electrons, n_{J_D} is given by

$$n_{J_D} = \left(\frac{J_D A_S M}{q f_c} \right)^{\frac{1}{2}} \quad (16)$$

where A_S is the area of single stage (four gates for a four phase device) and M is the number of stages.

In the upper curve of Figure 7 the measured noise is shown for a device which is clocked normally but the input is biased so that there is no electrical introduction of signal charge. The increase in noise from the lower curve which is being clocked in reverse is due to dark current. If these two curves are subtracted in quadrature a noise level of 21 e^- is determined which is due to dark current and is in good agreement with the value obtained from Eq. 16.

In general the dark current was found to be characterized by shot noise as was the case for the device in Figure 7, however, for devices in which localized avalanching was occurring (spikes) the noise was sometimes in excess of shot noise.

VIII. INPUT NOISE

In sections VI and VII the noise was determined for a CCD which is operated without intentionally introduced signal charge. This section and the next on bulk trapping noise will investigate those noise sources which are only present when there is signal charge being introduced. In order to separate the two components of this noise it is necessary to make use of their characteristic spectral distributions. In Figure 8 the measured spectral density for device A in units of equivalent rms

electrons squared (noise power) is plotted for the signal dependent noise.

This noise can be separated into a white noise component which is due to the electrical input of the signal charge and a part which has a $(1 - \cos 2\pi f/f_c)$ frequency dependence. This is the dependence to be expected for bulk state trapping¹² and will be investigated further in Section IX. From Figure 7 it is obvious that in order to separate out the input noise contribution it is only necessary to measure the spectral density at low frequency, where the trapping noise is suppressed. All the measurements presented in this section were made using this technique.

The method of introducing the input signal which was used was based on a low noise scheme which was developed independently at Bell Labs,³ Texas Instruments,² and RCA.⁴ This approach which will be called the "fill and spill" method involves application of the signal to an input gate (see Figure 9). The diode voltage is initially set so that there is no charge introduction into the channel. The input diode is then pulsed so that a full well of charge is introduced into the first CCD well. The diode voltage is then restored to its initial level and the capacitance associated with the receiving well is then discharged to a voltage level set by the signal on the input gate. At the termination of this process, charge stored in the pinched-off transfer channel, under the input gate is minimal, and uncertainties associated with its removal path are small. The amount of charge introduced is the difference between the input and the clock voltages times the capacitance of the receiving well, C_{in} . Analyses predict that the number of rms noise electrons, n_{in} which are introduced into the signal packet using this input technique is given by

$$n_{in} = \frac{1}{q} (\alpha k T C_{in})^{\frac{1}{2}}, \quad (17)$$

in which α is on the order of one¹⁸. In order to reduce the input noise it is only necessary to reduce the size of the input capacitance, C_{in} . This was done by constricting the channel stop under the first θ_1 well so that the channel width was only $12 \mu\text{m}$ wide as shown in Figure 10. Since the operation of a buried channel

transistor in the regime near cutoff not well understood, α will be treated as a parameter and its value will be determined by fitting the data.

In the usual analysis the capacitance, C_{in} , is assumed to be a constant value, independent of signal size. For a buried channel input, however, as the signal size decreases the input capacitance decreases. There are two effects which cause this decrease. In Figure 2 the distribution of the signal charge is shown into the silicon and as discussed in section II, the distance from the gate to the signal packet increases with decreasing signal, thus decreasing the capacitance. The second effect which decreases the effective capacitance for small signals is that the area that the signal charge occupies decreases since a small value of signal charge will not cover the entire region under the gate. The signal packet contracts toward the potential minimum which lies at the center of the gate.¹⁴

To experimentally determine the actual capacitance of the input node, a small change in voltage, ΔV , was made on the input gate, which was biased at a voltage corresponding to an input of N_{SIG} electrons, and the corresponding change in charge level, ΔQ , was monitored at the output. The capacitance, C_{in} (N_{SIG}), was then calculated from the expression

$$C_{in} (N_{SIG}) = \frac{\Delta Q}{B \Delta V} . \quad (18)$$

The factor B takes into account the imperfect modulation of the buried channel potential by the gate above it. For the devices tested the measured value of B was experimentally determined to range from 0.8 to 0.9. A typical result of this measurement is that the input capacitance varies from 0.004 pF for an input signal level of $2.5 \times 10^4 e^-$ to 0.013 pF at $6 \times 10^5 e^-$. The input noise would, therefore, be expected to increase by a factor of 1.8 over this signal range.

In Figure 11 the measured value of input noise for device B is compared to the calculated value obtained using the capacitance values determined using Eq. 18 and an excellent fit to the data results for $\alpha = 1.1$ in Eq. 17.

A very important point to note in this figure is the extremely low noise levels that were obtained for very small signals.

For example only 10 noise electrons were introduced for the signal level of $6.2 \times 10^3 e^-$. The rapid decrease in noise for very small signals ($< 10^4 e^-$) is due to the decrease in area occupied by the signal charge. It is therefore, possible to inject very low noise bias charge levels (slim zeros). These bias charge levels are necessary to obtain optimum performance with buried channel devices.

At higher signal levels the noise increases to approximately 50 noise electrons, this is still a very low level (about 5 times lower than any previous reported results) and verifies the expected low noise characteristics of the input structure shown in Figure 10.

There are some special characteristics of this structure, however, which may limit its usefulness in certain applications that are more demanding than noise measurements. Due to the dependence of the input capacitance on signal level, the input has a rather non-linear relationship between charge and voltage. A second difficulty is that because of the restricted size of the first CCD well it would require large voltages on the input and the first CCD gate in order to introduce a full well of signal charge.

VI. BULK STATE TRAPPING

The extremely low noise levels which were obtained for the other three CCD noise sources has made possible extensive characterization of noise due to bulk state trapping. The spectral density of the trapping noise was measured, as was its dependence on clock frequency and signal level.

The trapping of signal charge in bulk states affects the transfer efficiency and noise of buried channel devices in a manner similar to the way surface states determine the noise and transfer efficiency of surface channel devices. A thorough discussion of these effects has been presented,^{5,9,16} and only the points relating to the measurements to be presented will be reviewed in the next section. Following this review the results of spectral density measurements will be presented as a function of signal size and clock rate. In order to obtain the density and emission times of the bulk traps which are contributing to the noise the double pulse measurements of the loss will be presented. The double pulse technique

will then be extended to noise measurements and the emission times and densities obtained from these measurements will be compared with the results of the loss measurements.

REVIEW OF EFFECTS OF BULK STATE TRAPPING

The effect of impurities in the bulk silicon is to introduce trapping levels, which can be characterized by a single emission time. When a sufficiently large charge packet comes into contact with these traps they are rapidly filled. This fill time is strongly dependent on signal size, but except for very small signals it is extremely fast compared to standard clock rates (< 10 MHz). As the charge packet is transferred to the next electrode, these traps will emit a portion of the trapped signal charge and this reemitted charge will transfer along with the signal packet. However, after a transfer time T_t , additional emitted charge will reside in trailing charge packets, which results in charge loss from the initial packet. To determine the net amount of charge that is lost from a signal packet, it is necessary to know the initial occupancy of the traps.

A simple case in which this occupancy can easily be determined is the case of a train of signal packets ("ones") which are followed by a series of N_z empty packets ("zeros"). The loss per transfer due to bulk trapping in the first "one" after N_z zeros is⁵

$$N_z^{\text{loss}} = M V_{\text{SIG}} \sum_i N_i e^{-T_t/\tau_i} [1 - e^{-N_z T_c / \tau_i}] \quad (19)$$

where V_{SIG} is the volume that the signal charge (the ones) occupy, N_i is the density of the i th bulk trap which is characterized by an emission time τ_i , T_c is the clock period and M is the number of transfers.

The rms noise, $n_{B.T.}^{N_z}$, introduced into the first one after N_z zeros is⁵

$$(n_{B.T.}^{N_z})^2 = M V_{\text{SIG}} \sum_i N_i [e^{-T_t/\tau_i} (1 - e^{-T_t/\tau_i}) + e^{-(N_z T_c + T_c)/\tau_i} (1 - e^{-(N_z T_c + T_c)/\tau_i})] \quad (20)$$

In the latter part of this section both the loss, N_z^{loss} and the noise $n_{B.T.}^{N_z}$ will be measured as a function of N_z . From these measurements the density and emission times of the bulk states which are present in the buried channel will be determined by fitting the data to Eqs. 19 and 20.

Inspection of Eq. 19 and 20 indicates that knowing the transfer time T_t is very critical to interpretation of any data which is fit to these equations. However, the transfer time, T_t , is a somewhat difficult parameter to determine, since it depends strongly on the clock waveform used to drive the device and the dynamics of charge transfer. A simplified model to determine the dependence of the transfer time on clock waveform is outlined in Figure 12. In curve A of this figure the channel potential is shown with signal charge being stored under the \emptyset_1 well. The bulk states will therefore be completely filled under this electrode. In curve B the signal packet has transferred to \emptyset_2 and the charge emitted from the bulk states under \emptyset_1 are swept into the adjacent \emptyset_2 well. This is the beginning of the transfer time interval. In curve C the signal packet has transferred to \emptyset_3 , and the emitted charge is now sufficiently removed from the initial charge packet so that there is an equal probability for the signal charge to transfer along with the signal packet or to transfer into the following packet and this will be considered the end of the transfer time interval. Using this model the transfer time, T_t , for a four-phase device as a function of fractional overlap of adjacent clock phases is found to be

$$T_t = (.375 - Y/2) T_c \quad (21)$$

Since the overlap can vary from almost 0 to 3/4 a wide range of transfer times are possible for a single clock rate. This is in contrast to the usual assumption for T_t which is that $T_t = T_c/p$ where p is the number of clock phases.^{6,11} From Eq. 16 and 23 it can be seen that the noise which is contributed by a given species of bulk trap can be varied substantially by simply varying the clock overlap, therefore care must be taken to keep the overlap constant in order to obtain consistent data especially in comparing data at different clock rates.

The noise due to bulk trapping has several distinctive characteristics which

make it simple to separate from the other CCD noise sources. Besides the dependence on the occurrence of signal charge (given by Eq. 20 for a simplified case) it also depends on the signal size. As the signal charge increases in size, the volume it occupies, and thus the number of bulk states it interacts with also increase. This is shown in Figure 2 in which the volume is seen to increase from a 500 Å wide layer for a small signal to a 1500 Å wide layer for a large signal. Figure 2 is a one-dimensional plot and therefore does not include the contraction of the signal packet to an area that is less than the size of the gate. These edge effects will be found to be important for very small signals and thus the volume (and therefore the noise) is found to decrease substantially at low signal levels.

The most unambiguous characteristic of bulk state trapping is the dependence of the spectral density on frequency and for the case of a continuous input signal the spectral density has been calculated by Thornber and Thompsett.¹² Their calculation has shown that because of the correlation which exists between noise in adjacent charge packets (a deficit in one packet results in excess in the adjacent packet) the spectral density has a distribution $n_{B.T.}^2(f)$, in units of equivalent rms noise electrons (see Section III), given by

$$\left(n_{B.T.}^2(f) \right)^2 = \left(n_{B.T.}^0 \right)^2 \left(1 - \cos \frac{2\pi f}{f_c} \right) \quad (22)$$

where $n_{B.T.}^0$ is calculated by setting $N_z = 0$ in Eq. 20. This dependence was already exploited in the measurement of the input noise (see Section VIII) and will be used in the next part to provide unambiguous identification of the bulk state trapping noise. Therefore, it will be possible to obtain experimental verification of the above theoretical expressions and it will be found that satisfactory agreement was obtained in all cases. The first set of measurements to be described will be spectral measurements for varying signal levels and these will be followed by a series of rms voltage measurements in which the dominant bulk traps are identified.

SPECTRAL DENSITY MEASUREMENTS

The purpose of these measurements was to verify the spectral dependence predicted

by Eqn. 22. In Figure 8 the noise power has been separated into two components. The dashed line represents the contribution of the input noise which was discussed in Section VIII, and added to this (since noise power is being summed it is a linear addition) is the noise due to bulk state trapping. The solid line is a fit to the trapping component of the noise by the expression for $n_{B.T.}^2(f)$ given in Eq. 22 in which N_z was used as a curve fitting parameter. The fit is found to be excellent for a value of $n_{B.T.}^0 = 52 e^-$. If only one type of bulk state is contributing to this noise and if it is assumed that this bulk state has an emission time of 0.7 μsec (so that the peak in the noise occurs at a 500 kHz clock rate), then a trap density of $1 \times 10^{11} \text{ cm}^{-3}$ is required to obtain the measured noise level. Measurements as a function of clock rate, given later in this section, indicate there is a peak in the noise near 500 kHz so that the assumption of a 0.7 μsec trap emission time appears valid. It should be noted that the use of double pulse measurements discussed at the beginning of this section are a more accurate way to obtain the bulk state density⁵ but it would require a high clock rate (> 5 MHz) to observe this .7 μsec level.

As discussed previously, as the size of the signal charge increases then the noise should increase. Figure 13 shows the spectral density of the bulk state trapping noise for signal levels from 1870 e⁻ up to $7.5 \times 10^5 e^-$. As expected as the signal charge is increased, the amount of bulk state trapping noise, also increases. For each signal level the characteristic $(1 - \cos 2\pi f/f_c)$ spectral dependence is clearly observed. It is interesting to note that for the signal level of 6250 e⁻ the rms number of noise electrons was 42 e⁻, whereas for the even lower level of 1870 e⁻ the rms number of noise electrons is only 16 e⁻. For this range of input signal the number of noise electrons is decreasing almost proportionally with the signal level. This is due to the contraction of the charge packet to a reduced area in the center of the electrode. This result is significant for very low light-level imaging where it is important that trapping noise not degrade small signals.

A more direct plot of the bulk state trapping noise as a function of signal level is given in Figure 14 for three different

devices. In this figure the rms noise power is plotted as a function of signal level and is determined by integration of noise power curves like those in Figure 13 using Eq. 5. The noise is seen to rise rapidly at small signal levels (an increasing area of the electrode is being filled with signal) and then to rise slowly with further increases in signal size as the charge packet increases its volume by spreading toward the surface is shown in Figure 2. Even though all three of these devices were processed at the same time (in fact A and C were on the same slice), the bulk state trapping noise at $N_{SIG} = 4 \times 10^5 e^-$ is quite variable ranging from $34 e^-$ for device B to $55 e^-$ for device D.

An important characteristic of bulk state trapping is its dependence on clock rate. Figure 15 shows a plot of the rms number of noise electrons for two devices, and the clock frequency dependence of the noise is readily observable. However, since there are no well-defined peaks and nulls in the noise, it is difficult to determine from this figure the individual emission times and densities of the bulk states that are giving rise to the noise. In fact, it seems likely that there are several states of varying densities and emission times which, when added together, result in the relatively smooth clock rate dependence seen in Figure 15. One aspect of this figure that can be commented on is the increase in noise of device A as the clock rate is decreased to 50 kHz. From double pulse measurements to be described in the next section identifies a bulk trap which has a 12 μ sec emission time. From these measurements it is predicted that this trap should yield a peak noise of $55 e^-$ at a 45 kHz clock rate, which is consistent with the data presented here in Figure 16.

Figures 12 through 16 show data from only a few devices, but these results are typical of the much broader sampling that was measured. For a signal input of $5 \times 10^5 e^-$ at a clock rate of 500 kHz the bulk trapping noise for 10 devices was found to range from a low of $37 e^-$ to a high of $96 e^-$.

From spectral density measurements it is possible to unambiguously identify how much noise is due to bulk state trapping but it is difficult to extract information about which bulk traps are contributing

to the noise. In the next section a different type of measurement will be described which measures the emission times and densities of these traps.

DOUBLE PULSE MEASUREMENTS OF LOSS

Equation 19 suggests a very simple measurement to determine the emission rates of the bulk traps which is analogous to the double pulse measurements first performed on surface channel devices by Carnes and Kesonocky.¹¹ The experiment proceeds by measuring the loss in the leading edge of a series of ones as a function of the number of zeros between sets of ones. If this is plotted on semi-log paper, using Eq. 19, emission times of the bulk traps can easily be identified.

In conducting these measurements on buried channel devices, a refined technique was developed. Reference to Figure 16(a) indicates the difficulty in accurately quantizing the transfer inefficiency of a very low-loss CCD shift register. It is unrealistic to expect accurate visual estimation of the leading edge loss or trailing edge residue. It is difficult to amplify this waveform and investigate the differences in the leading or trailing pulses without exceeding the dynamic range of the preamplifier or oscilloscope. Without an improved technique, the device in Fig. 16a would be described as having a charge transfer efficiency of about 0.99999. The improved procedure involves sequentially sampling-and-holding the CCD output resulting from the first and second packets in the pulse train. Since for a small amount of loss from the first packet, the sample-and-hold output is a dc level corresponding to the pulse-train level with a slight perturbation due to the difference in the first two pulse amplitudes, it is possible to ac-couple and amplify this difference without dynamic range problems. The resulting waveform is shown in Figure 16(b). The transition from the first pulse level to the second is clearly 10 mV. Since for devices with very small loss, the loss is confined to the first packet, the transfer efficiency can be calculated from this figure and is found to be .999992.

Figure 17 shows curves for two devices which give very close agreement with Eq. 19. The data are plotted as a function of time between pulse trains

instead of the number of zeros to facilitate the extraction of information about the emission time of the bulk states. The loss is expressed as a fraction of the signal packet lost out of the first one after N_z zeros. The solid lines in this figure are calculated curves using the expression given in Eq. 19. A summary of the results obtained from this measurement is given in Table I. The bulk state densities given in this table were calculated using a charge packet volume of $2 \times 10^{-10} \text{ cm}^{-3}$, (which is obtained from a potential profile calculation) for devices A and B. The signal packet size used in the measurement was $7 \times 10^5 e^-$ for both devices.

For device A there were two bulk states which contributed to the loss; one with emission time of 900 μsec and the other with a 12 μsec emission time. Device B only exhibited trapping by the bulk state with a 900 μsec emission time. Measurements of thermally stimulated capacitance²⁰ have shown that gold has an emission time of 900 μsec and on this basis the 900 μsec bulk state observed in these CCDs is identified as resulting from gold impurities. Further evidence for this identification is provided by Collett¹⁹ who made variable temperature measurements on a buried channel MOSFET and determined that the bulk state which had a 900 μsec lifetime was located ~.54 eV from the band edge which is the location of one of the gold trap energy levels.

The impurity which has a 12 μsec emission time that was observed in device A has not been identified.

DOUBLE PULSE MEASUREMENTS OF NOISE

From the double pulse measurements of loss several bulk states were identified. If a similar double pulse measurement is made but instead of measuring loss in the first "one" after N_z "zeros", the rms noise is measured, a peak in the noise should occur when the time between the ones, $N_z T_c$, is approximately equal to the emission time of these bulk states (Eq. 20). For example, for device A there should be a peak in the noise near 12 μsec and 900 μsec . In Figure 18 the measured noise of device A as a

function of $N_z T_c$ is shown and as expected the noise exhibits peaks near 12 μsec and 900 μsec . In addition, another peak is seen to appear which corresponds to an emission time of 20 ms which was out of the range of the loss measurements. In this Figure only the noise dependent on N_z is plotted. An expression for $n_{D.P.}^{N_z}$ can be derived from Eq. 20 by only keeping the terms dependent on N_z :

$$(n_{D.P.}^{N_z}) = M V_{SIG} \sum_i N_i e^{-\frac{(N_z T_c + T_t)}{\tau_i}} \left[\frac{(N_z T_c + T_t)}{\tau_i} \right] \quad (23)$$

The solid lines in Figure 18 are a fit to the data using this expression in which the bulk state densities N_i are treated as a curve fitting parameter. The same emission times that were used to fit the data in the double pulse loss measurements in (Figure 17) were used in fitting this data.

The bulk densities determined to be a best fit are $2.0 \times 10^{11} \text{ cm}^{-3}$ for the bulk state with the 12 μsec emission time and $2.4 \times 10^{11} \text{ cm}^{-3}$ for the bulk states with the 900 μsec and 20 msec emission times. These values compare favorably with those obtained by the loss measurements which are given in table I for device A.

The two sets of data, shown as triangles and dots in Figure 18 correspond to two separate sets of measurements. The variation in these two sets of data gives an indication of the reproducibility of the measurement.

X. CONCLUSIONS

Noise measurements were made on a linear 150 stage buried channel CCD. The total device noise was found to be composed of four components; the electrical insertion of signal charge, bulk state trapping, dark current noise, and the output amplifier. We did not observe any of the extraneous excess noise sources such as pulser noise and abnormally high input noise which have been observed by previous authors.^{18,20}

In making these measurements the concept of correlated double sampling¹ was used in an output amplifier which had a noise level which was equivalent to less than 30 noise electrons. The dominant noise sources in this amplifier were discussed.

A low noise input structure^{2,3,4} for electrical insertion of signal charge was used which introduced a signal which had a noise level which ranged from 10 to 60 e⁻.

The extremely low noise levels which were obtained at the input and output made possible direct measurement of the noise due to bulk state trapping. In fact, even for very high quality devices (transfer efficiency > .99999) because of the advances made in reducing the input and output noise, it was possible to observe the noise due to bulk states. The spectral density of the bulk state noise was presented as a function of frequency and signal level and was found to be in good agreement with the theoretical modeling for trapping noise.

APPENDIX A

ANALYSIS OF NOISE TRANSFER FUNCTION OF CORRELATED DOUBLE SAMPLING FOR BANDLIMITED WHITE NOISE

In this appendix the effect of the correlated double sampling on a band-limited white noise source, V_n , will be derived. The band-limiting will be assumed to be performed by an RC single-pole low-pass filter. If thermal noise in resistor R of this filter is non-negligible, it may be treated as all or part of V_n .

First, the autocorrelation function, $R(t)$, of the band-limited noise must be derived. This can be found by taking the Fourier transform of the single-sided noise power spectrum [$V_n^2 H^2(\omega)$],

$$R(t) = \frac{1}{2\pi} \int_0^\infty e^{j\omega t} V_n^2 H^2(\omega) d\omega \quad (A-1)$$

where $H^2(\omega)$ is the transfer function of the low pass filter,

$$H^2(\omega) = \frac{1}{1 + \left(\frac{\omega}{\omega_c}\right)^2} \quad (A-2)$$

in which ω_c is the 3 dB point of the RC filter

$$\omega_c = \frac{1}{RC} \quad (A-3)$$

Evaluating the integral of Eq. (A-1), the following result is obtained:

$$R(t) = V_n^2 B e^{-t/RC} \quad (A-4)$$

where B is the noise bandwidth of a single-pole RC filter

$$B = \frac{1}{4RC} \quad (A-5)$$

The rms output voltage of the CDS, V_{CDS} , is the difference in the input voltage level, $V(t)$, at two points in time separated by a time interval Δt , which is given by¹³

$$V_{CDS}^2 = \lim_{T \rightarrow \infty} \frac{2}{T} \int_0^T [V(t)]^2 dt - \lim_{T \rightarrow \infty} \frac{2}{T} \int_0^T [V(t + \Delta t)]^2 dt \quad (A-6)$$

where it has been assumed that $V(t)$ is stationary. Using the definition of an autocorrelation function

$$R(\Delta t) = \lim_{T \rightarrow \infty} \frac{1}{T} \int_0^T V(t)V(t + \Delta t) dt \quad (A-7)$$

$(V_{CDS})^2$ can be rewritten as

$$V_{CDS}^2 = 2 [R(0) - R(\Delta t)] \quad (A-8)$$

Substituting (A-4) into (A-8) the following result is obtained:

$$V_{CDS}^2 = [2V_n^2 B (1 - e^{-\Delta t/RC})]^{\frac{1}{2}} \quad (A-9)$$

If this voltage level is referred to the CCD channel and then multiplied by the CCD output capacitance, the noise level is then converted into noise electrons, n_{CDS} ,

$$n_{CDS} = \frac{C_o V_n}{Aq} [2B(1 - e^{-\Delta t/RC})] \quad (A-10)$$

where A is the amplification between the CCD output and the noise source v_n .

To obtain Eq. 7 the appropriate wide band noise, v_n , to substitute into A-9 is the thermal noise of R_{off} , $(4kT R_{off})^{1/2}$, which is band limited by C_0 , resulting in a noise bandwidth of $B = \frac{1}{4R_{off}C_0}$.

For Eq. 10 the wide band noise of interest is given by Eq. 11 which is band limited by the R_1C_1 filter so that $B = \frac{1}{4R_1C_1}$.

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TABLE I

Device	Bulk State 1	
	Emission Time (μ sec)	Density cm^{-3}
A	900	1.7×10^{11}
B	900	1.7×10^{11}
 Bulk State 2		
Device	Emission Time (μ sec)	
		Density cm^{-3}
A	12	1.4×10^{11}
B	-	0

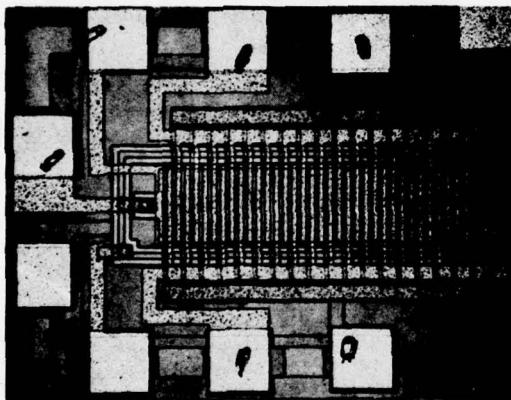


Figure 1. One end of the linear shift register used in the noise measurements.

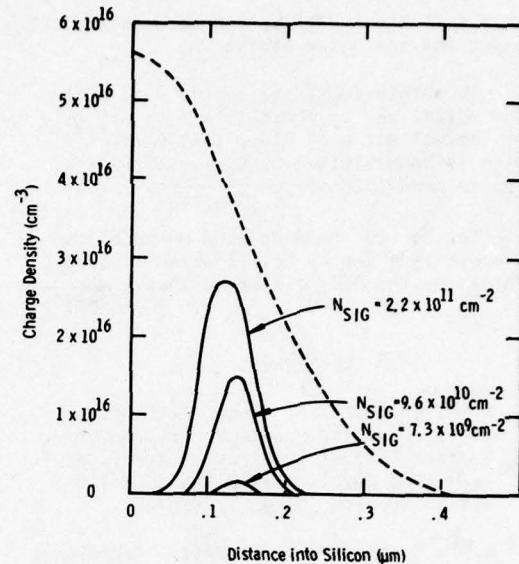


Figure 2. The charge distribution in the buried channel (solid line) shown with the impurity distribution (dashed line).

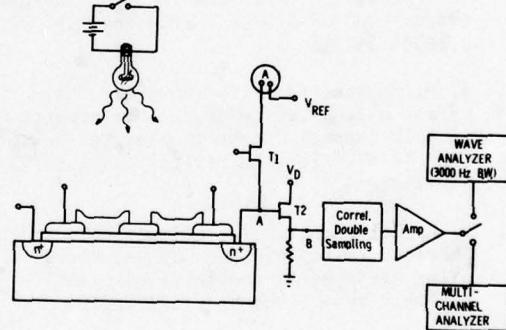


Figure 3. The test set-up used for the noise measurements.

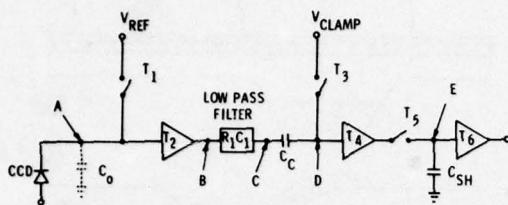


Figure 4. Schematic of the circuit used to implement correlated double sampling.¹

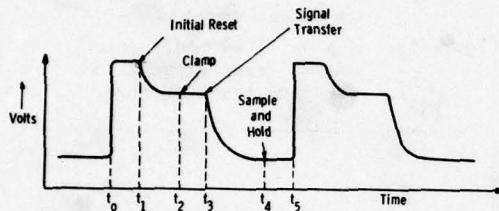


Figure 5. The voltage waveform observed at point B in Figure 4.

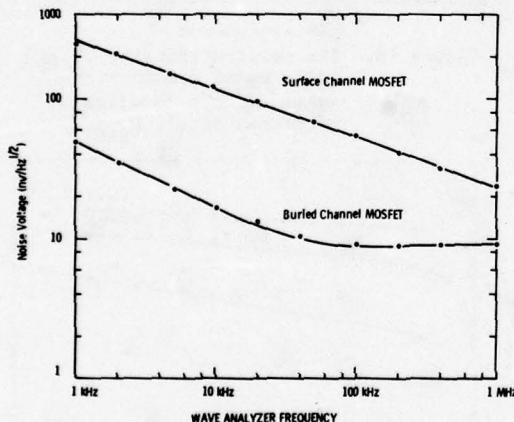


Figure 6. Comparison of noise voltage for buried and surface channel MOSFETs.

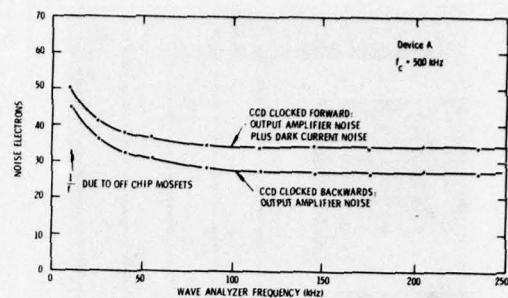


Figure 7. Output amplifier and dark current noise of device A.

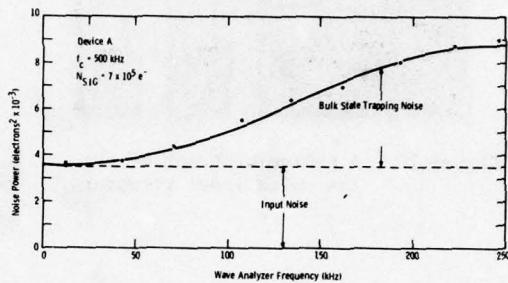


Figure 8. Measured spectral density of noise power showing peaking at high frequency due to bulk state trapping.

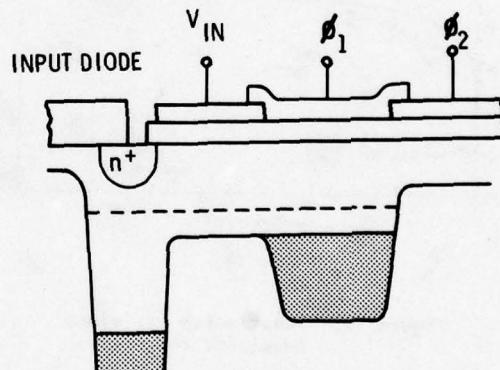


Figure 9. Input structure for the fill and spill input technique.^{2,3,4}

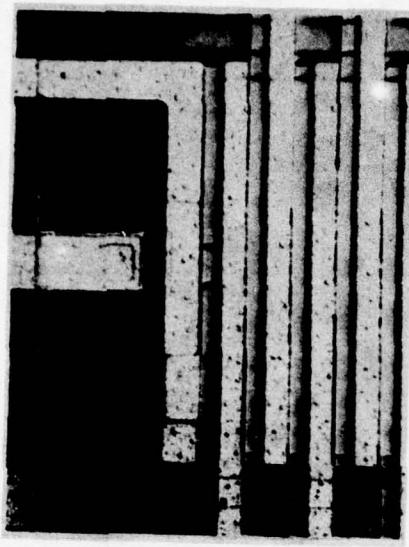


Figure 10. A photomicrograph of the low noise input structure.

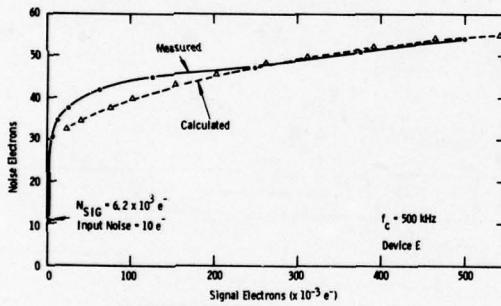


Figure 11. Input noise vs. signal level for device E.

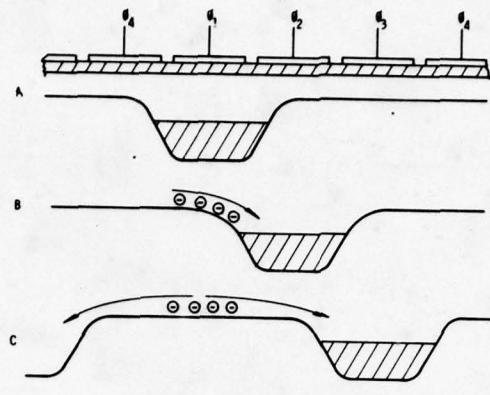


Figure 12. A simplified model for charge transfer used to estimate transfer time.

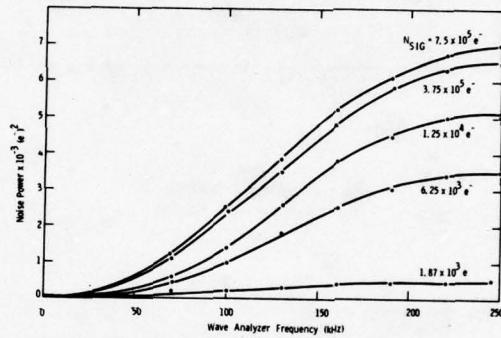


Figure 13. The spectral density of noise power due to bulk trapping as a function of signal level, N_{SIG}^*

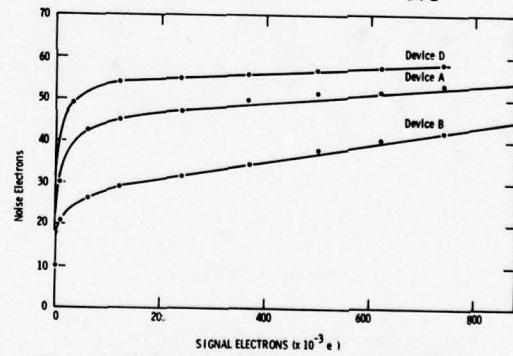


Figure 14. Measured dependence of bulk trapping noise on input charge level.

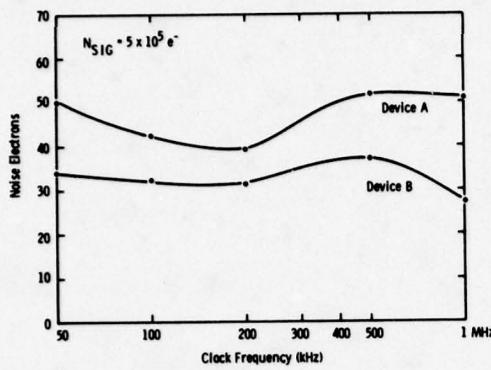


Figure 15. Measured dependence of bulk state trapping noise on CCD clocking frequency.

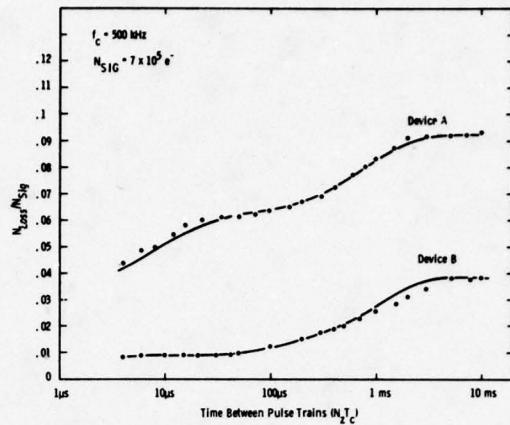


Figure 17. The double pulse measurements of loss due to bulk state trapping with the solid lines obtained by fitting to Equation 19.

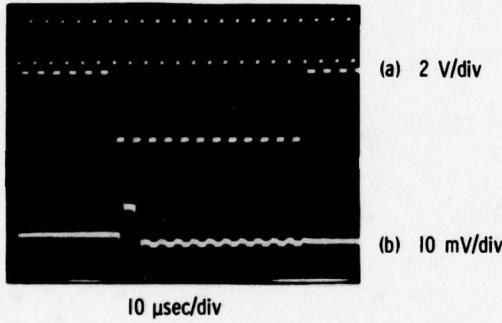


Figure 16. Measurement of transfer efficiency for CCD.
(a) Pulse Train Response
(b) Sample and Hold Output

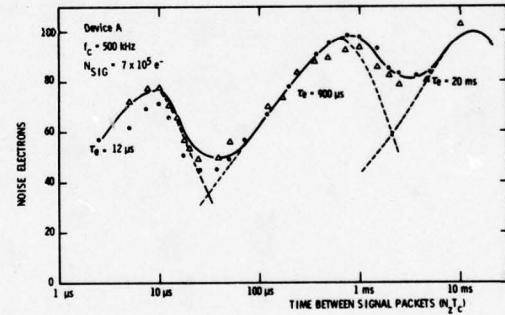


Figure 18. The double pulse measurement of noise due to bulk state trapping with the solid lines obtained by fitting to Equation 20.

Noise Linearity and Trapped Charge Measurements
with Charge Sensitive Amplifiers

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ABSTRACT. A measurement technique is described for precise determinations of the magnitudes of the charges flowing in a CCD and their statistical distribution as a function of clock number and related to changes induced on specific clocks. The method involves the use of charge sensitive amplifiers, sample and hold circuits and pulse amplitude analysers commonly used in nuclear measurements. The advantages of off-chip amplification for quantitative determinations and comparisons between devices are demonstrated. Measurements on a few CCDs showing some of the merits of the technique are included. Direct measurements of the charge injected electrically at the input and the noise associated with this are also possible.

1. INTRODUCTION

Determination of the magnitudes and the times of collection of pulses of charge generated in radiation detectors by incident quanta is a common and long established experimental procedure in nuclear measurements. A precision of one part in 10^3 in pulse amplitude and a small fraction of $1\mu s$ in time is routinely achieved and the stability of the amplitude measurements is generally required to be better than one part in 10^4 . The pulses of charge usually contain between 10^3 and 10^7 carriers and occur randomly in time. The detector is electrically equivalent to a capacitor, and signal amplification and noise in such systems has been extensively studied^(1,2). Sophisticated equipment for measuring pulse amplitudes⁽³⁾ and advanced signal processing methods^(4,5) have also been developed for these applications.

Our interest in charge coupled devices is centred round their application in signal processing and we are using nuclear measurement techniques to study the performance of these new devices. The linearity and noise of CCDs is of the utmost importance in view of the above stringent requirements. Inefficient charge transfer in a CCD introduces a complex time varying characteristic which may make these devices

unsuitable for many nuclear instrumentation applications. It is the purpose of this paper to describe measurement techniques which we believe will lead to a better understanding of the phenomena which limit their performance. The results of measurements on a few CCDs will also be given.

2. THE METHOD

Frequency domain analysis and measurements are unlikely to give a clear indication of the physical processes in a CCD which essentially operates in the time-domain. One of the main features of a CCD is that the clock need not be regular and signal processing applications where the clocks are not repetitive can only be analysed by time-domain methods. If there is adequate knowledge of the devices in the time-domain it is relatively easy to predict their behaviour in the simpler case when the clock is regular and at a fixed frequency.

The present study is therefore aimed at measurements of charge flow using clock pulses occurring in bursts with the period T_0 , total number N_0 in the burst and the repetition rate of the bursts independently variable. Charge is inserted into the input electrically

either as a single charge packet on a specific clock, once in each burst, or combined with a constant level of charge packets of independently variable magnitude extending over a number of clocks. The average value of the output charge on any specified clock or the integral over a number of adjacent clocks is measured with a digital voltmeter and the statistical distribution of amplitudes of the individual packets over a large number of bursts is measured with a pulse amplitude analyser(3). This latter measurement will give r.m.s. fluctuations of the charges. These measurements are repeated over a range of clock numbers and at different clock frequencies.

The system has been designed to measure the absolute magnitudes of the charges to about 5%. The stability of these measurements is better than 0.2% and the relative measurements of charge are also to this accuracy or to 1 fC whichever is the larger. Such precision is expected to yield useful information on the charge states and transfer properties of the CCD. In order to maintain moderately high accuracy the amplitudes of all drive waveforms including those to the input diode and gate are maintained to an accuracy of about 50 mV. The short term fluctuations and the noise on these waveforms is estimated to be less than 1 mV. The measurements with the present system are not reliable at clock frequencies in excess of 1 MHz owing to the precautions taken to maintain accuracy but faster circuit techniques may make it possible to extend the measurements to 5 MHz.

3. EXPERIMENTAL APPARATUS

A block diagram of the major parts of the equipment is given in fig 1. A brief description of the features of each part will now be given.

3.1 CCD AND DRIVE

All the CCD's used in our measurements were three phase n-channel devices with an input diode, one input gate, output diode and one output gate. The output gate and output diode were held at fixed potentials of +3 V and +7 V respectively for most of the measurements. Electrical charge input was achieved by pulsing the input diode and input gate within the duration of the ϕ_1

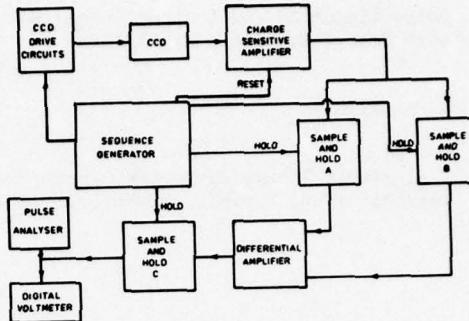


Fig 1

Block diagram of equipment

drive waveform as shown in fig 2. This is a surface potential equilibration method as described by Tompsett(6) with the difference that the durations of the charge setting time T_g and equilibration time T_E are fixed and independent of the clock rate. As shown in fig 2 the input diodes were normally held at $E_C + 2$ volts, where E_C is the phase-clock amplitude and pulsed to a low voltage for charge injection. E_C was +10 V for all the measurements reported here. The total number of input diode pulses is limited to about 20 from the first phase clock.

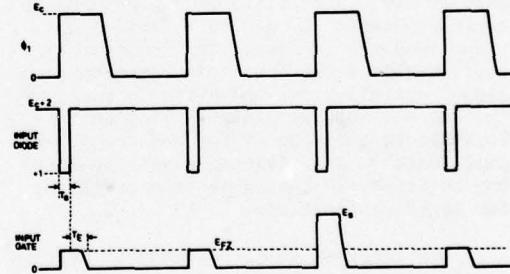


Fig 2

CCD drive waveforms for electrical charge input

The input gate is normally held at 0 volts and pulsed to E_{FZ} or E_s where E_{FZ} is the fat zero control level and E_s is the signal control level. The signal pulse E_s is applied only on one nominated clock N_s clocks after the beginning of the phase clocks and N_s is variable from 0 to 9. The fat zero level of pulses on the input gate were maintained on all clocks except the signal clock for the entire duration of the burst of phase-clocks. However since the total number of the input diode pulses was restricted to about 20 clocks the injection of fat zero signals terminated at that point. This enabled us to study the build-up and decay of fat-zero pulses at the output. The phase-clocks had an overlap of 50 ns and a linear fall time of 150 ns except in the experiment on linearity described later.

3.2 THE CHARGE SENSITIVE AMPLIFIER

The measurements reported here depend critically on the performance of this amplifier. There are two parts as shown in the simplified schematic in fig 3. The charge signals are amplified in the low noise amplifier⁽²⁾ which has a JFET input stage and a feedback capacitance C_f which defines the charge sensitivity. With adequate forward gain A the output voltage is equal to Q/C_f , where Q is the charge signal at the input.

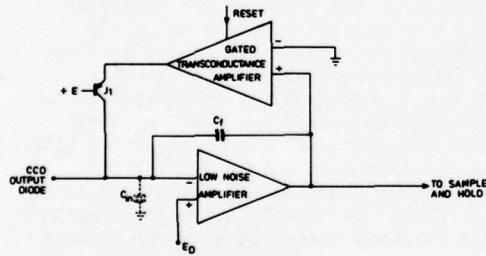


Fig 3

Schematic of charge sensitive amplifier and reset system

The gated transconductance amplifier is normally off so that transistor J_1 passes only the small leakage current of

less than 100 pA. When a reset signal is applied this current increases and the output voltage of the low noise amplifier is quickly restored to near 0 volts which is the reference input to the transconductance amplifier. In this reset condition the voltage at the output diode of the CCD will be close to E_D which is the reference voltage into the low noise amplifier. Reset is not applied during any of the clocks inside the sampling period or during the preceding or following clock i.e. during the period from $N - 1$ to $N + n + 1$.

Because of the large amount of negative feedback over the charge sensitive amplifier its input impedance is low and equivalent to a capacitance of value AC_f . The feedback capacitance is 0.8 pF so that an output voltage of 1 mV corresponds to an input charge of 5×10^3 electrons. Since this is virtually independent of the CCD output capacitance (at the output diode or on a floating gate) the calibration of the system is maintained for any CCD connected to the input. Another important consequence of this arrangement is that any contribution to the non-linearity due to the finite output conductance⁽⁷⁾ of the CCD, particularly when using floating gate sensing, can be entirely eliminated.

The leakage current of the input JFET is a few pA so that most effects of this can be ignored. The equivalent noise of the amplifier is about 0.11 r.m.s. electrons-Hz^{-1/2} referred to its input. Typically therefore the noise contribution of the amplifier will be 78 r.m.s. electrons for a clock frequency of 1 MHz when the output signals are put through a 0.5 MHz low-pass filter. In our measurements however the actual noise due to the amplifier is about 430 r.m.s. electrons owing to the greater bandwidth and the double sampling method as explained in the discussion on the results. With a good on-chip amplifier it may be possible to reduce the amplifier noise to 0.025 r.m.s. electrons-Hz^{-1/2} if the noise voltage of the source follower is of the order of 10nV-Hz^{-1/2} and the total sensing capacitance including the gate capacitance of the source follower is 0.4 pF. Our measurements on some poly-silicon gate FETs gave an equivalent noise of about 0.1 r.m.s. electrons-Hz^{-1/2} which is not very different from the off-chip

amplifier used in these experiments. Furthermore the introduction of a feedback capacitance into the on-chip amplifier is not very convenient. Even if this were possible the value of this feedback capacitance is required to be about 0.2 pF in order to maintain a sufficiently low input impedance at the gate of the on-chip amplifier and this will result in a further degradation of the noise performance.

3.4 SAMPLE AND HOLD CIRCUITS

The output of the charge sensitive amplifier is processed in two stages. The sample and hold A is made to hold the level existing at clock N and sample and hold B holds at clock $N + n$ so that the output of the differential amplifier, after the clock $N + n$, is proportional to the charge collected in the n clocks starting from N. In our three phase system the "hold" instruction to both the circuits, for most measurements excluding the reverse connected tests on charge injection, is given on the ϕ_2 phase when there is no charge output from the CCD. The sample and hold circuit C is made to sample the output of the differential amplifier some time after clock $N + n$ so that the voltmeter and analyser do not see the transitions between clocks N and $N + n$. The accuracy and stability of the sample and hold and difference circuits is better than about 0.5 mV referred to the output of the charge sensitive amplifier i.e. about 2500 electrons. The noise level is negligible in relation to the charge sensitive amplifier.

3.5 DIGITAL VOLTmeter, ANALYSER AND RECORDER

The digital voltmeter is used to measure the mean amplitude of the charge signal in the designated range N to $N + n$ as determined by the sample and hold circuits and the pulse analyser records the amplitude distributions of this signal over a large number of bursts - at least 10^5 . From this distribution the r.m.s. noise in units of electrons referred to the CCD output is readily calculated.

The linearity of the CCD is also measured automatically by using a sweep voltage generator which sweeps the voltage E_s (or E_{FZ}) applied to the input gate

(see fig 2) linearly. At a fixed repetition frequency the number of counts recorded in each channel of the analyser is then inversely proportional to the slope of the transfer function of the CCD at that signal level. The actual transfer function can also be recorded automatically by using a chart recorder in place of the digital voltmeter.

4. RESULTS AND DISCUSSION

Three types of surface channel CCD's were tested. The first, MA302, is a 100 element aluminium gate device with gate length of 8 μm , width 100 μm and a gap between gates of 2 μm . The second, MA315, is a 10 element single level doped-undoped polysilicon gate device with gates of 10 $\mu\text{m} \times 75\mu\text{m}$ and inter-gate region of 4 μm . The third, MA318, is a 100 element device, similar to the MA315, with a gate width of 60 μm and with an on-chip amplifier.

4.1 NOISE ON SINGLE INPUT PACKET

The total capacitance, including the CCD, at the input of the charge sensitive amplifier was nearly 20 pF and the equivalent noise voltage of the FET was measured to be 0.9 nV-Hz $^{-\frac{1}{2}}$. This should give an equivalent input noise of 0.11 r.m.s. electrons-Hz $^{-\frac{1}{2}}$. In order to ensure that the waveform was reasonably flat between the 500 kHz clock transients we used a bandwidth of 4 MHz in the charge sensitive amplifier. The noise of the amplifier will then be equivalent to 220 r.m.s. electrons and taking two random samples should give an equivalent noise of 308 r.m.s. electrons at the output of the differential amplifier. The measured noise was about 430 r.m.s. electrons with the CCD taken out and an equivalent capacitance shunting the input of the amplifier. We cannot find a good explanation for this discrepancy except perhaps the effect of the finite rise time of the hold waveform in the sample and hold circuits. We are however confident that the measurements of CCD noise are accurate since these noise components do not change in the ϕ_2 clock phase when the sampling occurs.

Measurements of charge output and noise on the MA302 with only one charge packet at maximum level injected into

the input on clock 9 at 500 kHz clock rate are shown in fig 4. The output signals on clocks 109 and beyond was measured with $n = 1$ so that the magnitudes of individual charge packets are shown here. The back-

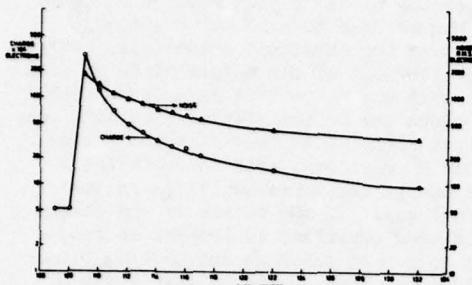


Fig 4

Charge output and noise of MA302
as a function of clock number with
single input, $N_s = 9$,
without fat zero

ground noise as measured on clock 90 was subtracted in quadrature and the noise is therefore that due to the presence of a signal. The fact that the small residual charge and noise 20 clocks or more after the main packet can be reproducibly measured gave us some confidence in the procedures adopted. There was a considerable variation in the magnitude of the charge output when the ambient temperature changed, presumably due to the change in losses due to trapping, and the noise measurements had to be made with automatic stabilisation of the mean signal amplitude in the pulse analyser. The noise measurements were then consistent over many repeated measurements.

The leakage current of the MA302 at the output was typically 5 nA without signal and the measured noise in the absence of signal was 420 r.m.s. electrons which is considerably greater than the noise expected from 5 nA confirming the excess noise reported earlier by Mohsen et al⁽⁸⁾. The leakage current fell to about 1 nA when ϕ_1 and ϕ_2 were kept permanently at 0 volts. One interesting feature was that the leakage current increased to more than 4.0 nA when ϕ_2 was kept at 0 volts. This behaviour is attributed to the buried n+ connection to the ϕ_2 gates causing current injection into

the output diode. Another observation was a partial decay of the transient waveform induced by the clock steps into the output diode with a time constant of the order of 5 μ s. If the coupling is purely due to capacitance the step functions of the clocks should be reproduced exactly at the output. Thorough investigation confirmed that this was not due to instrumental factors. From the above observations it is suggested that the high noise level of the MA302 in the absence of signal could be due to the pumping of charge into and out of the output diode by the various clock waveforms. The resultant current can have a small mean value but cause a high noise level owing to the components being emission or diffusion limited. It is therefore necessary to take great precautions on the details of the layout of all the diffused regions in the silicon as well as the gates and interconnections on top of the thin and thick oxides.

4.2 CLOCK NOISE

Considerable amounts of clock noise have been reported by Mohsen et al⁽⁸⁾ and Carnes et al⁽⁹⁾. Careful measurements of the noise of the MA318 with no signal present are given in table I. Since the normal output from this device was only available through an on-chip amplifier we operated the device reverse connected so that the originally intended input diode,

Table I

Noise of MA318 with no signal

	Total noise r.m.s. electrons
Charge sensitive amplifier without CCD	430
Charge sensitive amplifier and CCD without drives	425
Charge sensitive amplifier and CCD with drives	444

which has a direct connection, was connected to the charge sensitive amplifier as if it was the output diode. Since these measurements are concerned with the noise level in the absence of a signal the details of the

connections to the new input diode and gate are irrelevant so long as they were kept at potentials which prevented charge injection.

The noise measurement without the CCD was taken with a capacitance equal to the measured capacitance* of the CCD shunting the input of the charge sensitive amplifier. These measurements are reproducible to better than ± 3 r.m.s. electrons on the totals given above. The noise contribution of the CCD is estimated to be 130 r.m.s. electrons with the clocks present and no more than 50 r.m.s. electrons in the absence of the clocks. The mean leakage current with the clock present was about 1.1×10^{-4} electrons in each $2\mu s$ clock period and this could account for about 105 r.m.s. electrons of noise so that the increase of noise due to the clocks not explained by leakage is less than 80 r.m.s. electrons. It is not easy to determine how much of this may still be due to reversible charge pumping which has a small mean current at the output.

4.3 ELECTRICAL INJECTION NOISE

One of the significant causes of noise in a CCD used for signal processing has been ascribed to the electrical charge injection process at the input⁽⁸⁾. In normal operation it is not easy to separate this component from those due to charge trapping and free charge transfer inefficiency. The methods which use extrapolations of the noise from light signals injected at varying positions from the end of a long CCD and the net noise from electrical charge injection are not very accurate because they rely on the difference between large numbers. We have devised a method which should give a more direct and accurate figure for the electrical charge injection noise.

Let us consider the details of operation of the output gate and diode. In our case the bias for the output gate and output diode are +3v and +7v respectively

in order to perform the normal function of receiving the charge transmitted by the last ϕ_3 electrode. In this condition the output charge of the CCD is amplified by the charge sensitive amplifier connected to the output diode. If however the potential of the output gate is at least 1v higher than that of output diode, allowing for threshold potentials, charge will flow out of the output diode to fill the well under the last ϕ_3 gate on each ϕ_3 clock and be transferred back into the output diode at the end of the ϕ_3 clock. These charge flows will be amplified by the charge sensitive amplifier in the normal way. If the output of the charge sensitive amplifier is sampled on sample and hold A on clock ϕ_2 and on sample and hold B on clock ϕ_3 of the same clock N the difference will be the charge pumped out of the diode to fill the well under ϕ_3 . By suitable setting of the potentials at the output gate and diode it is possible to simulate the conditions at an input gate and diode during charge injection and equilibrium. The input diode can be connected to the charge sensitive amplifier and the magnitude of the charge injected into ϕ_1 can be obtained directly from these measurements. We studied the fluctuations in these charges and have arrived at the conclusion that the fluctuations are not much greater than the theoretical figure of $400\sqrt{2}Cg$ where Cg is the capacitance in pF of each of the two electrodes in the potential equilibration system. Details of this will be reported elsewhere.

An example of high injection noise due to incorrect operation of the fat zero level of the MA302 is shown in fig 5. The level E_{FZ} (fig 2) was kept at about 0.5v above the threshold in order to obtain a fat zero level of about 50% of the maximum charge. The correct operating voltage to obtain this fat zero level would have been about 6v when normal surface potential equilibration would have taken place. With only 0.5v on E_{FZ} the filling of the well under ϕ_1 would be emission limited and exhibit a large noise level. In order to demonstrate this a signal level E_s of 2.5v, which gives 75% of maximum charge with equilibration, was also set on clock 9 ($N_s = 9$). The resulting charge output and noise are seen in fig 5. It is seen that the noise on clock 109 was smaller than the

*Capacitance and leakage measurements of the CCD give variable results and these will be reported elsewhere.

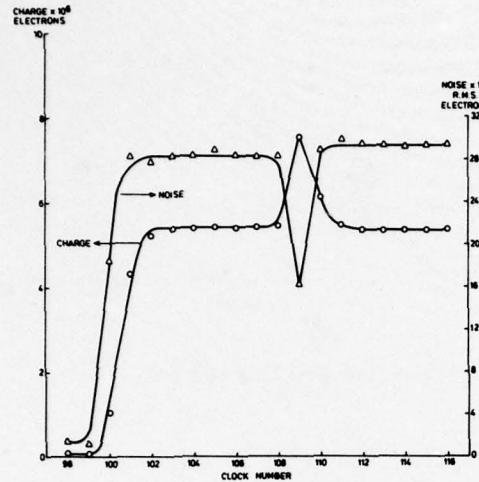


Fig 5

High injection noise in the MA302 when operated with incorrect voltage for obtaining fat zero and lower noise on a larger signal on clock 9 with correct potential equilibration

noise on the other clocks which exhibit the high noise due to incorrect operation of the fat zero.

4.4 CHARGE TRAPPING AND FREE CHARGE TRANSFER EFFICIENCY

A simple example of the effects of charge trapping is seen in fig 6. In this case the fat zero control level E_{FZ} of the MA302 was set at 1.5v in order to obtain maximum charge with correct potential equilibration. The signal level E_s on clock 9 was set at 0v so that no charge injection took place on this clock. It is seen that the noise builds up on clock 100 to a larger value than the steady state figure before the fat zero charge amplitude built up to the steady state level. Again when the charge on clock 109 falls to a very low value, owing to the absent signal on clock 9 at the input, the noise on clock 109 shows a slight increase and increases

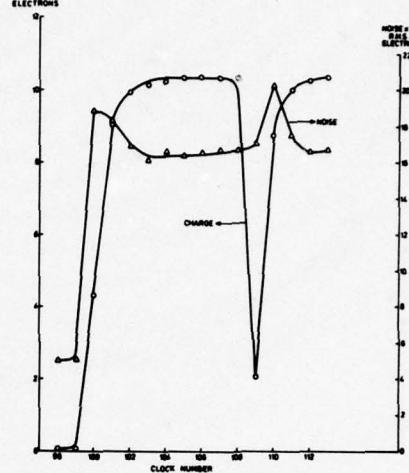


Fig 6

Noise build up in the MA302 on 100% fat zero and excess delayed noise on an absent signal

by a large amount on the trailing clock 110 before returning to the steady state value 2 clocks later. The exact nature of this behaviour will depend on the relationship between the clock period T_0 and the trap emission time constants.

A detailed study of the build up and decay of a string of fat zero pulses will yield information on the relative contribution of losses due to trapping and free charge transfer. Such measurements are in progress and an indication of the accuracy obtainable even with devices with high transfer efficiency is given in fig 7. One interesting aspect is that the figure for transfer inefficiency changes appreciably if many trailing pulses are taken into account rather than only the first one. If the charge recovered on the first trailing pulse only is used the transfer inefficiency of this device is calculated to be 4.9×10^{-4} without fat zero and 3.3×10^{-4} with fat zero. If however the total charge

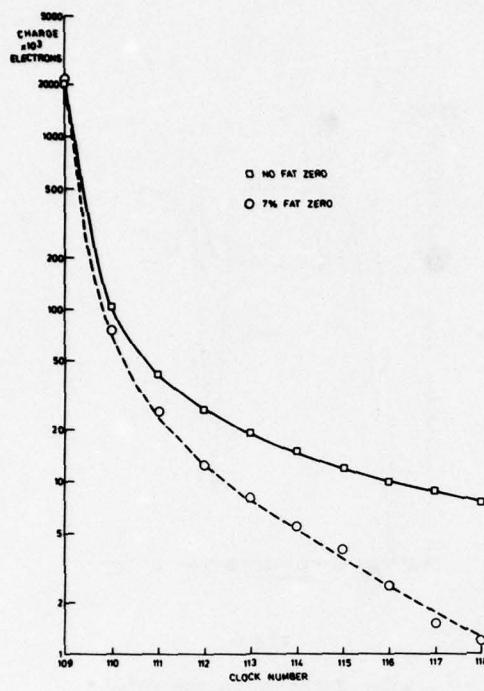


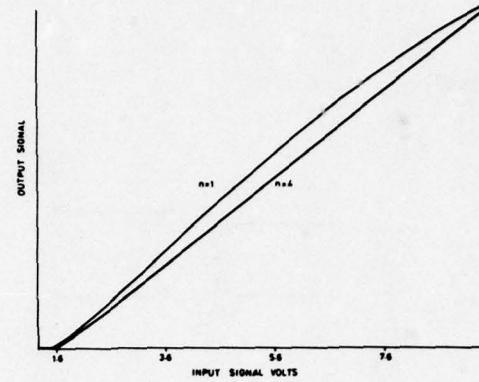
Fig 7

Charge output of MA318 as a function of clock number with and without fat zero.
The fat zero level was deducted
in these plots ($N_s = 9$, $n = 1$)

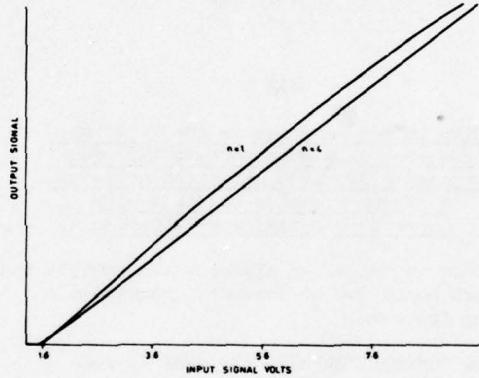
recovered in 10 trailing pulses is used in the calculation the figures are 1.2×10^{-3} without fat zero and 5.3×10^{-4} with fat zero.

4.5 LINEARITY

It has been shown above that the study of charge packet size and the associated noise as a function of clock number following a change in the input can give useful information on device behaviour. The study of linearity of the transfer function can be equally useful if it is suitably oriented. The normal transfer function measurement consists of recording the actual magnitude of the output charge as a function of the input and two examples of such a record are given in fig 8. All these measurements were made at a clock frequency of 500 kHz. In figure 8(a) the



(a) clock trailing edges 70 ns



(b) clock trailing edges 170 ns

Fig 8

Transfer function of MA315
measuring charge output in
the first clock ($n = 1$)
and on the total charge in
the first four clocks ($n = 4$)

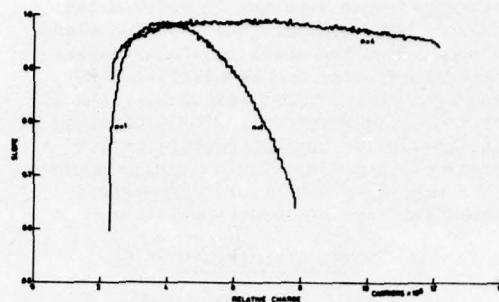
transfer function is plotted for the case where the trailing edge of the phase driving clocks had a linear fall time of 70 ns and the two curves correspond to the charge collected on the first pulse and the integral of the charge on the first four pulses. Fig 8(b) shows the measurements

with a clock fall time of 170ns. It is seen that there is some difference between these measurements but it is difficult to abstract quantitative information from these results. The output signal scales in fig 8 are only relative and have been adjusted in each case to make the maximum signal levels correspond to make comparisons easier.

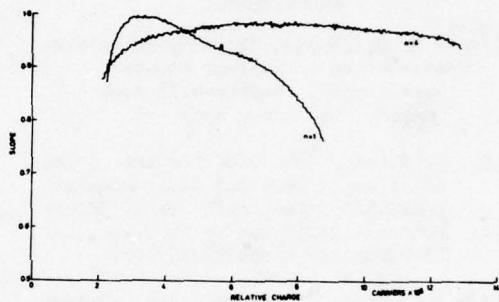
A much more reliable and accurate technique is one in which the differential coefficient of the transfer functions shown in fig 8 is plotted as a function of output charge. This is readily obtained automatically by sweeping the input voltage E_{FZ} or E_s (fig 2) linearly over some predetermined range, maintaining a constant pulse burst repetition frequency and plotting the number of counts recorded in each bit interval (channel) of the pulse analyser in fig 1. This is standard procedure for measuring linearity with pulse analysers and the results for the same cases as in fig 8 are shown in fig 9. The gross nonlinearity with $n = 1$ for the faster trailing edge of the clock due to variation in free charge transfer efficiency is reduced by integrating the output charge over four clocks ($n = 4$). However it is also noticed that the non-linearity when $n = 4$ is slightly worse for the longer trailing edge and for the smaller charge packets owing to charge trapped in the interelectrode gaps during transfer. It is seen that the differential linearity for $n = 4$ of this 10-element device with 10v clocks is better than 5% for a total charge output range of about 10^7 electrons (from 2×10^6 to 12×10^6). We have not attempted to interpret these in terms of harmonic distortion since the differential linearity gives a better and more direct indication of the expected performance of the device in our signal processing applications.

5. CONCLUSIONS

The measurement techniques reported here give accurate numerical figures which are a direct indication of the mechanisms governing CCD operation. Direct measurements of the charge injected and the noise associated with this process can be obtained so long as the connections to the appropriate electrodes are available. It has been shown that the noise performance of the off-chip amplifier is more than



(a) Trailing edges 70 ns



(b) Trailing edges 170 ns

Fig 9

Differential linearity measurements
for the conditions
identical to those in fig 8

adequate for most measurements. The linearity, constancy of calibration and low input impedance of the charge sensitive amplifier make it possible to make direct quantitative comparisons between a range of devices.

From the measurements reported it is evident that the background noise both intrinsic and extrinsic are quite small even with off-chip amplification. The

techniques used for the control of drive waveforms have resulted in clock noise figures much smaller than reported elsewhere. Even the small remaining excess background noise can be attributed to spurious charge flow induced into the CCD by the clock waveforms. The difficulty of calibration of on-chip amplifiers and their dubious linearity and noise performance make them unsuitable for serious investigations of device behaviour.

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ANTI-ALIASING CHARACTERISTICS OF THE FLOATING DIFFUSION INPUT*

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ABSTRACT. The CCD is inherently a sample-data device. It follows that preservation of signal-to-noise ratio requires that the noise on the processed signal be bandlimited to avoid aliasing. In many applications, particularly those involving integration of pre-CCD electronics onto the CCD monolith, it is desirable that this low-pass filtering be accomplished by the CCD input itself.

An analysis is presented of the small-signal frequency response of the floating diffusion (FD) input,^{1,2} which predicts a band-limiting effect approaching the $\sin x/x$ response of an ideal integrator. The analysis applies with equal validity to all inputs using the potential equilibration technique.^{1,2,3,4,5}

Frequency response data are presented together with noise measurements which agree well with theory. These measurements made on the FD input indicate excellent noise anti-aliasing under practical conditions of operation which maintain the insensitivity to threshold voltage inherent in this input.

I. INTRODUCTION

In most signal processing applications using CCDs, noise and dynamic range are important considerations. Because the CCD is inherently a sample-data device, the band-limiting of high frequency noise and signals (those above the Nyquist frequency) is essential to prevent aliasing. This is often accomplished using RC filters in the interface electronics preceding the CCD input.

This paper deals with the small-signal frequency response of the floating-diffusion input^{1,2}, a common input technique for injecting charge into CCDs. An analysis is presented which predicts that, properly operated, this input exhibits a frequency response approaching the $\sin x/x$ response of an ideal integrator and may be used to effectively prevent noise aliasing. Data are presented verifying this performance. The analysis is equally valid for the "fill-and-spill" or "potential equilibration" input^{1,2,3,4,5}.

The inherent anti-aliasing characteristics of the floating-diffusion input are particularly beneficial in applications where it is desired to integrate all of the pre-CCD interface electronics onto the CCD monolith itself in a high density format. Noise band-limiting is achieved without the undesirable threshold voltage sensitivity characteristic of the true integrator or "direct injection" mode of charge injection.⁶

II. REVIEW OF THE FLOATING DIFFUSION INPUT

The structure of the floating diffusion input is shown in Figure 1. In simple terms, the technique involves first setting the intermediate node to a voltage dependent on the signal voltage applied to the first transfer electrode V_{g_1} , and then resetting the node to a reference voltage applied to the transfer electrode V_{g_2} . The

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second process is accomplished through transfer of charge into the receiving CCD well; as such, the charge introduced is derived from the difference in the two preset levels multiplied by the capacitance of the floating node and is insensitive to threshold voltage (V_t) to the extent that V_t is the same under closely spaced electrodes.⁶ The noise characteristics of this input are known to be approximately described by kTC .^{1,2}

The first process in the two step sampling operation of the floating diffusion input is essentially the "fill-and-spill" or "potential equilibration"^{1,2,3,4,5} procedure applied to a diffusion instead of a CCD or MIS node. This process is initiated by pulsing the input diode (V_{id}) negatively (for an N channel CCD) to introduce excess charge onto the diffused node and then returning it to a high positive value to extract charge from the node while the channel current is controlled by the signal voltage applied to the input gate (V_{g1}). The first process is terminated by the pulsing of the second gate, (V_{g2}) which, for a multiplexer, is the serial-parallel transfer electrode. An analysis will next be presented which predicts that for noise, the time interval associated with the first process constitutes an effective integration time, τ , and the input acts to band-limit the noise.^{7,8}

III. FREQUENCY RESPONSE ANALYSIS OF THE "FILL-AND-SPILL" OR "POTENTIAL EQUILIBRATION" TECHNIQUE

As pointed out in the preceding section, the first step in the two-step sampling process of the floating diffusion input is identical to the "fill-and-spill" or "potential equilibration" technique. The only difference is that for the floating diffusion case, as charge is being extracted the gate V_{g1} acts as the gate of the MOSFET whose drain is the input diode and whose source is the diffused node; for the fill-and-spill input, the CCD potential well (or intermediate MIS node) acts as a virtual source. The equations describing the channel current are essentially identical. The input voltage is applied to the gate (V_{g1}) of the input transistor, and when the input diode V_{id} is pulsed positive, current flows into the capacitor (electrons "spill" out) until the channel current decreases to a small value, i.e., until $V_{fd} \approx V_{in} - V_t$. When V_{in} is a constant value, the problem

is well defined and the voltage transient can be calculated.² In reference 2, V_{in} is assumed to be constant, and the effect of channel noise is calculated. In this section an analysis is given of the case where the input voltage varies with time during the "spill" transient. The analysis applies to noise on the input or to small input signals.

The circuit diagram for the floating diffusion input during the spill cycle is shown in Fig. 2b. The capacitor voltage $v(t)$ increases after the input diode V_{id} is pulsed positive at $t = 0$. In the case where the input voltage is constant ($V_{in}(t) = 0$), the spill transient follows the curve $v_o(t)$ shown in Fig. 2a. For the above threshold case, $v_o(t)$ asymptotically approaches $V_{in} - V_t$ where V_t is the MOS threshold voltage. The spill transient is terminated after time τ when the charge on the capacitor is clocked further into the CCD.

Assume that a small ac signal $v_n(t)$ is applied to the input gate along with the time invariant V_{in} . The asymptotic value which the spill transient approaches changes with time, and the analysis which follows is based upon the fact that the form of the spill transient $v(t)$ depends only upon the asymptotic final value it would be approaching if the gate voltage remained at its instantaneous value $V_{in} + v_n(t)$. This follows from the fact that the channel current is controlled by the voltage between the gate and the floating diffusion node (i.e., the transistor gate-to-source voltage).

Suppose, as shown in Fig. 2a, an incremental change in gate voltage dv_{n1} occurs at some time t_1 . The result is to cause the transient to be further away from its new asymptotic final value $V_{in} - V_t + dv_{n1}$. By our assumption the waveform should have the same shape that $v_o(t)$ had at an earlier time $t_1 - dt_{n1}$, where

$$dt_{n1} = \left(\frac{dv_o}{dt} \right)^{-1} t_1 \quad (1)$$

Analytically, we have defined a new function $v_1(t)$ for the transient, which would be valid for all $t \geq t_1$ if no further incremental changes occurred at the gate. This function $v_1(t)$ is given by

$$v_1(t) = v_o(t - dt_{n1}) + dv_{n1} \quad (2)$$

where the dv_{n1} reflects the increase in asymptotic final value. Now, suppose a second incremental change occurs at time t_2 . In an identical manner a new delay time dt_{n2} is defined by

$$dt_{n2} = \left(\frac{dv_1}{dt} \right)_{t_2}^{-1} dv_{n2} \quad (3)$$

and a new functional form for the transient becomes

$$\begin{aligned} v_2(t) &= v_1(t - dt_{n2}) + dv_{n2} \\ &= v_o(t - dt_{n1} - dt_{n2}) + dv_{n1} + dv_{n2} \end{aligned} \quad (4)$$

Which, as before, would be valid for all $t \geq t_2$ if no further changes in gate voltage were to occur.

As a result of numerous incremental changes in input voltage, the node voltage at the end of the spill transient becomes

$$v(\tau) = v_o(\tau - \int_0^\tau dt_n) + \int_0^\tau dv_n \quad (5)$$

with dt_n given by

$$dt_n = \left(\frac{dv}{dt} \right)^{-1} dv_n \quad (6)$$

In calculating $\int dt_n$, it is assumed that the time varying input voltage $v_n(t)$ is sufficiently small that dv_o/dt can be used to approximate dv/dt in Eq. (6). This small signal restriction effectively linearizes a highly non-linear input and permits the definition of a linear transfer function. The physical significance of this linearization in terms of its restrictions on the amplitude of $v_n(t)$ remains the primary area for future analysis and experimental work. The simplifying effect of this assumption is that Eq. (5) can be integrated to give

$$v(\tau) = v_o(\tau - t_n) + \int_0^\tau \frac{dv_n}{dt} dt \quad (7)$$

where

$$t_n = \int_0^\tau \frac{dv_n/dt}{dv_o/dt} dt \quad (8)$$

At this point a further linearization is made. It is assumed that t_n is sufficiently small that $v_o(\tau - t_n)$ can be approximated by

$$v_o(\tau - t_n) = v_o(\tau) - \left(\frac{dv_o}{dt} \right)_\tau t_n \quad (9)$$

whereby Eq. (7) can be written

$$\begin{aligned} v(\tau) &= v_o(\tau) - \left(\frac{dv_o}{dt} \right)_\tau \int_0^\tau \frac{dv_n/dt}{dv_o/dt} dt \\ &\quad + \int_0^\tau \frac{dv_n}{dt} dt \end{aligned} \quad (10)$$

The quantity of interest is $\Delta v \equiv v(\tau) - v_o(\tau)$ which represents the difference in final voltage which results from $v_n(t)$. From Eq. (10)

$$\Delta v = \int_0^\tau \left[1 - \frac{(dv_o/dt)_\tau}{(dv_o/dt)} \right] \frac{dv_n}{dt} dt \quad (11)$$

Equation (11) can be used to determine the frequency response of the floating diffusion input. Let us assume that $v_n(t)$ is of the form

$$v_n(t) = V_n e^{i2\pi ft} u_{-1}(t) \quad (12)$$

where V_n is the complex amplitude of the input noise or signal voltage at frequency f and $u_{-1}(t)$ is the unit step at $t = 0$. Inserting Eq. (12) into (11) and assuming that $(dv_o/dt)_\tau \ll (dv_o/dt)_{t=0}$ gives

$$\Delta v = V_n \left\{ 1 + \int_0^\tau \left[1 - \frac{(dv_o/dt)_\tau}{(dv_o/dt)} \right] s e^{st} dt \right\} \quad (13)$$

where the shorthand $s \equiv i2\pi f$ has been used.

In order to proceed further with the evaluation of Eq. (13), equations for $v_o(t)$ must be used. Two cases will be considered.
1) The case where τ is so short that the above-threshold transistor equation⁹ describes the spill transient.

$$I_D(t) = \frac{\beta}{2} (V_{in} - V_t - v(t))^2 \quad (14)$$

In this expression

$$\beta \equiv \frac{W}{L} C_{ox} u \quad (15)$$

characterizes the transistor channel width W , channel length L , oxide capacitance per unit area C_{ox} and majority carrier mobility u .

2) The case where τ is so long that the transistor operates in the subthreshold regime during most of its spill transient. In this case the subthreshold transistor equation applies.¹⁰

$$I_D(t) = \beta \frac{1}{m} \left(\frac{n k T}{q} \right)^2 \exp \left[\frac{q}{n k T} (V_{in} - V_t - \frac{k T}{q}) - v(t) \right] \quad (16)$$

where m and n are capacitance ratios on the order of unity which are defined in Ref. 10.

Case 1 applies when

$$\tau < \frac{2C}{\beta} \frac{q}{nkT} \quad (17)$$

and case 2 applies when

$$\tau \gg \frac{2C}{\beta} \frac{q}{nkT} \quad (18)$$

(See Ref. (11))

Case 1

Assuming Eq. (14) for the transistor drain current, the spill transient $v_o(t)$ can be calculated to be^{2,11}

$$v_o(t) = V_{in} - V_t - \frac{V_{in} - V_t - v_o(0)}{1 + \frac{\beta t}{2C} [V_{in} - V_t - v_o(0)]}, \quad (19)$$

which, apart from an initial transient, is approximately

$$v_o(t) = V_{in} - V_t - \frac{2C}{\beta t}, \quad (20)$$

from which

$$\frac{dv_o}{dt} = \frac{2C}{\beta t^2} \quad (21)$$

Inserting Eq. (21) into Eq. (13) gives

$$\Delta v = V_n \left\{ 1 + \int_0^\tau \left[1 - \frac{t^2}{\tau^2} \right] s e^{st} dt \right\} \quad (22)$$

which can be integrated to give the transfer function $H \equiv \Delta v/V_n$

$$H(s) = \frac{2}{s\tau} + \frac{2}{(s\tau)^2} (e^{-s\tau} - 1). \quad (23)$$

The magnitude of this function is shown in Figure 3 as a solid line.

Case 2

When the transistor is characterized by Eq. (16), the spill transient $v_o(t)$ is given by¹¹

$$v_o(t) = V_{in} - V_t - \frac{nkT}{q} + \frac{nkT}{q} \ln \left[\frac{\beta n k T}{C m q} (t - t_o) + 1 \right] \quad (24)$$

where t_o is the time at which the transistor enters the subthreshold regime, i.e., the time at which $v = V_{in} - V_t - nkT/q$. In this analysis it is assumed that $\tau \gg t_o$, and since the form of dv_o/dt is important only at large t , it is approximated by

$$\frac{dv_o}{dt} = \frac{nkT}{q} \frac{1}{t} \quad (25)$$

Inserting Eq. (25) into Eq. (13) gives

$$\Delta v = V_n \left\{ 1 + \int_0^\tau \left[1 - \frac{1}{t} \right] s e^{st} dt \right\} \quad (26)$$

from which $H(s)$ is determined to be

$$H(s) = \frac{1}{s\tau} (1 - e^{-s\tau}). \quad (27)$$

The magnitude of this is identical to the ideal integrator and is given by the dotted line in Figure 3.

Work is continuing to determine the range of signal amplitudes over which the above linearizations are valid. However, data in the following section support these results.

IV. EXPERIMENTAL RESULTS

A.) Experimental Setup. A schematic is shown in Figure 4 of the experimental setup used for measuring the small-signal frequency response and noise aliasing characteristics of the floating diffusion input.

The output of the CCD is a conventional preset or floating diffusion amplifier, buffered by a bipolar emitter follower. The output waveform is sampled-and-held by an Analog Devices SHA-2. The amplified output of the SHA-2 sample-and-hold circuit is fed into a Hewlett-Packard HP 302A wave analyzer for determination of the RMS level of signal and spectral intensity of noise. At the

input the option exists to apply either a small-signal sinusoid excitation (from the wave-analyzer oscillator) or a white noise voltage from a GR 1390B noise generator. The bandwidth of the applied noise is controllable using a KH 3550 tunable filter. Provisions are also made in the CCD clocking electronics to vary the effective integration, τ .

B.) Small-Signal Frequency Response. The data plotted in Figure 5 were obtained by biasing the input to approximately 50% full well and then modulating this charge level with peak-to-peak charge excursions of the order of 1% (or less) of a full well while varying the normalized integration time, τ/T_c . The clock frequency was 18 kHz. The data in its raw form does not readily indicate the frequency response of the input because of the $\sin x / x$ frequency response of the output due to the SHA-2 sample-and-hold circuit. The data was massaged by dividing through, point by point, by the measured frequency response of the SHA-2. The massaged data is shown plotted in Figure 6. For an effective integration time τ of 0.1 T_c , the input response was quite flat well beyond the clock frequency, f_c , in good agreement with the predictions of Figure 3.

For the case of $\tau = 0.9 T_c$, on the other hand, the small-signal response of the input was very nearly that of an ideal $\sin x / x$ integrator. This response is in good agreement with the subthreshold model depicted in Figure 3. From an aliasing standpoint, substantial aliasing would be anticipated for the case of $\tau = 0.1 T_c$, where $\tau = 0.9 T_c$ mode of operation should yield little or no aliasing.

C.) Noise Aliasing. To corroborate the aliasing conclusions based on the massaged small-signal data, the GR 1390B noise generator was connected to the input (See Figure 4). The raw data is shown in Figure 7. Although again the spectral intensity is effected by the output $\sin x / x$ at high frequencies, the aliasing properties can easily be inferred by the low frequency noise intensity. The lowest curve represents the inherent noise obtained with the GR 1390 cut off. The second lowest curve denoted by the solid dots was obtained with the KH 3550 upper cut off frequency set to the Nyquist frequency. The elevated noise indicated input-noise dominated performance.

Because of the bandlimiting of the 3550, however, no aliasing was present.

Coincident with the second lowest curve is shown a set of data points denoted by X's. These data were obtained with the KH 3550 bandwidth set at 20 times the Nyquist frequency (or 10 f_c) and with the integration time τ approximately 0.9 T_c . No increase in low-frequency noise was observed; i.e., no aliasing occurred. The two higher noise curves were obtained for smaller values of normalized integration time τ/T_c .

Figure 8 shows a normalized plot of noise data obtained at $f = 0.1 f_c$ for different values of normalized integration time τ/T_c . The dashed line is the theoretical aliasing factor, defined as the fractional increase in low frequency noise due to aliasing, as predicted by the above-threshold model of Figure 3. The data actually indicates better agreement with the sub-threshold model, consistent with the small-signal response data of Figure 6.

V. Conclusions

In summary, the small-signal frequency response analysis of section III predicted that substantial anti-aliasing performance may be realized using the floating-diffusion input. The data presented verified this prediction for practical conditions of operation. From an application standpoint, these anti-aliasing characteristics can be a valuable benefit, especially for high density applications where additional filter circuitry is undesirable. The results obtained are equally valid for all inputs incorporating the "fill-and-spill" or "potential equilibration" technique and are achievable while maintaining the high level of threshold voltage insensitivity characteristic of the input technique.

Some important work remains in exploring analytically and experimentally the range of signal amplitudes over which this band-limiting effect remains operative. Of equal importance is the determination of the effect on the anti-aliasing characteristic resulting from spurious voltage transients in a system, both coherent and random.

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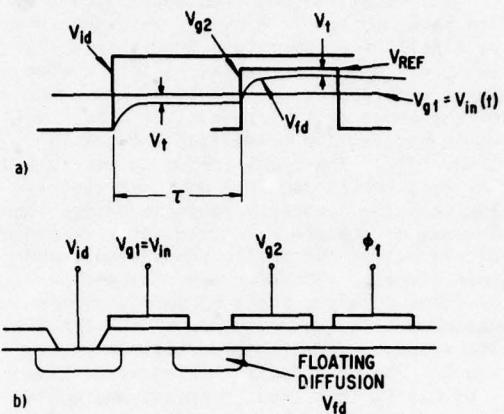


Fig. 1 FLOWING DIFFUSION INPUT
a) Waveforms
b) Structure

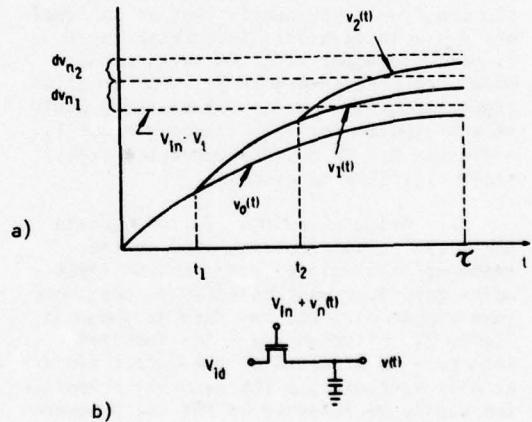


Fig. 2 MODEL FOR ANALYSIS OF SMALL-SIGNAL FREQUENCY RESPONSE OF FLOWING DIFFUSION INPUT
a) Transient "spill" curves
b) Circuit diagram

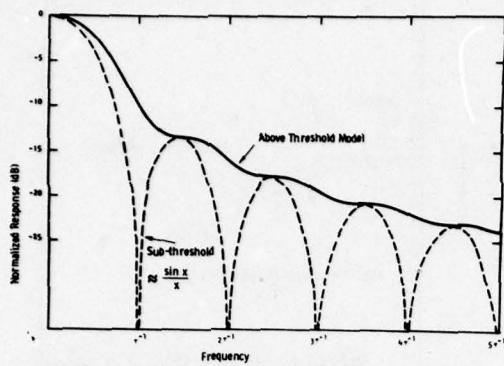


Fig. 3 CALCULATED FREQUENCY RESPONSE OF FLOATING DIFFUSION INPUT

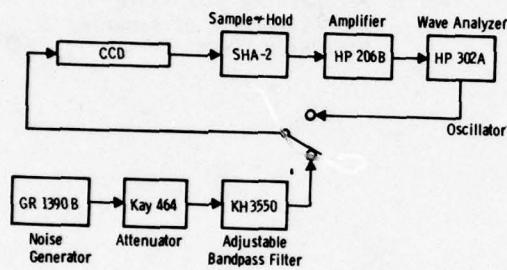


Fig. 4 EXPERIMENTAL SETUP FOR MEASURING FREQUENCY RESPONSE AND ALIASING CHARACTERISTICS



Fig. 5 MEASURED FREQUENCY RESPONSE OF CCD SYSTEM (INCLUDES $\sin x$ OF SAMPLE AND HOLD)

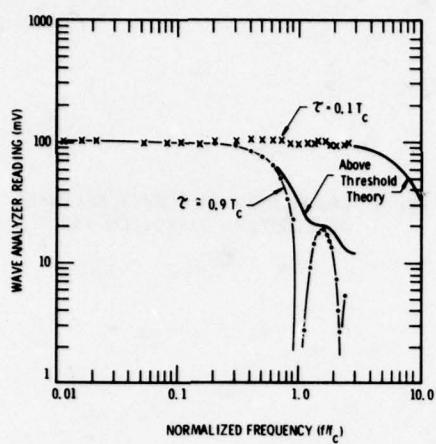


Fig. 6 REPLOTTED FREQUENCY RESPONSE WITH SAMPLE AND HOLD ($\sin x/x$) EFFECT REMOVED

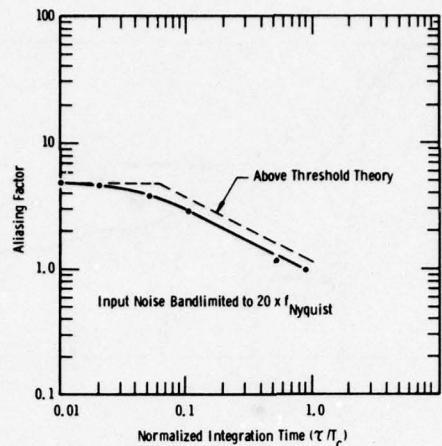


Fig. 8 MEASURED ANTI-ALIASING CHARACTERISTIC OF FLOATING DIFFUSION INPUT

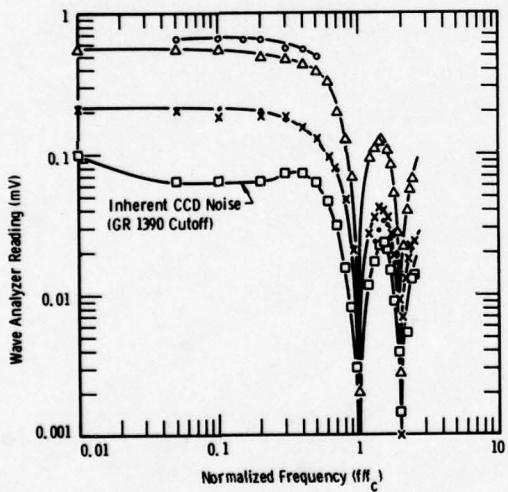


Fig. 7 MEASURED SPECTRAL INTENSITY OF NOISE VOLTAGE AT WAVE ANALYZER (INCLUDES $\sin x/x$ OF SAMPLE AND HOLD)

LIMITATIONS OF A THRESHOLD-INSENSITIVE CCD INPUT TECHNIQUE IN
A TOTAL DOSE RADIATION ENVIRONMENT

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ABSTRACT. The sensitivity of the potential equilibration input method to flat-band voltage shifts has been investigated. The conditions required for proper operation of the technique have been used to predict the magnitude of the flat-band voltage shift that can be accommodated. The effect of gamma irradiation on the device transfer characteristics was determined. The experimental threshold shift tolerance is compared to the predicted behavior. The trade-offs involved in maximizing the threshold shift accommodation are discussed.

INTRODUCTION

Characteristics such as low cost, small size, low power, and high reliability make charge-coupled devices (CCD's) especially attractive for certain space and military applications if the devices can be made sufficiently tolerant of radiation environments. Experiments performed on several types of buried channel devices have shown that the charge transfer process itself is fairly insensitive to irradiation produced interface state trapping and flat-band voltage shifts in devices having the "proper" structure.¹ Buried channel devices have been operated with acceptable transfer efficiencies after exposure to gamma doses greater than 10^6 rads.² One of the major obstacles to the use of CCD's in irradiated systems is the sensitivity of the electrical input to flat-band voltage shifts. Even if "hard oxide" techniques can be employed in the fabrication of CCD's, a flat-band voltage shift of about 1v will have to be accommodated at 10^6 rads for the most favorable bias condition.³

POTENTIAL EQUILIBRATION INPUT TECHNIQUE

The "potential equilibration input technique", also known as "spill and fill" or "charge extraction", was developed as a low noise CCD input.^{4,5,6} This method has the property of being independent of the

flat-band voltage if the flat-band voltages of the input gate and the first transfer gate are equal.

The manner in which the potential equilibration input technique was operated on the test devices is shown in Fig. 1. The input diode (ID) is pulsed to a low value, VIDL, when the voltage on the first two transfer gates P1 and P2 is high, injecting charge into the well under P1 and P2. While both transfer gates are still high, the diode voltage is returned to its high level, VIDH, pulling the excess charge from under these electrodes. The amount of charge retained under the first two electrodes is proportional to the difference in the channel potentials under these electrodes and the input gate (IG). It was necessary to use the first two transfer gates since the first P1 gate is much narrower than the remaining transfer gates on this particular device. Hence, very little charge could be held under it. See Fig. 2. A typical transfer curve for the 150 bit buried channel test device is shown in Fig. 3. The threshold insensitive region of operation is indicated.

PREDICTED FLAT-BAND SHIFT EFFECTS

As a first order approximation the amount of signal charge injected into the CCD will

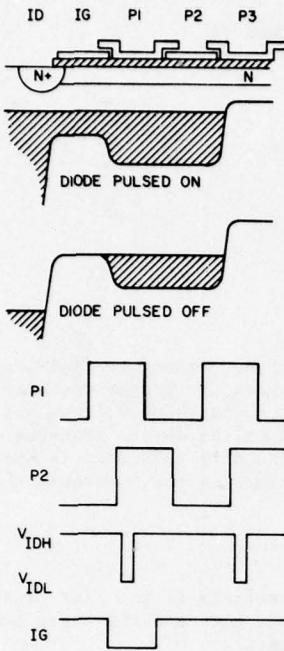


Fig. 1 Schematic cross-section of the buried channel shift register with the buried channel potential profile and the waveforms employed in the potential equilibration method.

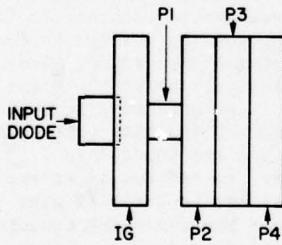


Fig. 2 Schematic top view of the shift register input structure.

be insensitive to flat-band voltage shifts of equal magnitude under the input and first transfer gates, provided that the conditions for proper operation of the potential equilibration input technique remain satisfied.⁷ Expressed in the notation of Fig. 1 these

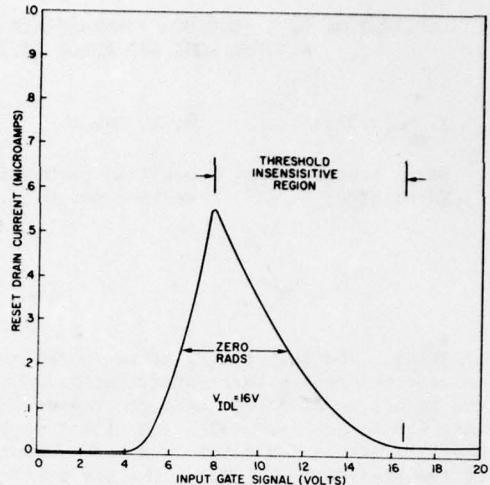


Fig. 3 Transfer curve for the potential equilibration input technique.

conditions for a buried channel device are

$$\begin{aligned} \phi_{IGL} &> V_{IDL}, \quad \phi_{P1H} > \phi_{IGH}, \\ V_{IDL} &> \phi_{P1L}, \quad V_{IDH} > \phi_{IGH}. \end{aligned} \quad (1)$$

where ϕ_{nL} and ϕ_{nH} are the maximum potentials in the buried channel when the voltages on the n'th gate are respectively low and high.

These inequalities may not be satisfied after irradiation since the channel potentials, ϕ , are a function of the flat-band voltage while the diode voltages, V , obviously are not. These inequalities can be used to predict the maximum flat-band voltage shift which the potential equilibration input can tolerate for a fixed set of pre-irradiation clock and bias voltages. In the case of the n-channel buried channel test device, only the last two inequalities can be upset by the irradiation produced flat-band voltage shift. The one dimensional solution to Poisson's equation for a buried channel device with a constant channel doping density was used to determine the channel potential maximum.⁸ The pre-irradiation value of the terms in these inequalities, listed in (2a) and (2b), were calculated using the operating clock and bias voltages.

$$V_{IDL} = 16v > \phi_{PIL} = 11.6v \quad (2a)$$

$$V_{IDH} = 40v > \phi_{IGH} = 24.3v \quad (2b)$$

From (2a) it is seen that when the channel potential under P1 changes by +4.4v, the inequality will no longer be satisfied. A change in channel potential of 4.4v for this device would result from a flat-band voltage shift of -4.7v. In order to increase the magnitude of the flat-band voltage shift for which the inequality will remain satisfied one can either increase V_{IDL} or decrease ϕ_{PIL} . However, the maximum signal charge, Q_{max} , that can be injected is reduced for both options, since

$$Q_{max} \propto \phi_{P1H} - V_{IDL} \quad (3)$$

and $\phi_{P1H} - \phi_{PIL}$ is fixed for a given clock swing. Of course, increasing the clock swing allows a greater flat-band voltage shift to be accommodated for a given maximum signal capability.

Up to this point it has been assumed that the flat-band voltage shifts under the input and first transfer gates are identical. This assumption is reasonable if the oxide structure and the electric field in the oxide beneath both the input gate and first transfer gate are identical. The voltage drop over the oxide, V_{ox} , in an empty buried channel device is given by⁹

$$V_{ox} = \frac{-qN_D d}{\epsilon_{ox}} \left[t - \phi_c^{\frac{1}{2}} \left(\frac{2N_A \epsilon_s}{qN_D^2} \right)^{\frac{1}{2}} \right] \quad (4)$$

where $q = 1.6 \times 10^{-19}$ C, N_D is the channel doping density, d is the oxide thickness, ϵ_{ox} is the dielectric constant of the oxide, t is thickness of the buried channel, N_A is the substrate doping density, ϵ_s is the dielectric constant of the silicon and ϕ_c is the channel potential at the p-n junction. ϕ_c is related to the maximum channel potential by

$$\phi_{max} = \phi_c (1 + \frac{N_A}{N_D}) \quad (5)$$

The greatest difference in the potentials under the input and first transfer gates occurs when the first transfer gate returns to its low value (in this case 1v), while the input gate is biased for zero signal

(in this case approximately 16v). The voltage drops across the oxide for this worst case are -5.3v for the +16v gate and -5.8v for the +1v gate. Since the gate is biased negatively with respect to the channel and the difference in the fields under the input and first transfer gates is small, the flat-band voltage shifts for these adjacent gates should be approximately the same. However, even small differences in the flat-band voltage shifts will result in an approximately parallel shift of the post irradiation curve in the operating region.

EXPERIMENTAL DETAILS

The test device was a 150 bit, four phase, n-buried channel shift register with an aluminum-anodized aluminum-aluminum double-level metallization.¹⁰ The gate oxide was 1000 Å and the channel depth was either 1000 Å or 6000 Å. The implanted dose was $1.5 \times 10^{12} \text{ cm}^{-2}$ phosphorus. The resistivity of the <100> orientation substrates was 10 to 70 ohm cm. The transfer gates were 30.5 micrometers long and 127 micrometers wide.

The shift registers were operated using the double clocking scheme at 500 kHz.¹¹ The clock swing was from 1 to 16V with a 50% duty cycle. The buried channel was kept depleted by applying 26.4v to the reset drain. The reset pulse swing was from 0 to 8v. The on-chip output amplifier was operated as a source follower with a drain voltage of 41v. The 10 kilohm source follower resistor was connected to +11v. The substrate was held at 0v. The output gate voltage was +4v.

The potential equilibration input was characterized by means of a transfer curve. An electrometer was inserted in the reset drain line and its output was fed into the Y axis of an XY recorder. The input gate voltage was applied to the X axis. The reset drain current was measured to avoid the effects of the radiation on the output amplifier. All transfer curves were taken with $V_{IDH} = 40v$ and $V_{IDL} = 16v$.

Four devices were irradiated in the NRL Cobalt 60 gamma ray source while being operated as shift registers with normal clock and bias voltages. The input gate was held at +15v during the irradiation except when a burst of eight full well signals were inserted every 256 clock

periods as a check for proper operation of the device. Transfer curves were taken after each dose increment. The displacement effects due to increased output diode leakage and dark current were subtracted out. The highest dose rate employed was 4.4×10^3 rads (Si) per minute.

EXPERIMENTAL RESULTS AND DISCUSSION

A series of potential equilibration input transfer curves were taken prior to irradiation in which a flat-band voltage shift was simulated by applying positive offset voltages to all the CCD gates. In the operating region the transfer curves were insensitive to offset voltages of up to +4v.

The transfer curves for the potential equilibration input as a function of total dose are shown in Fig. 4.

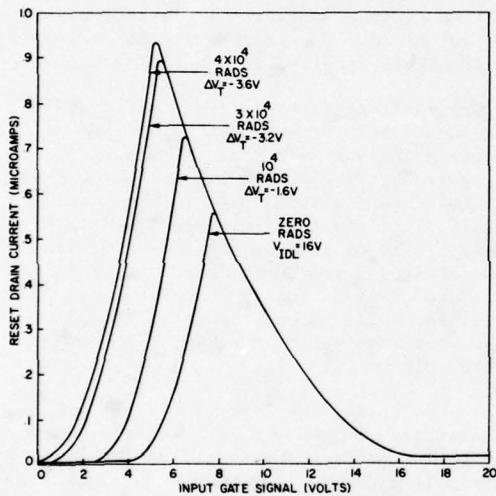


Fig. 4 Potential equilibration input transfer curves as a function of total dose.

The signal charge injected for a given gate voltage was insensitive to threshold voltage shifts up to -3.6v (4×10^4 rads Si). The increase in the maximum charge handling capability of the input as a function of dose can be explained by referring to equation (3). The flat band voltage shift increases the channel potential ϕ_{PL} and decreases the gate voltage for which

$\phi_{IGL} = V_{IDL}$. The threshold voltage shifts were obtained from the dynamic current injection input transfer curves shown in Fig. 5.

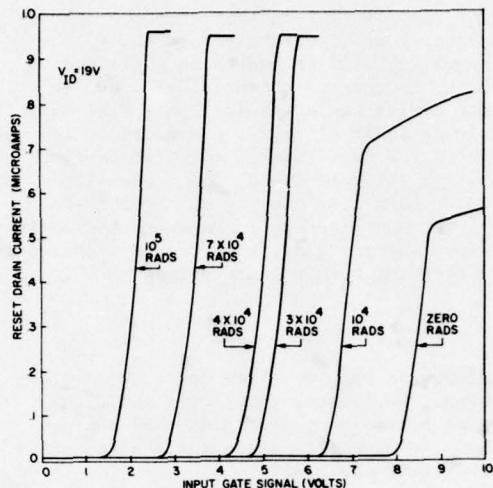


Fig. 5 Dynamic current injection input transfer curves as a function of total dose.

Threshold shifts of less than one volt caused the dynamic current injection transfer curve to be shifted completely out of the pre-irradiation operating range while the potential equilibration input characteristics remained unchanged even after a -3.6v threshold shift. Experimentally it has been observed that the threshold voltage shifts measured by the dynamic injection input are approximately equal to the flat-band voltage shifts measured by the 1MHz CV technique, for a buried channel device.¹² At 7×10^4 rads, the threshold voltage shift was -5.1v, making ϕ_{PL} equal to 16.6v. As expected, the transfer curve for $V_{IDL} = 16v$ shown in Fig. 6 no longer falls on the pre-irradiation curve for high gate voltages. The predicted threshold shift tolerance (-4.7v), falls within the range of the observed values (-3.6v to -5.1v). If the inequality $V_{IDL} > \phi_{PL}$ is restored by increasing V_{IDL} to +17v, the post irradiation curve is brought more nearly into coincidence with the zero rad curve. See Fig. 7. The effect of not satisfying the condition $V_{IDL} < \phi_{PL}$ is further illustrated in Fig. 8.

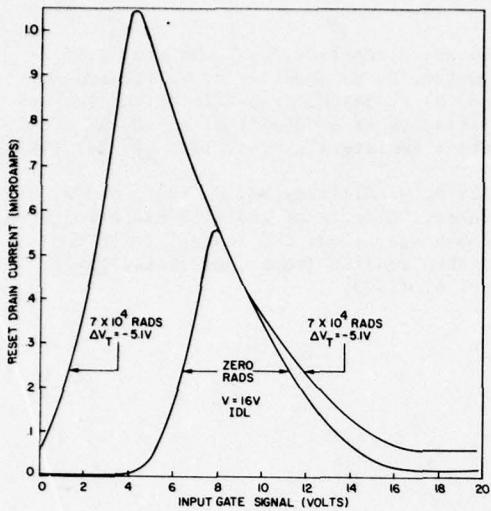


Fig. 6 Comparison of the potential equilibration input transfer curves at zero rads to the curve at 7×10^4 rads.

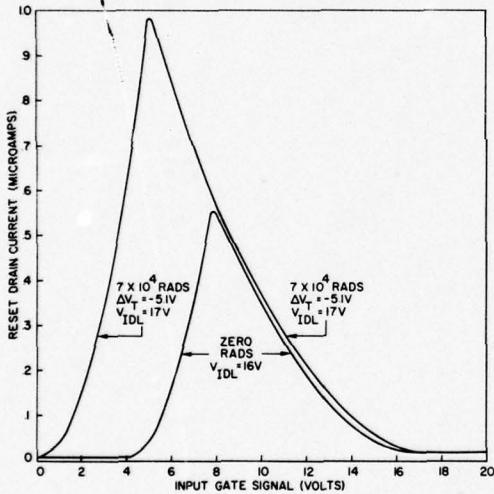


Fig. 7 Comparison of transfer curve at zero rads with $V_{IDL} = 16v$ to the curve at 7×10^4 rads with $V_{IDL} = 17v$.

At 10^5 rads Si ($\Delta V_T = -6.5v$), ϕ_{PLL} has a value of 17.4v and the input characteristics are severely distorted for $V_{IDL} = 16v$.

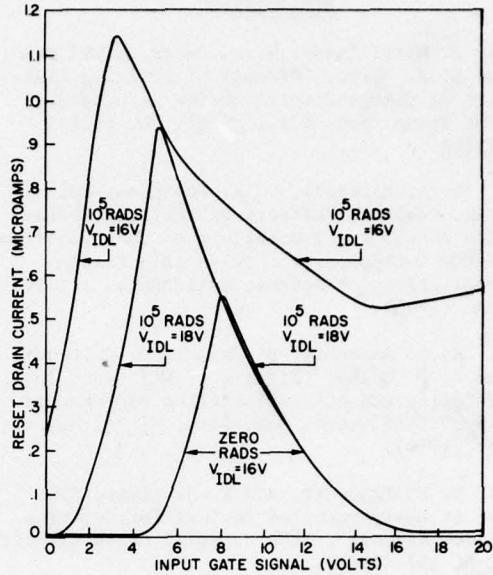


Fig. 8 Comparison of transfer curves at 10^5 rads (Si) as a function of V_{IDL} to the zero rad curve.

Increasing the input diode low voltage to +18v restores the transfer curve to its pre-irradiation value in the operating region. The tradeoff involved in using a larger input diode low voltage to increase the threshold voltage is a reduced signal handling capability. At zero rads the maximum signal for $V_{IDL} = 18v$ was 65% of the 7×10^6 electron capacity for $V_{IDL} = 16v$.

CONCLUSIONS

The potential equilibration input has been shown to be insensitive to irradiation produced input threshold voltage shifts of equal magnitude under the input and first transfer gates provided that the conditions for the proper operation of the input remain satisfied. If CCD's can be fabricated with hardened oxides, this input method would be insensitive to the flat-band voltage shift produced by a megarad dose.

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RADIATION HARDNESS OF SURFACE AND BURIED CHANNEL CCDs*

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ABSTRACT. A series of radiation tests have been performed to determine the effects of gamma, pulsed electron beam, and neutron radiation on several variations of double level electrode surface and buried channel CCD structures. The test samples were characterized in terms of leakage current, well capacity, noise spectrum, and linearity of the CCDs and plus leakage, capacitance, and threshold voltage of MOSFETs and gated diodes on the CCD chip before and after exposure. The latest group of tests included: 1) Neutron total fluence effects tests at levels of 10^{11} to 10^{13} neutrons/cm². 2) Total gamma dose effects tests at dose levels of 10^4 to 3×10^6 rad from Co⁶⁰. 3) Low rate gamma response tests at rates of 5 to 100 rad/sec. 4) High dose rate pulse survival and recovery time tests using 100 ns Linac electron beam pulses at dose rates of 10^9 to 10^{11} rad/sec. The results to date from examination of the test data are reported. Results from these tests include a comparison of the gamma total dose effects on aluminum gate and poly-silicon gate devices, neutron total dose effects, and photo current generation rates for Co⁶⁰ gamma radiation.

INTRODUCTION

Many military and space applications of CCDs will require operation in nuclear radiation environments. A series of radiation tests have been performed to determine the effects of total gamma dose, low dose rate gamma, high dose rate pulsed electron beam, and fission spectrum neutron radiation on several variations of double level electrode surface and buried channel CCD structures. Both aluminum gate and poly-silicon gate devices were included in the latest tests.

The CCD chip used for the test samples contains: (1) a 150 bit 40 overlapping gate CCD with a precharge diffusion/source follower output, (2) an MOS gated diode and capacitor (3) a short channel MOSFET, and (4) a field oxide MOSFET. The test samples included aluminum and polysilicon gate devices from the same processing lot, devices with gate oxide through which ions had been implanted and devices which had a new gate oxide grown after ion-implantation. The gate oxide for all devices was grown dry at 1000°C.

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Detailed electrical characterization of the test samples was done before and after irradiation on each sample. The measurements made are listed in Table I. The variation of CCD leakage with temperature for a typical device before irradiation was measured from -15°C to +75°C and found to vary linearly with temperature, doubling for approximately each 80°C temperature increase. Analysis of the measurement data after irradiation is still in progress. Descriptions of the radiation tests and the results obtained to date are discussed in the remainder of this paper.

NEUTRON EFFECTS TESTS

The neutron total fluence test exposures were made at the Fast Burst Reactor (FBR) at the Nuclear Effects Laboratory at White Sands Missile Range. The test levels were 1.3×10^{11} , 1.4×10^{12} , and 1.0×10^{13} neutrons/cm², and one-third of the test samples were exposed to each of the levels. The corresponding gamma

dose exposures were 40, 250, and 950 rad (Si). For the 10^{13} n/cm² exposure, a 10 cm thick lead shield was used to reduce the gamma dose level below 10^3 rad. Sulfur pellets were used for the neutron dosimetry and TLD-400 for the gamma dosimetry.

To reduce the effects of the small, unavoidable gamma exposure on the neutron test devices, all samples were irradiated under zero bias conditions. This was achieved by shorting the leads of the test samples together by means of a layer of conductive foam. This also protected the devices from any damage due to possible EMP effects during the reactor pulse transient.

Twenty-one test samples were used for the neutron tests, including nine SC aluminum gate samples, nine BC aluminum gate samples, and three SC polysilicon gate devices.

NEUTRON TEST RESULTS

The analysis of the neutron test results to date has shown no unexpected effects on CCD operation from neutron irradiation. As shown in Figure 1, the integrated CCD leakage current increases nearly linearly with increasing fluence in the 10^{11} to 10^{13} neutrons/cm² range. The leakage increased by approximately a factor of six for each decade increase in fluence for both BC and SC samples. The gated diode leakages as a function of gate voltage for these samples were examined to determine the source of this leakage increase. The changes of the bulk and surface components are plotted in Figure 2 for buried-channel samples and in Figure 3 for surface-channel samples. From these curves, it can be seen that the bulk component of leakage increases rapidly with neutron fluence, but the surface component increases only slightly. It is probable that the increase in surface component is due to the small gamma dose received with the neutron exposure. If the change in leakage with gamma dose shown in Figure 9 is extrapolated to lower dose levels, the values of surface leakage current obtained are of the same order as seen in Figure 2.

The changes in charge transfer inefficiency (CTI) with neutron fluence for typical SC and BC devices operated with fat zero are shown in Figure 4. For the 10^{13} n/cm² fluence samples it is seen that the CTI for BC devices is increased much more than for SC devices. This result, together

with the leakage current data, shows that the neutron irradiation produces mainly bulk crystal damage and causes relatively small amounts of oxide charge buildup and surface state increase. The threshold voltage shifts which were less than 0.5 volt also indicate that very little oxide charge increase was caused by the neutron irradiation. No significant differences have been seen between the aluminum gate and polysilicon gate samples in regard to the effects of neutron exposure.

LOW DOSE RATE GAMMA EFFECTS TESTS

The low dose rate gamma tests were made at the Co⁶⁰ gamma facility at Sandia Labs in Albuquerque. The minimum rate achievable with this source was 5 rad/sec, so the tests were made at dose levels of 5, 15, and 100 rad/sec, instead of the 1, 10, and 100 rad/sec levels originally planned. The dose rates were determined by TLD-400 dosimetry.

The samples used in these tests were six BC samples and six SC samples, including both aluminum and polysilicon gate devices. The samples were operated during irradiation in a test fixture that allows six test CCDs to be operated simultaneously. The clocks and input signals are provided to all six samples in parallel through coaxial cables from clock and signal generation electronics located outside the radiation chamber. The individual CCD outputs can be selected one at a time. The clock generator logic allows the test set to be operated in either the integrate and shift-out mode or the continuous clocking mode. For the gamma rate response tests, the samples were operated in the integrate mode with the integration time at each dose rate selected to provide an output signal large enough for accurate measurement, but not so large as to fill the well.

The results of these measurements are shown for three typical BC and three typical SC samples in Figures 5 and 6. These figures show the time required to completely fill the CCD well versus the dose rate. The times shown are extrapolated from the measured data. The variation between samples was due mainly to differences in full well capacity. Typical times range from 50 msec at 5.5 rad/sec to 5 msec at 100 rad/sec. This corresponds to generation rates of 3.1×10^{13} electrons/rad-cm³ at 5.5 rad/sec to 1.27×10^{13} electrons/rad-cm³ at 100 rad/sec, based on an

estimated collection volume of 7.86×10^{-7} cm³.

GAMMA TOTAL DOSE TESTS

The gamma total dose tests were also made using the Co⁶⁰ gamma facility at Sandia Labs. Dose rates used for the total dose test ranged from 100 to 230 rad/sec. Exposure levels were determined by TLD-400 and Cobalt Glass dosimetry. Table 2 summarizes the tests, showing the number and type of samples irradiated to each level and the dose levels at which data were taken for each group.

The same test set was used for these tests as was used for the low rate gamma test. During exposure, all the devices were run in the normal clocking mode with the common input level set so that all samples were operating at a charge level lower than full-well. The input level was set this way so that the BC units would be operating in the buried-channel mode, as is necessary to reduce oxide charge build-up effects. Any one of the six CCD outputs could be selected and observed by means of reed relay switches and a return cable driver in the test fixture. Before exposure and at each of the intermediate levels, the following CCD parameters were measured with the radiation off: (1) input diode threshold level, (2) charge transfer efficiency, (3) integrated CCD leakage current, and (4) output dc voltage level.

The CCDs were operated with normal bias and continuous clocking during irradiation. The clock voltage levels for all the active tests were 0 and +12 volts. For the other tests devices, the source and drain diffusions were reverse-biased with +20 volts, and a 0 to +12 volt 50% duty cycle pulse was applied to all gates except the gate of the field oxide transistor, which was connected to +28 volts.

GAMMA TOTAL DOSE TEST RESULTS

Analysis to date of the data from the post-exposure measurements of the gamma test samples showed that the results for BC devices are similar to those from the earlier tests. The most serious degradation from gamma radiation is the very large leakage current increase and the resulting reductions in storage time and dynamic range and increase in noise. One new result from these tests is that this leakage increase is

large even at low dose levels, as seen in Figure 7. The leakage for sample 130-4-89, which initially was 2.0 nA/cm², increased to 160 nA/cm² at 3×10^4 rad and to 385 nA/cm² at 10^5 rad. At the 10^6 rad level, the leakage was measured with the substrate voltage first at 0 volt as at the lower dose levels, and then at a positive substrate bias to reduce the potential difference between the channel and the channel stop. It can be seen that this reduced the leakage by nearly 50%. It was then decided to run the next group of samples at a positive substrate bias (relative to the low clock level) during exposure. The result of this change is illustrated by the curve for sample 130-4-88. The leakage current increase was significantly less at 3×10^4 and 10^5 rad, but at 3×10^5 rad and higher it was equal to the zero substrate bias case.

The limitations that leakage currents of this magnitude impose on a given system depend, of course, on the particular system requirements for storage time, dynamic range, and noise. However, the leakage levels seen even at 10^5 rad are too high for many applications. Figure 8 is a series of curves obtained by combining the measured effects of photocurrent resulting from a background level of gamma radiation and the leakage caused by the permanent damage effect of the accumulated gamma radiation dose. The curves give the calculated time to reach a level of 10% of full-well for a typical BC sample. That is, if a maximum leakage generated charge of 10% of a full signal charge is allowed, the times shown are the maximum time that a given information bit can be stored in the CCD. The 10% full-well criterion is too high for most analog applications, but might be allowable in a digital memory. For the case of zero background radiation, a dose of 10^6 rad reduces the storage time at room temperature from more than one second to 3.2 msec. At background radiation levels of about 15 rad/sec, the leakage due to photocurrent is about equal to that caused by 10^6 rad accumulated dose, and at higher background levels the photocurrent component is dominant.

The leakage current versus gate voltage characteristics of the gated diodes were studied to determine the source of this radiation-induced leakage. The typical variation of the surface and bulk components of leakage for these samples is shown in

Figure 9. Before irradiation, both components were about 1 pA, but after 10^5 rad the surface component had increased about 75 times, while the bulk component had only doubled.

The gated diode leakage vs gate voltage plots of Figures 10 and 11 show the very large increases in total leakage as the gate voltage goes positive that were seen on devices from the earlier tests. At the 3×10^6 level this leakage, which is thought to be due to breakdown caused by high surface fields at the channel stop junction, is so large that it nearly obscures the leakage step due to depletion of the surface. A more detailed investigation of the nature and cause of the effect is being performed.

The change in charge transfer inefficiency with gamma dose for these test samples was similar to earlier results. Figure 12 shows results for typical samples. Again, there was considerable variation from sample to sample in CTI, as in the last tests. The only difference seen so far between aluminum and polysilicon metallization is a larger V_T shift with the polysilicon gate for gamma radiation. For the gate oxide MOSFET after 10^6 rad the typical ΔV_T for aluminum was 2.5 volts, and for polysilicon it was 4.5 volts.

HIGH DOSE RATE IONIZING PULSE RECOVERY TESTS

The high dose rate ionizing pulse recovery tests were made on the Linac at WSMR operating in the direct electron beam mode. The tests were made in the same way as in the previous series, but the new test fixture permitted closer approach of the sample to the Linac exit window so that the maximum dose rate achieved was 10^{11} rad/sec. The electron energy was 20 MeV and the pulse width was 100 nsec. Series current-limiting resistors of 100 to 200 Ω were placed in each of the CCD supply leads.

Seven samples were tested, including surface and buried-channel devices and aluminum and silicon gate devices. The test data have not yet been completely analyzed, but no evidence has been found of the thermal damage that was seen in the previous test when no current-limiting resistors were used. The time required for the output circuit to return to normal operating levels and to remove the full wells of photo current from the CCD channel was from 250-300 μ sec at a clock rate of 1 MHz.

SUMMARY OF RESULTS TO DATE

The main effect of neutron exposure in the 10^{11} to 10^{13} neutrons/cm² range is an increase in the bulk component of leakage, which apparently is due to lattice displacement damage. Above 10^{12} neutrons/cm² this damage also significantly degrades the charge transfer efficiency of buried-channel CCDs.

Photon-generated charge from continuous gamma radiation was found to fill the wells of BC devices in times ranging from about 50 msec at 5.0 rad/sec to 5 msec at 100 rad/sec.

The total gamma dose effects results that have been analyzed are similar to those from earlier tests, with the new result that the surface leakage buildup is large enough to seriously affect storage times even at doses as low as 3×10^4 rad. The recovery times seen in the high dose rate transient tests were from 250 to 300 μ sec for a clock rate of 1 MHz. By use of current-limiting resistors, thermal damage from photocurrent can be prevented for dose rates up to at least 10^{11} rad/sec for 100 nsec pulses.

The only significant difference found between aluminum and polysilicon gates is a larger threshold voltage shift with polysilicon from gamma dose effects.

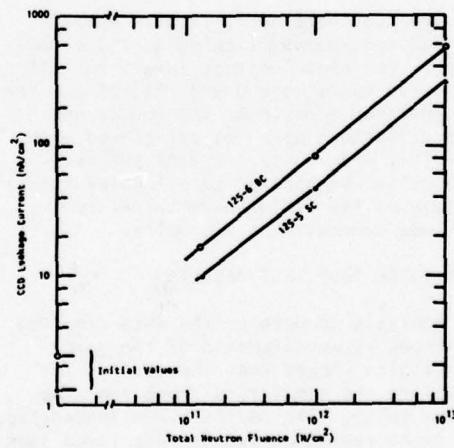


Figure 1 Typical CCD Integrated Leakage vs Neutron Fluence

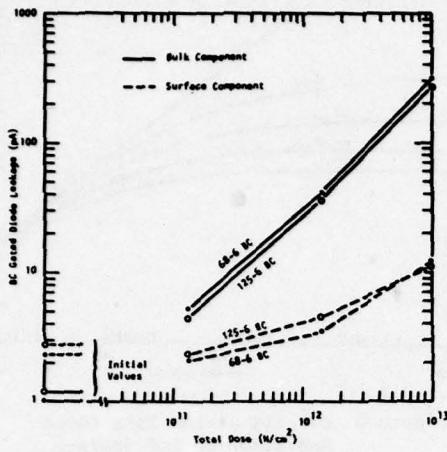


Figure 2 BC Gated Diode Leakage vs Neutron Fluence

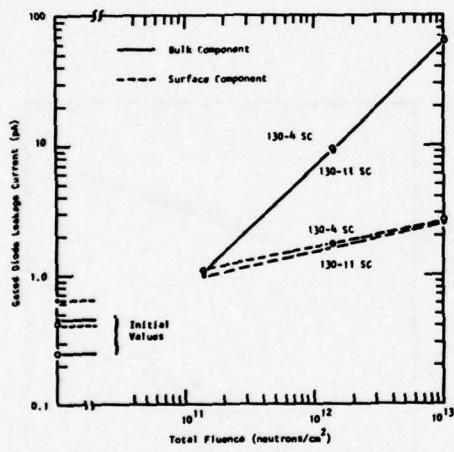


Figure 3 SC Gated Diode Leakage vs Neutron Fluence

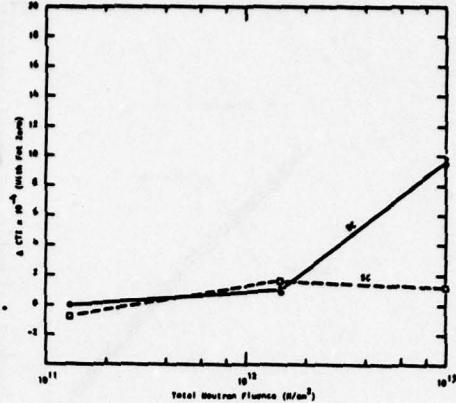


Figure 4 Change in Charge Transfer Inefficiency (CTI) with Neutron Fluence for Typical Surface- and Buried-Channel CCDs

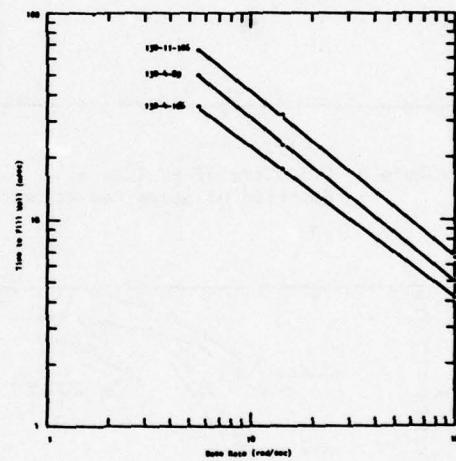


Figure 5 Fill Time of BC CCDs as a Function of Gamma Radiation

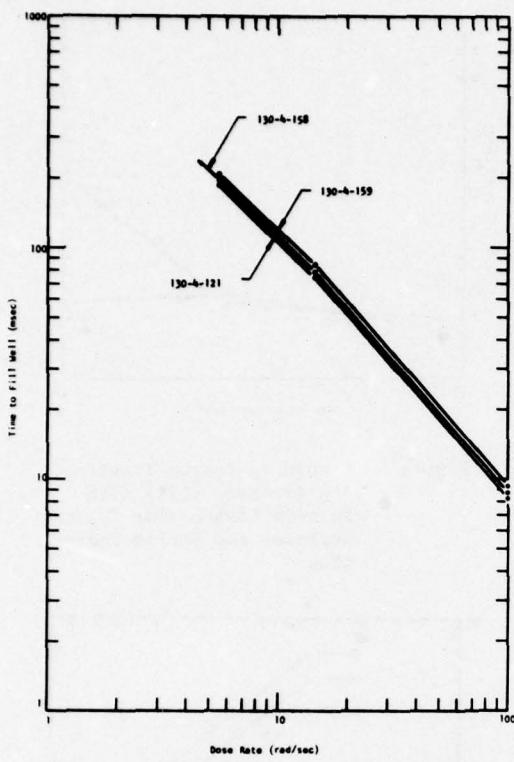


Figure 6 Fill Time of SC CCDs as a Function of Gamma Radiation

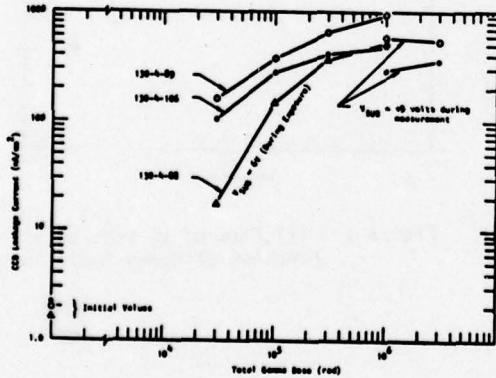


Figure 7 Typical Buried Channel CCD Leakage vs Gamma Dose

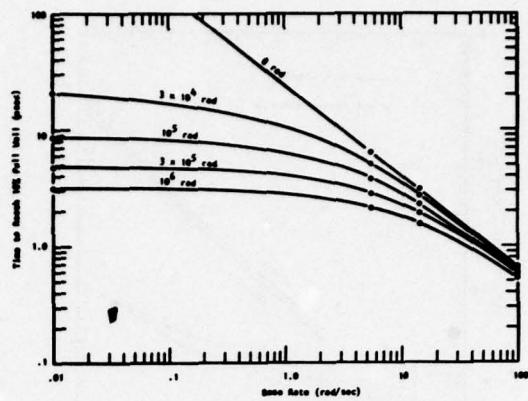


Figure 8 Effects of Low Rate Gamma Radiation on CCD Storage Time After Various Total Dose Levels

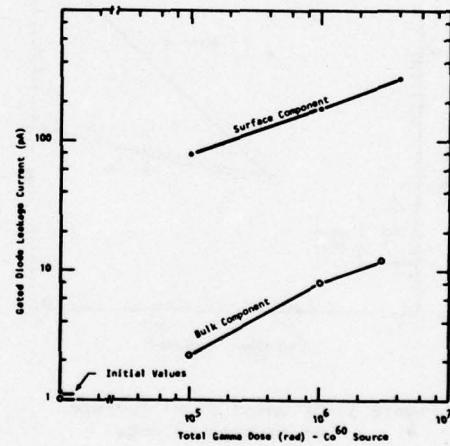


Figure 9 Graph of Bulk and Surface Components of Gated Diode Leakage vs Gamma Dose for BC Samples

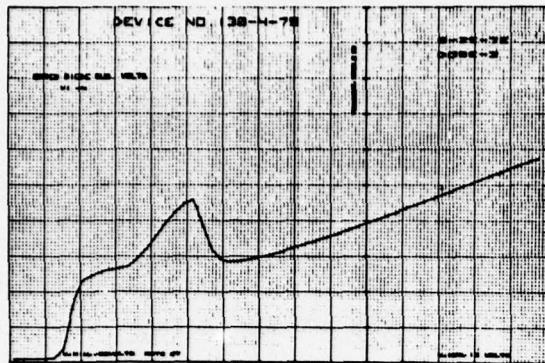


Figure 10 Plot of Gated Diode Leakage vs Gate Voltage for BC Sample After 10^6 Rad. Vertical scale is 100 pA/mark; horizontal scale is 2.0 volts/mark.

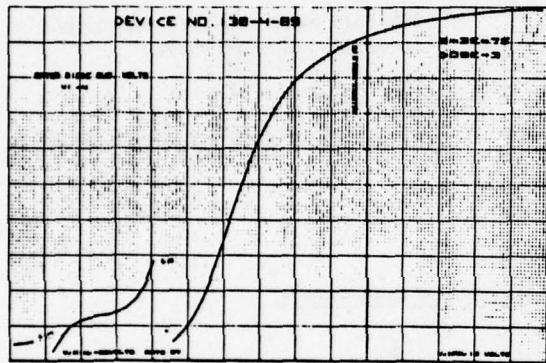


Figure 11 Plot of Gated Diode Leakage vs Gate Voltage for BC Sample After 3×10^6 Rad. Vertical scale is 25,000 pA/mark for $V_G > 11$ volts, 2500 pA/mark for 11 volts $< V_G < 18$ volts, and 250 pA/mark for $V_G < 18$ volts. Horizontal scale is 2.0 volts/mark.

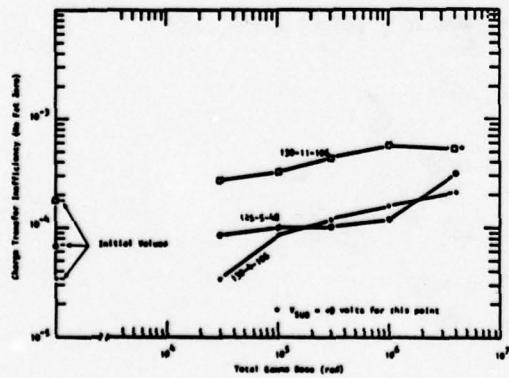


Figure 12 Charge Transfer Inefficiency vs Gamma Dose for Typical BC CCDs

TABLE 1
Test Sample Characterization

<u>Measurement</u>	<u>Test Device</u>	<u>Parameters Sought</u>
Integrated Leakage Current	CCD	CCD Leakage Current
Leakage Versus Gate Voltage	Gated Diode	MOS Capacitor I_L , T_{Bulk} , S_0 , and N_{SS}
Charge Transfer Efficiency	CCD	No Fat Zero CTE, Fat Zero CTE
Channel Current Versus Gate Voltage	CCD	Surface and Bulk Mobility
Threshold Voltage	CCD and MOSFET	V_T and Q_{SS}
Harmonic Distortion	CCD	CCD Linearity
Output Detector Current/ Voltage	CCD	CCD Full Well Capacity and Output Detector Transfer Curve
Output Noise Versus Frequency	CCD	Spectral Noise Density
Diode C-V	Gated Diode	Pinch-Off Voltage and Oxide Thickness

TABLE 2
Summary of Gamma Total Dose Test Units and Dose Levels

<u>Total Dose (rad)</u>	<u>Test Samples</u>	<u>Data Points (rad)</u>
3×10^6	4 Al Gate BC 2 Si Gate BC	$0, 3 \times 10^4, 10^5, 3 \times 10^5, 10^6, 3 \times 10^6$
10^6	4 Al Gate BC 2 Si Gate BC	$0, 3 \times 10^4, 10^5, 3 \times 10^5, 10^6$
10^5	4 Al Gate BC 2 Si Gate BC	$0, 10^5$
10^6	4 Al Gate BC 2 Si Gate BC	$0, 10^6$
10^5	3 SC	$0, 10^5$
3×10^5	3 SC	$0, 3 \times 10^5$
10^4	3 SC	$0, 10^4$

LOW TEMPERATURE SILICON CCD OPERATION

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ABSTRACT. Experimental results are presented on the operation of bulk (peristaltic) and surface channel silicon CCD's at cryogenic temperatures. The transfer inefficiency of both devices exhibited a similar pattern as a function of temperature between 300°K and 30°K, namely a broad curve with a minimum around 77°K. At that temperature the transfer inefficiency per cell of the two devices was measured to be $\epsilon_{(PCCD)} = 5.5 \times 10^{-4}$ and $\epsilon_{(SCCD)} = 4 \times 10^{-4}$. The bulk channel CCD exhibited a sharp transition in transfer inefficiency at the onset of freeze-out, increasing from $\epsilon = 1 \times 10^{-3}/\text{cell}$ at 30°K to $\epsilon = 1 \times 10^{-2}$ at 18°K and then leveling off to $\epsilon = 2 \times 10^{-2}$ at 4.8°K. The surface channel CCD did not show a freeze-out transition in transfer inefficiency, rather it increased slowly to a value of $\epsilon = 1.4 \times 10^{-3}$ at 5°K.

I. INTRODUCTION

The low temperature operation of silicon charge coupled devices, in the range between 5°K and 80°K, is a critical factor in the utilization of CCD's in infrared systems [1]. The temperature of operation of Infrared Charge Coupled Devices (IRCCD) is a function of a number of factors: the type of CCD, the wavelength region of interest, the IR detector material, the sensitivity requirements, etc.

Infrared CCD's (IRCCD's) fall into two categories: monolithic and hybrid. The monolithic IRCCD concept generally uses the standard CCD structure with the substrate consisting of a narrow bandgap or an extrinsic semiconductor sensitive to IR radiation. In the extrinsic semiconductor substrate case the photogeneration is an extrinsic process where only the majority carriers are mobile. The temperature of operation must, therefore, be kept in the neighborhood of freeze-out or below to minimize the dark current. With silicon being used for the substrate, that temperature can vary depending on the wavelength region of interest from 15°K for Si:As with $\lambda_{co} \approx 24 \mu\text{m}$ to 50°K for Si:In with $\lambda_{co} \approx 8 \mu\text{m}$. The CCD operation in this case can be either in the accumulation

mode [2] if the same elements are used for detection and readout or inversion mode if the detection and readout functions are separated but still integrated on the same chip.

The hybrid IRCCD consists of the coupling of any one of various types of IR photo-detectors to a silicon CCD shift-register unit. In the hybrid structure, the functions of detection and signal processing are performed in distinct but integrable components. The role of the silicon CCD in this case is that of a signal processor performing appropriate functions, such as multiplexing, amplification, correlation, delay-and-add, etc. The temperature of operation is once again dictated by the detector requirements and could fall anywhere from 5°K to ~ 200°K.

Since on the one hand the great majority of detectors are operated at ~ 80°K or below and on the other hand the most important questions to be resolved lie in the operation in the freeze-out region, we have concentrated our investigation of the low temperature CCD operation to the 5°K to 80°K temperature range.

II. DEVICE STRUCTURE AND OPERATION

Both bulk channel and surface channel CCD's were investigated. The epitaxial bulk (peristaltic) channel CCD (PCCD) [3], [4] with its high frequency of operation is of great interest for large IR focal plane arrays where a high data rate is required for the readout of all detectors in one frame time. The PCCD used is an n-channel epitaxial ion implanted device of 130 cells with an $0.8 \times 10 \text{ mil}^2$ cell size (see Fig. 1). The p-type substrate has a doping of $5 \times 10^{14}/\text{cm}^3$ and the $5 \mu\text{m}$ thick epitaxial layer is doped at $1 \times 10^{15}/\text{cm}^3$. The driving gate system consists of a two-level overlapped Al structure with a silox intergate isolation layer. A cross-section of the device is shown in Fig. 2. The high frequency room temperature operation of this device is discussed by Y. T. Chan et al [4], who report a present high frequency limit of 105 MHz.

The surface channel CCD (SCCD) is a p-channel device [5] with 100 cells and 8 input taps spaced every 12 cell, as shown in Fig. 3. The taps are designed for the coupling of IR detectors in a hybrid IRCCD structure. The channel width is 2 mils and the cell size $1 \times 2 \text{ mils}^2$. The gate structure is the same as for the PCCD described above, namely two-layer overlapping Al gates. The substrate doping is $\sim 1 \times 10^{15}/\text{cm}^3$.

III. EXPERIMENTAL RESULTS

For the low temperature operation, the devices were placed inside a dewar and connected via an "umbilical" cord to a rack containing the CCD electronics (see Fig. 4). The operating temperature was varied through the use of refrigerants with different boiling points (helium, neon, and nitrogen) and a heater located on the cold finger. The temperature was monitored with a calibrated temperature sensitive resistor. The operating voltages for either devices did not change greatly with temperature, the only exception being the output reset FET which below freeze-out required considerably greater bias voltages to reset properly. For comparison purposes, both CCD's were operated at the same clock frequency, $f_c = 10 \text{ KHz}$.

The transfer inefficiency per cell of the PCCD is plotted as a function of temperature in Fig. 5. At 300°K the transfer

inefficiency per cell of this particular PCCD was $\epsilon = 1.2 \times 10^{-3}$. It should be pointed that since our investigation was of a general nature, no effort was made to choose devices with maximum performance [6]. At liquid nitrogen temperature, 77°K , the transfer inefficiency has decreased to $\epsilon = 5.5 \times 10^{-4}$. For temperatures between 77°K and 30°K , the pattern is reversed with the transfer inefficiency now slowly increasing with decreasing temperature. At 30°K the transfer inefficiency is $\epsilon = 1 \times 10^{-3}$, which is approximately the same value as at room temperature. Below 30°K , the transfer inefficiency increases abruptly, an order of magnitude over a range of ten degrees to $\epsilon = 1 \times 10^{-2}$ at 18°K . Finally, below 18°K , ϵ continues to increase but much more gradually and it approaches what appears to be a saturation level of 2×10^{-2} at 4.8°K .

The major factor contributing to the transfer inefficiency of a peristaltic CCD are the bulk traps [7]. To measure the trap emission time constant charge is first introduced into the CCD to fill all the traps. A second charge packet is introduced after a variable time interval, Δt . The output corresponding to the second packet will be a function of the number of traps empty at time Δt and thus capable of capturing charge: $A = A_0 e^{-\Delta t/\tau_e}$. The output signals for various time intervals are shown in Figure 6 (left hand axis) for the PCCD operated at 80°K and clocked at 10 KHz. The trap emission time constants are obtained by plotting $\ln(A_0/A)$ vs Δt on the same graph (right hand axis). A value for A_0 of 55 mV is obtained by extrapolating the curve to the origin. A time constant with an apparent value of 0.26 mV is calculated from the data. At room temperature, only one time constant was found [4] with a value of 0.55 ms was found for the same device.

The transfer inefficiency of the SCCD is shown as a function of temperature in Fig. 6. Between 300°K and 30°K , the general behaviour is very similar to that of the PCCD with an apparent minimum of $\epsilon = 4.5 \times 10^{-4}$ at 77°K . However, below 30°K the SCCD does not exhibit the same transition region shown by the PCCD at the onset of freeze-out. Rather only a gradual increase in transfer efficiency is observed to 5°K where $\epsilon = 1.4 \times 10^{-3}$.

In conclusion, both bulk channel and surface channel CCD's have been shown to operate at temperatures as low as 5°K.

The author would like to thank R. A. Stacey and L. Nash for performing the measurements and R. D. Williams, B. T. French and Y. T. Chan for useful discussions.

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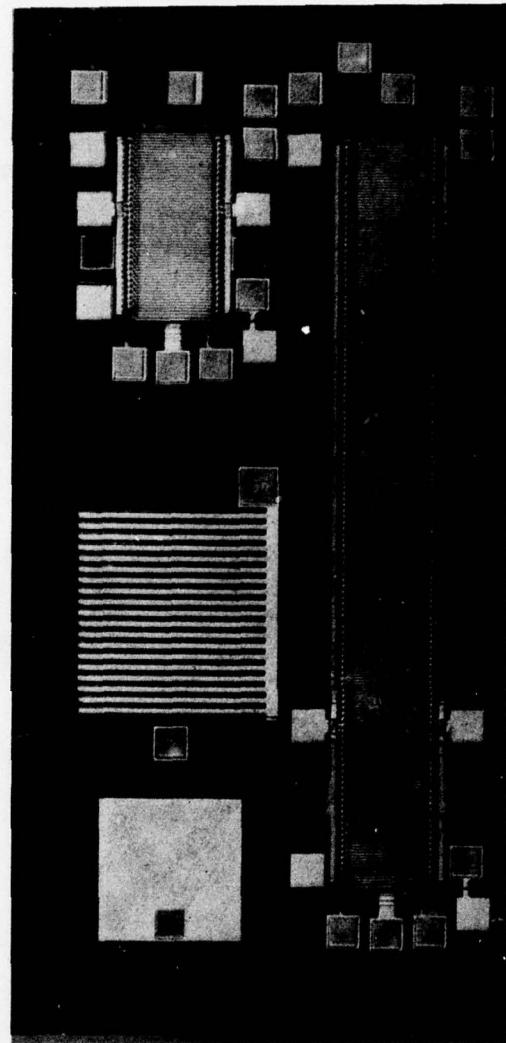


Fig. 1 Photograph of Peristaltic CCD's:
32 cell and 130 cell shift
registers.

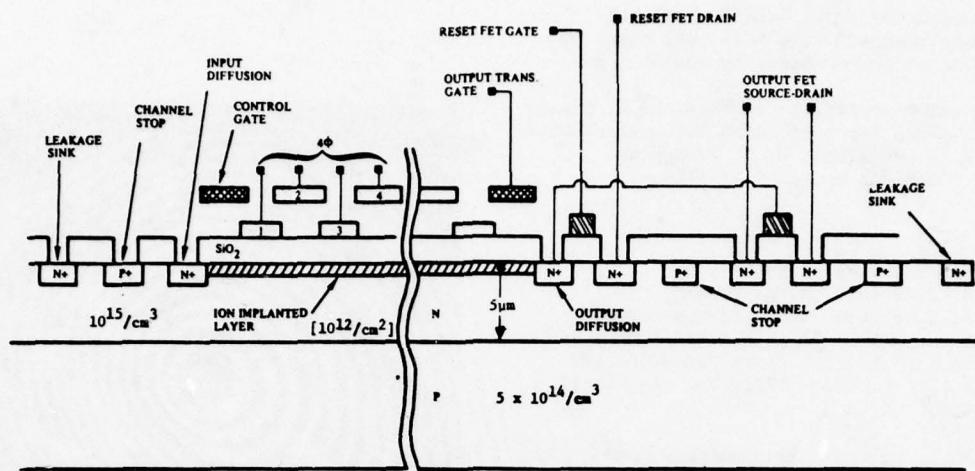


Fig. 2 Cross section of PCCD in direction of charge propagation [4].

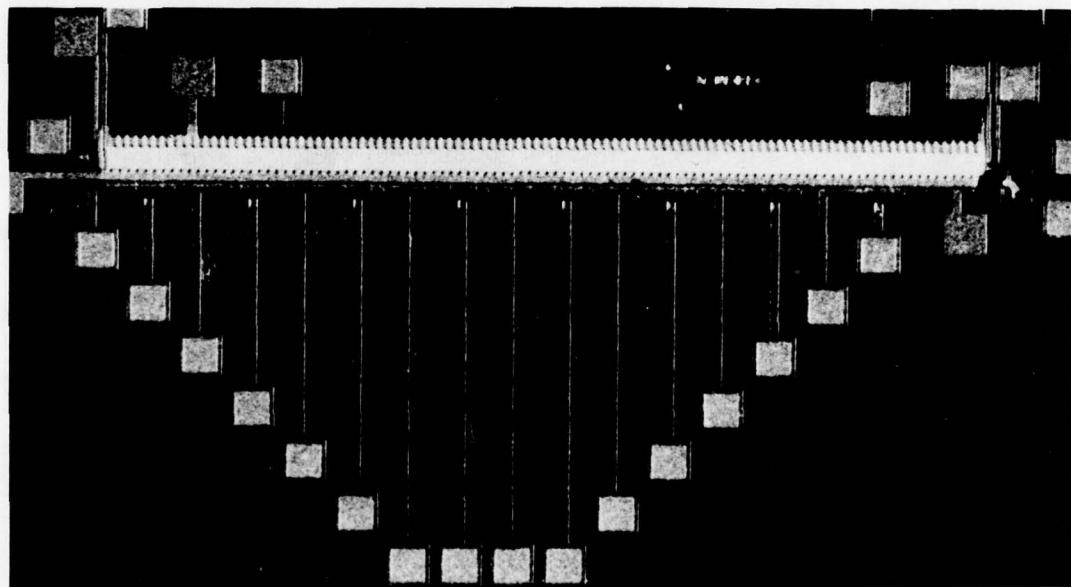


Fig. 3 Surface Channel CCD: 100 cell input-tapped shift register [5].

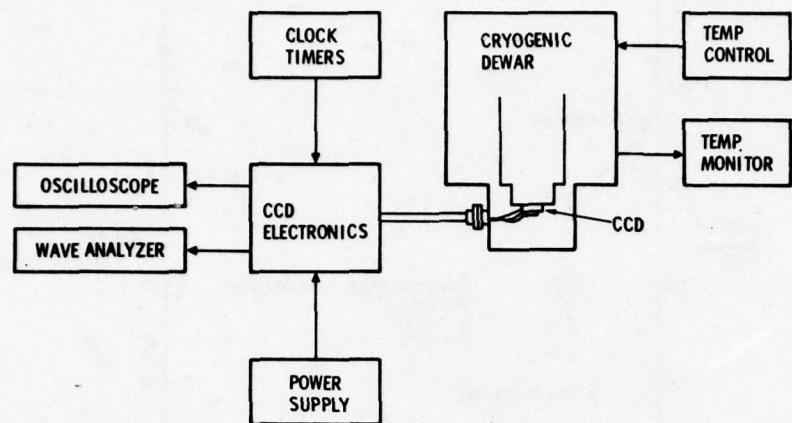


Fig. 4 Low Temperature Experimental Set-up: Block Diagram

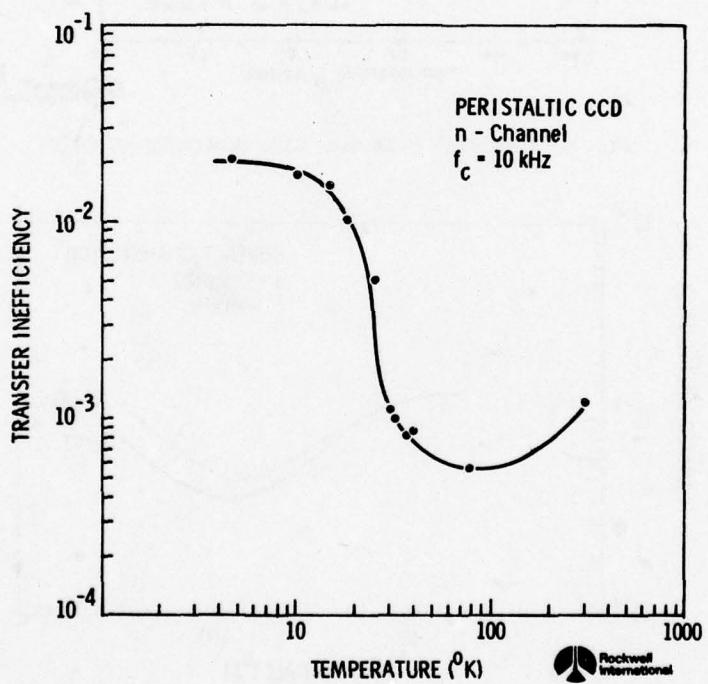


Fig. 5 PCCD transfer inefficiency vs. temperature

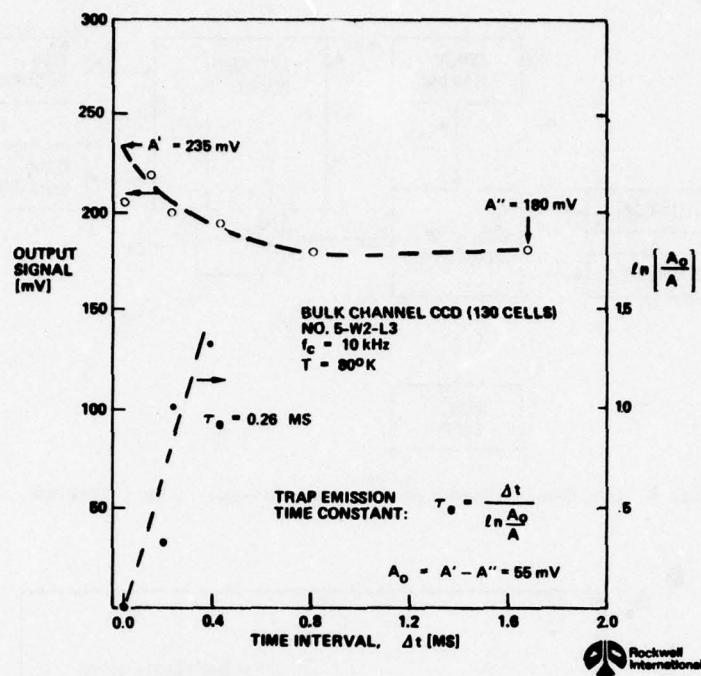


Fig. 6 PCCD trap emission time constants at 80°K

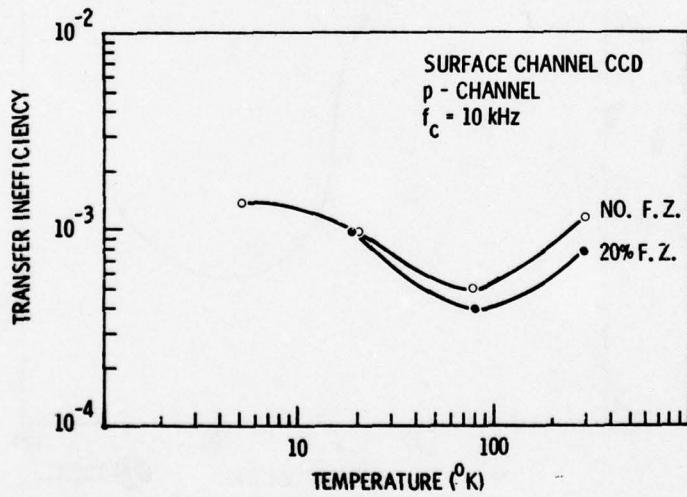


Fig. 7 SCCD transfer inefficiency vs. temperature

EXTREMELY HIGH SPEED CCD ANALOG DELAY LINE*

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B. T. French

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ABSTRACT. An N-channel epitaxial ion beam doped buried channel CCD has been fabricated and used to obtain time expansion of sampled analog data. Pulse trains containing up to 130 pulses of analog data were loaded into the device at 105 Mpps. The signal was then transferred out of the CCD for display and examination at 100 kpps. The fast-input/slow-output mode of operation circumvented on-chip high frequency difficulties, reduced the average power requirement of the driving circuitry, and provided a method of observing the effect of high transfer rates on charge transfer efficiency.

The device is a four phase double-overlapping gate structure with an ion implanted/epitaxial deeply buried N-channel. Gate length for this device, in the direction of charge propagation is 0.2 mils (5 μm). Each cell has a 10 mil wide channel which allows a full cell to contain about 0.76 pico coulombs of charge and permits operation over a wide dynamic range. Using push-clock waveforms with voltages switched between +3 to +13 volts, the device exhibited transfer efficiencies in excess of 0.999 per cell. This charge transfer efficiency was observed to be independent of the operating rate. The transfer inefficiency has been attributed to bulk traps with a time constant of 550 μsecs . Output voltages as high as 1.2 volts were observed on the output FET. Trap noise for a full well is characterizable by a sigma of 0.6 mV. No additional noise was observed in the fast/slow mode operation when compared with 500 KHz operation. Linearity of the device and background leakage charge have also been characterized and data is presented herein.

INTRODUCTION

An N-channel epitaxial ion implanted buried channel (peristaltic) CCD has been used to obtain time expansion of data. Input pulses of analog data have been inserted at a rate up to 105 Mpps, up to a maximum of 130 pulses. After acquiring the signal the operating rate of the device was reduced to 10^5 pps and the acquired signal was displayed and examined.

Normally CCD devices transfer the final portion of charge under a given gate from a location which is so near to the transfer gate surface that the effect of the transverse field is negligibly small. This effect limits the operating speed with which good transfer efficiency can be obtained to around 20 MHz. In order

to operate at higher frequencies, Esser introduced the peristaltic CCD which transfers charge in a channel several microns below the surface.¹ This configuration was obtained by using epitaxial layers grown on silicon substrates. Because the transverse electric field is very strong at the charge transfer area, the charge can be moved very rapidly out of each cell and, therefore, this type of CCD has been operated at very high frequencies.

DEVICE STRUCTURE

The device discussed here is a 130 cell, four phase CCD. It was fabricated using an N-type epitaxial layer grown on P-type silicon. The dopings of these layers were 1×10^{15} and $5 \times 10^{14} \text{ cm}^{-3}$, respectively. A cross sectional view of the

design is shown in Figure 1. A four phase overlapped Al propagation gate structure was employed as the driving structure. Silox was used as insulation between the two gate layers. The entire gate structure was formed on a layer of SiO_2 under which was the ion implanted layer. The ion implantation was followed by annealing for 1 hour at 1000°C . This process made the final SiO_2 layer 1500 Å thick. Because the device was intended for high speed operation, gate length (in the direction of propagation) was made as small as practicable, i.e., 0.2 mils. This was the spacing for the lower gate electrodes. A 0.225 mil line width for upper gate electrodes was used in order to provide adequate overlap over the lower gates. The total cell length consisting of 4 gates was 0.8 mils. The channel width was 10 mils in order to provide sufficient charge per cell. Referring to the figure, the first gate on the left was used as an input control electrode. A built-in FET amplifier as well as a diode were designed into the structure as outputs. Figure 2 and Figure 3 show photographs of the input and output regions of a finished device. The complete chip consisting of 2 PCCDs, a smaller test CCD and auxiliary test circuitry is shown in the photo of Figure 4. The N+ input and output diffusions shown in Figure 1 and discernible in photos provide good ohmic contact. The P+ diffusion around the CCD channel, also observable in the photos and illustrated in the drawing, acts as a channel stop in order to contain the active charges. Outside the P+ channel stop is an N+ diffusion which functions as a leakage sink. This feature is added in order to remove all leakage currents generated outside the P+ channel stop, a feature which is very important if these devices are to be used on substrates containing other active electronic devices.

HIGH FREQUENCY CCD DRIVER

The drive circuit supplies all gate voltage to operate a CCD with 4 phase drives. The phases are designed to be individually adjustable, although this has not been critical. The charge input was supplied from an external pulse generator which was synchronized with the counter in the driver circuit. For maximum speed, the device operates with 128 fast cell transfers, then 128 slow cell transfers.

The control logic for switching between fast and slow is done by MECL III and MECL 10000 series IC's. The block diagram is shown in Figure 5. Basically, the tester consists of three parts:

1. The logic circuit which controls the start/stop function and the changing of the clock rates;
2. The driving amplifiers which provide the gate voltages required to operate the CCD;
3. The external pulse generator which provides CCD input charge.

The logic circuit in Figure 5 has two clock frequency inputs; one for high and one for low speed operation. Each of the inputs goes through a synchronized switching circuit. When the high rate counter is activated, the high frequency clock is gated on at the beginning of a cycle. When counter sets to the low state, the low frequencies are passed through in the same way. Then the clock frequency is divided by two to obtain 4-phase voltages. Then this 4-phase square wave is amplified to more than 10 volts peak-to-peak and A.C. coupled to the CCD propagating gates. Each gate has its own D.C. bias adjustment.

The amplifier is a differential amplifier using two 2N5583's, followed by an emitter follower to lower the output impedance. The rise and fall time is around 5ns.

FAST/SLOW DEVICE OPERATION

To perform the required task of time expansion, the device was operated in fast/slow mode. First, the circuitry described above was used to operate the CCD in the fast mode. Signal data to be expanded were applied to the inputs and the entire device was filled with packets of analog signal charge. Next, the logic was switched to the slow mode, the input was gated off, and the signal charge packets were propagated to the output transistor for further processing or display. Several devices have been tested under fast input/slow output operation. The devices were operated through 130 cycles of high speed charge transfer followed by 130 cycles of low speed transfer. The timing diagram is shown in the drawing of Figure 7. As the input pulse is moved N cycles, the output is delayed the same number when it is run at low

frequency. Hence, the time expansion is proportional to the ratio of the high speed to low speed operation. The output and the input of the PCCD is shown in the oscilloscope photo of Figure 6. For this test the high speed input was at 62.5 Mpps and the slow speed output was at 100 Kpps.

Two signal pulses are visible both in the input and output traces of the CCD. The lefthand pulse, which emerges first in time, has been transferred through 110 cells at 62.5 MHz and 20 cells at 100 KHz. The right hand pulse has been transferred through 7 cells at 62.5 MHz and 123 cells at 100 KHz.

It was noted that transfer efficiency remains relatively constant over a wide range of operating frequencies. By varying the time of insertion of a single input pulse, the charge packet can be caused to traverse the CCD under any combination of fast/slow transfers totaling 130. In all cases, the transfer efficiency was found to be constant. The values were measured in excess of 0.999 per cell.

The low frequency limitation to slow playback is the thermal generation of carriers which fill the wells. The cumulative effect of thermal generation of charges becomes increasingly apparent at low frequencies and long device lengths. This effect is shown in the oscilloscope photo of Figure 8, as a continuous ramp buildup due to the thermally generated charges when the device is operated in the fast/slow mode.

INPUT LINEARITY

In order to achieve linearity and reduce the effects of input frequency variation upon quantity of input charge, our work utilized the input structure shown in the sketch, Figure 9a. The first gate (nearest the input diffusion) is the control gate G_1 . The other gates shown are transfer gates. As schematically shown in Figure 9b, the input N+ diffusion is pulsed more negative than gate G_1 so that electrons are injected through G_1 and ϕ_1 . Gate 2 is at a lower potential than the N+ region so that electrons are blocked by this barrier from continuing along the CCD channel. The next step labeled 9c shows the N+ region returned to a voltage higher than G_1 .

Some of the electrons under gate ϕ_1 now flow back. Hence, the surface potential under ϕ_1 will be level with G_1 . The next step, 9d, shows the transfer of this charge into the active CCD channel by increasing the voltage of gate ϕ_2 . Figure 9e shows the charge completely transferred to the CCD channel and the ϕ_1 and ϕ_2 gate voltages are returned to their previous values, thus starting the next cycle. The input/output transfer characteristics at 62.5 Mpps were measured and plotted. The results of this are shown in Figure 10. Additional information about the linearity of the device was derived from spectrum analysis of the output when driven with a low harmonic content sine wave input. Photographs of these experimental data are shown in Figures 10a and 10b.

Additional tests using 2-phase instead of 4-phase propagating drives indicate a reduction to 70% of previous output level with a slight degradation in linearity.

TRAPS

The time constant of the bulk traps of this device was measured. Our method of measurement consisted of running the CCD until all cells are empty; then transferring a few full packets of charge into the device so that the traps are filled. The inputting of charge is then stopped. When the input charge has stopped, the traps start to relax and release some of their charges. In order to measure the charge released at a particular time, a nearly full packet of charge is transferred to the CCD. Since part of this charge will now fill the empty traps sequentially, the traps will now take up the amount of charge which they have released during the decay time. Because the test charge will fill the vacated traps, the output level of this test charge will be less than the output if no traps were present. The difference in charge corresponds to the number of traps empty at the time the test charge passes through the device. Figure 11 is the plot of the relative number of traps remaining filled vs. time for two different operating frequencies. The parallel curves show that the trap release time constant (550 μ sec) is independent of operating frequency.

Other charge trapping mechanisms have been looked for but not observed. Surface state traps should not be involved since the

active charge carrying area in this device is isolated from the surface by the ion implanted layer.

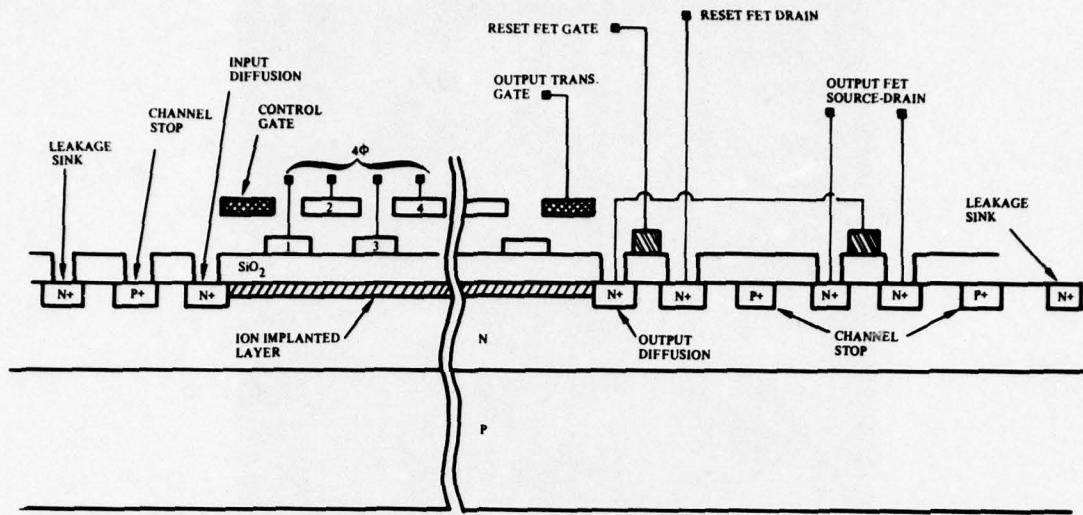
CONCLUSIONS

A CCD has been operated at rates up to 105 MHz. The present upper limit of operation is believed to be a function of the test circuitry and not of the CCD. It has been observed that charge transfer efficiency did not degrade with frequency of operation, and the results were only limited by our test equipment. From observations and experiments performed so far, it is believed the device will be able to be operated to at least 200 MHz. Bulk states which contribute to charge transfer inefficiency appear to be characterizable by a single trap level having a time constant of 550 usecs.

Noise and dynamic range of the device were found to be in close agreement with the values predicted theoretically for this design.

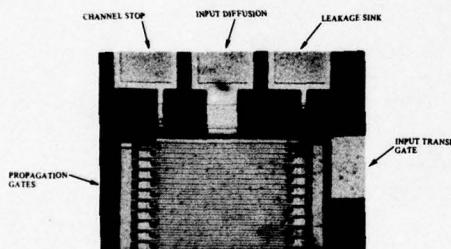
*This work was performed under subcontract by the Electronics Research Division of Rockwell International Corporation for GARD, Inc. performing under contract to Sandia Laboratories, a prime contractor of the U. S. Energy Research Development Administration.

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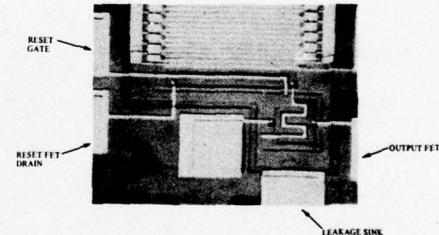
Peristaltic CCD - Cross Section (In Direction of Charge Propagation)

Figure 1.



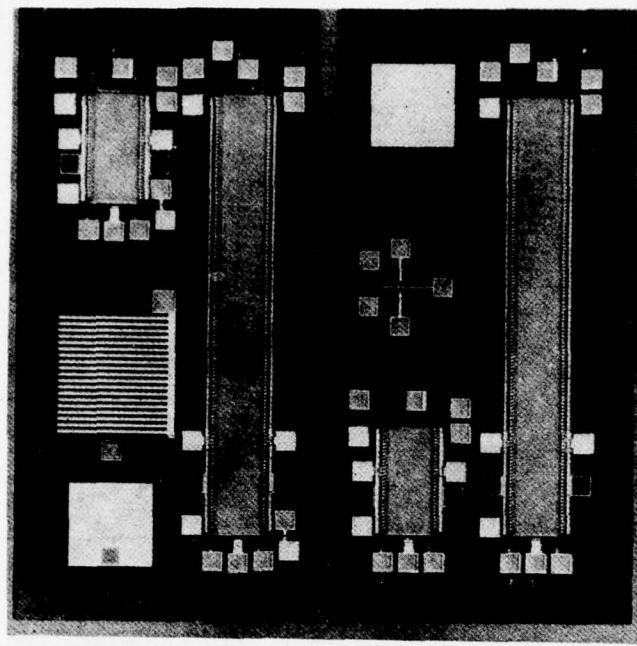
Photograph of Input of PCCD

Figure 2.



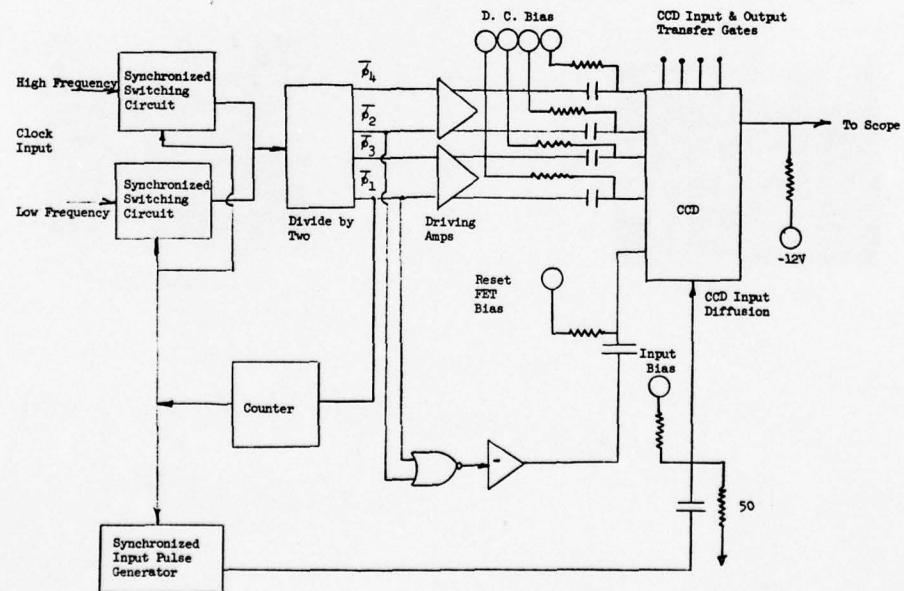
Photograph of Output of PCCD

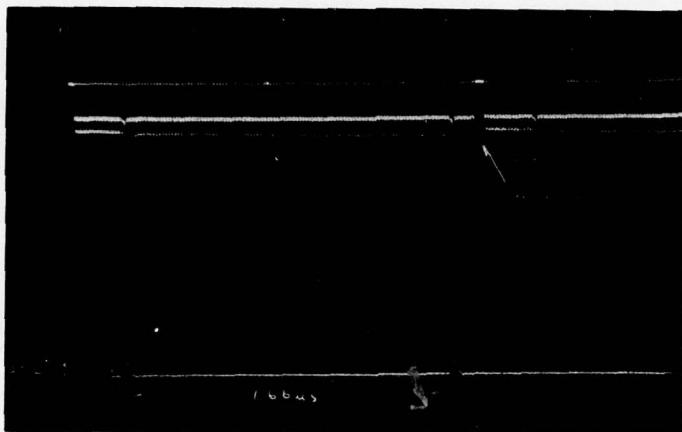
Figure 3.



PCCD Chip Design

Figure 4.

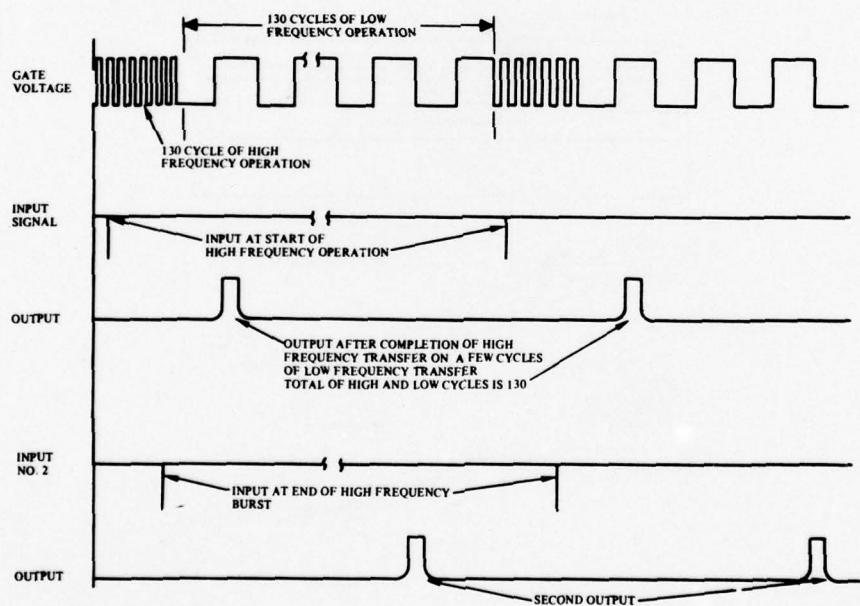




Comparison of Small and Large Number of High Speed Transfers in
CCD, Output Pulse of Small Number (7) is on Right,
Large Number (110) is on Left.

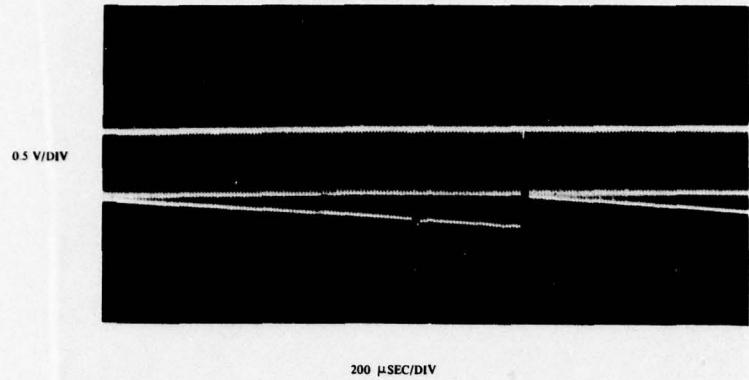
Output of Fast/Slow Operation

Figure 6.



Timing Diagram Fast/Slow Operation

Figure 7.



**Dark Current Output at 130° F in F/S Mode
(62.5 MHz/100 kHz)**

Figure 8.

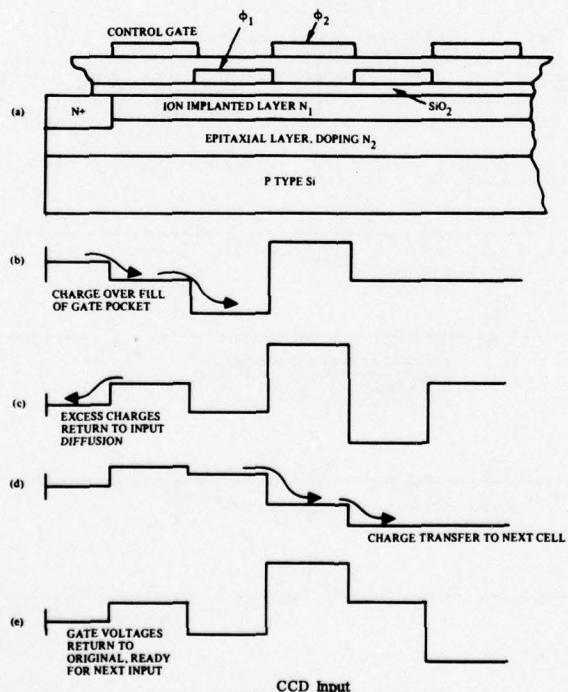
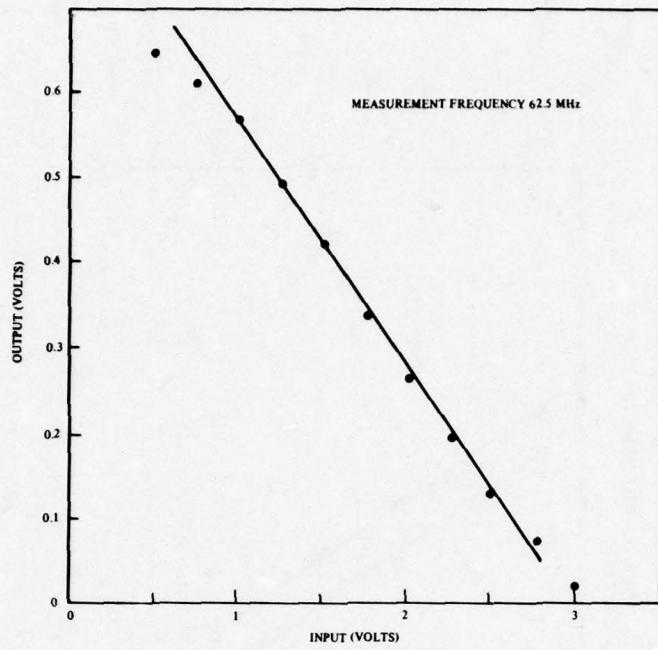
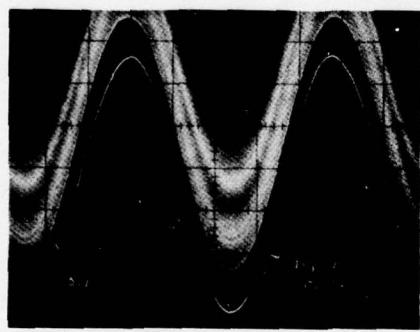


Figure 9.



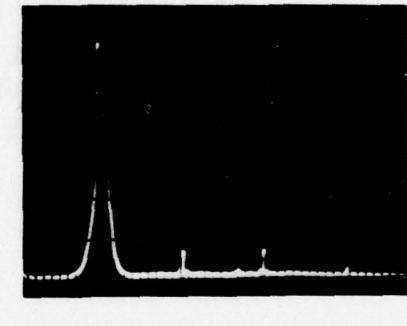
Peristaltic CCD Linearity

Figure 10.



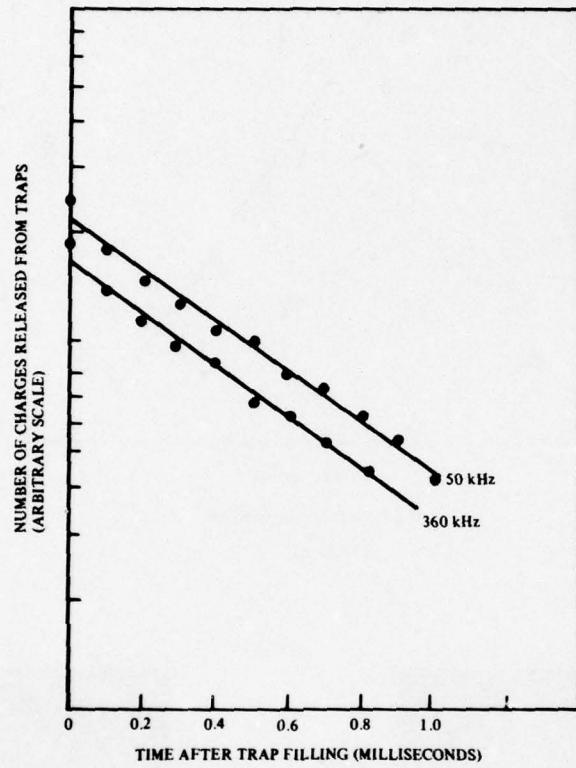
Sinewave Input to PCCD and its Output

Figure 10a.



Spectrum of CCD Output With 5 kHz Input Frequency

Figure 10b.



Bulk Trap Release Vs Time

Figure 11.

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HIGH SPEED OPERATION OF CCD's*

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ABSTRACT CCD's require a complex array of peripheral circuitry to support their operation in most applications. This includes input gating, multiple-phase clock signals and output gating, all synchronously functioning. Buried channel and peristaltic CCD's which can approach or attain VHF rates of operation require very sophisticated supporting circuits to fully realize their capabilities. Such circuits are in many cases not off-the-shelf items which can be independently selected. Good RF circuit techniques must be used in designing and combining circuits along with a thorough knowledge of CCD input and output parameters, to effectively develop a CCD analog system. This paper presents the development of peripheral circuitry for an analog CCD application at 62.5 Msamples/second. Unique aspects of input, output, and propagation gate drive circuits are considered both in terms of the CCD and its host system. The overall system application as a transient data recorder⁷ and the specific device development⁸, which was subcontracted to Rockwell International by GARD, are presented in separate papers at this conference.

INTRODUCTION

CCD analog shift registers are used for both delaying and expanding the time base of quantized analog data. The functional system required for either application is shown in Figure 1. A constant clocking rate provides a continuous quantizing of data with a constant delay. The time base of high speed data is expanded by reducing the clock rate after the data is loaded. The degree of expansion is proportional to the reduction in clock frequency. The operational requirements of the CCD peripheral elements in Figure 1 are the same with the possible exception of speed and bandwidth. The system described in this paper operates in the time base expansion mode with 62.5 Msample/second input rate and 100 Ksample/second output rate using a 128 cell peristaltic device. The discussion of the CCD supporting circuitry is divided into the three areas designated in Figure 1, namely, input, drive, and output sections.

INPUT

The high possible shifting rate and large dynamic ranges of various CCD's demands extremely high performance input techniques if the full capability of the devices are to be realized within a system. The state of the art in sampling techniques might well have to be advanced to meet these requirements. In a sampled data system, the aperture time requirement is a function of the maximum analog signal frequency and the resolution or accuracy desired. Sampling circuits with aperture times of well below one nanosecond and repetition rates approaching 100 MHz are needed. Several input approaches are discussed and compared below, followed by a description of a track and hold sampling circuit which has been developed and is compatible with the gate input methods.

INPUT TECHNIQUES

Potential Equilibrium Input

*This work was performed by GARD, INC., a Subsidiary of GATX Corporation, under Contract to Sandia Laboratories, a prime Contractor of the Energy Research and Development Agency (ERDA).

The potential equilibrium or fill and spill input technique has been shown to be a linear and low-noise method of applying input data to a CCD^{1,2}. It involves generating a potential well under an input gate, flooding it with charge and allowing the excess charge to spill back over the potential barrier of the adjacent gate. After the charge spilling process is completed, the measured charge packet is ready for transfer down the channel. The charge flooding can be achieved by a current pulse applied to the input diffusion. A major advantage of this method is that the measured charge quantity is independent of the exact nature of this diffusion pulse and is determined solely by the two input gate voltages. A disadvantage is that the charge spilling process requires a finite amount of time which increases with high accuracy requirements and thus places a frequency limitation and/or stringent timing requirement on the device clocking. This method is also susceptible to noise and interference components coupled to the input gates during the charge spilling period. These effects may be reduced, however, if the common mode rejection of the two input gates is significant and properly utilized in the input circuit design.

For high-speed high-resolution applications, a sample and hold circuit is required to reduce the aperture error to an acceptable level. The generation of the input diffusion current pulse must be sufficiently controlled within limits to insure adequate forward charge flow. Using standard fast ECL logic elements and high speed switching transistors, pulses with rise times and timing accuracies approaching one nanosecond have been constructed and proved adequate for generating input diffusion waveforms.

Gated Charge Input

A second input technique is the gated charge method, where the channel conductance below the input gate is simply varied to regulate charge flow, which accumulates for each charge packet. This method is much simpler and faster, but it has been shown to be less linear than the first method. Unlike the first method, the input charge packets are a function of the input diffusion current amplitude and duration.

This puts a much tighter control requirement on the input diffusion pulse waveform. In fact, the precision of the diffusion pulse generation must exceed the overall system accuracy requirement.

If the input current pulse width used is greater than the desired aperture time of the system, then a sample and hold circuit must be used. This method should be less susceptible to higher frequency noise and interference coupled to the input gate, since the input signal is effectively integrated over the input current pulse period. However, no common mode rejection is available with the single gate structure.

Direct Sampling Input

A third input approach is direct sampling of the analog signal on the CCD. To do this, the input structure must respond to pulse widths equal to or narrower than the desired aperture time. If this constraint is met, then in a manner similar to the second method, the analog signal can be applied to the input gate which controls the channel conductance during the diffusion pulse, which is now much shorter. Another version of this technique is to generate the narrow sampling pulse by gating the input current with a second input gate preceding the input signal gate.

This method is susceptible to coupled interference and noise on the signal gate for a much shorter period than the first two methods. In addition, since it requires no sample and hold circuit ahead of it, a lower impedance is more easily presented to the gate. This reduces the effects of stray capacitive coupling which can introduce interference and noise to the signal path. The narrower input pulse required with this method is more difficult to generate and may require different circuit devices and design techniques, such as step recovery diodes and use of transmission line techniques.

TRACK AND HOLD

A track and hold circuit has been developed which provides voltage sampling of an analog signal with an aperture error on the order of 100 picoseconds, and thus holding quantization error to 2^{-6} at 100 MHz. This circuit provides a constant voltage

level to the CCD for a large portion of its sampling period. Thus the CCD can be accurately loaded with the correct input sample as long as the appropriate CCD clocking occurs sometime during the "hold period" of the track and hold circuit. This increased CCD clock timing margin is quite significant in view of the very high current propagation gate signals which must be generated. This circuit also provides some degree of buffering between the analog signal path and the CCD.

Description

Figure 2 shows the basic sections of the circuit. The sampling gate consists of four matched Schottky diodes as shown in Figure 3. A balanced drive is provided to switch the bridge on and off, thereby allowing the hold capacitance voltage to track the input signal or hold the signal voltage level existing at the instant of turn-off. This arrangement provides the very small aperture time desired (less than 100 picoseconds). The clock balun section presents a balanced drive waveform to the diode bridge and performs an impedance transformation to provide proper voltage and current levels to the bridge. The degree of waveform balance achieved is very critical to the accuracy of the circuit. Two toroidal wound transmission line transformers are connected in tandem to maximize drive waveform symmetry. The low impedance signal source consists of a precision wideband attenuator which provides the following three functions: 1) reduces signal levels down to those compatible with track and hold CCD requirements, 2) isolates the signal source and signal line from the transients which the diode switching generates, and 3) provides a reduced driving impedance to the hold capacitance which enables faster charging. The input impedance of the attenuator can be adjusted to a nominal level such as 50 ohms which can then easily be connected to the signal source with 50 ohm transmission line. The output load impedance is limited to some value of capacitance which is chosen on the basis of slew rate, tracking, and hold voltage droop requirements of the circuit. This constraint makes the connection to the track and hold circuit to the CCD rather inflexible if the desired hold capacitance is low. A physically short connection minimizes stray shunt

capacitance and decreases noise and interference pickup.

Design Considerations

The wideband response and common mode rejection of toroidal wound transmission line transformers make them excellent devices for generating the balanced bridge drive³. Good squarewave response with rise times well below 1 nanosecond are possible if proper resistive loading is provided. Any degree of unbalance in the drive to the bridge results in an output error as the bridge is turned off. Minimum common mode output from the transformer is desired for all frequency components contained in the clocking waveform. Two transformers are used in tandem to further increase the degree of output balance. The degraded common mode rejection of these transformers at higher frequencies due to winding dissymmetries may be improved somewhat by adding a small trimming capacitance to one side of the transformer output. Care must be taken to avoid presenting excessive reactive loads to the transformers, since this causes output ringing which adds to output error or increases settling time.

A first order analysis of the hold capacitance charging phenomenon has been performed for the model in Figure 3. Assume that the balanced bridge drive is a gated constant current, the input signal is a constant voltage, and the four diodes are perfectly matched and conform to the standard diode V-I relation⁴. If the output voltage is initially zero, it is then constrained by the following equation after the drive current is applied.

$$(1) \quad V_o + R_g C_h \frac{dV_o}{dt} = V_g - .026 \frac{I + C_h \frac{dV_o}{dt}}{I - C_h \frac{dV_o}{dt}}$$

where V_g = signal voltage

R_g = signal source resistance

C_h = hold capacitance

I = bridge driving current

V_o = output voltage

The exact solution to this equation is difficult; however, it can be solved approximately

in three segments as shown in Figure 4. Equation (1) can be linearized and then solved yielding the following expression.

$$(2) \quad V_o = (V_g - V_B) \exp \left[\frac{-(t - t_B)}{(R_g + .052/I)C_h} \right]$$

This solution is increasingly accurate as the charging current, i_0 , decreases. It is, therefore, used to describe the final portion of the charging curve, segment BF in Figure 4. Point B is defined as the time when the solution reaches an accuracy of 95%. This can be shown to be when i_0 decreases to 0.39 I.

During the initial charging process, only two of the bridge diodes are conducting and essentially all of the drive current is flowing into the capacitor. The voltage is, therefore, described by equation (3).

$$(3) \quad V_o = \frac{I}{C_h} t$$

This expression defines segment OA of Figure 4. Point A is defined as the instant where i_0 decreases to 0.95 I. Segment AB is linear connection of the two points where its slope is taken to be the arithmetic means of the adjoining segment slopes. Equation (4) describes segment AB.

$$(4) \quad V_o = V_A + \frac{V_g - V_B}{2(R_g + .052/I) C_h} (t - t_A)$$

This approximation is justified by verifying that $V_B - V_A$ is a very small fraction of V_g for typical parameter values. Using equations (2), (3), and (4), it is possible to determine the final output voltage V_f and hence the charging error for a given set of operating parameters.

Matching of the four Schottky diodes is critical to the accuracy of circuit. DC matching provides minimum offset error and best temperature tracking of the diodes. AC matching is required to maintain good common mode rejection of the clocking signal as the bridge is turning off. Diode leakage is critical in determining the droop characteristics of the circuit. Fast slewing and charging rates require a very small hold capacitance which in turn is susceptible

to voltage droop. Since balanced leakage currents cannot be maintained under all operating conditions, worst case leakage at the maximum operating temperature should be considered.

The small value of the hold capacitance can lead to another problem. When the bridge is reverse biased, the signal source is still coupled to the output through the capacitance of the diodes. This results in a slight variation of the hold voltage as the input signal continues to change. This problem is reduced by increasing the hold capacitance and minimizing the diode capacitance. A neutralizing technique can also be employed which involves coupling a small controlled amount of inverted signal to the output to cancel the inherently fed through signal.

The signal attenuator can provide the lowest output impedance when a simple "L" section configuration is used. In general, increasing the amount of attenuation will decrease the output impedance which provides faster slewing, reduced charging error and faster transient recovery. It will also reduce the input VSWR and the switching transient levels resulting at the input. The input attenuator should be constructed with resistors which have good high frequency characteristics. Metal film resistors with minimum lead length or chip resistors are desirable.

Circuit layout techniques including component placement and connection methods greatly affect the operation of the entire circuit. Maintaining a symmetric configuration wherever possible helps maintain clocking balance and minimize common mode error. Stray capacitances, such as signal feed-through coupling, should be minimized. Minimum lead length and microstrip connections tend to reduce transformer ringing. High quality printed circuit board material with low dielectric loss characteristics up through microwave frequencies is desirable. Shielding techniques can be used to reduce stray coupling and susceptibility to interference. Track and hold circuits have been constructed which sample signal bandwidths up to 100 MHz at repetition rates in excess of 60 MHz. Thus far accuracies of 3% have been achieved.

Interface

The track and hold circuit developed is intended to drive only a small capacitive load, specifically an input gate shunted with a small capacitance of several pico-farads. The bulk of the input gate capacitance for the devices used is due to the bonding pad and package lead capacitance and totals about three picofarads. The stray capacitance of the diode leads and the PC board plating to ground is significant when working at these levels and must be considered in determining the effective value of hold capacitance.

If the signal source impedance is equal to the attenuator input impedance, for example 50 ohms, then a transmission line connection between the two of any length can be made with no effects other than signal delay. If the signal source has an output impedance other than 50 ohms, care should be taken to avoid transient reflections. This can be done by choosing the transmission line length such that the total round trip propagation time from the attenuator to the signal source and back does not equal an integral multiple of the sampling rate period. This will insure that a sampling transient does not reflect back into the attenuator as a succeeding sample is being taken. The source impedance at frequencies well above the signal bandwidth must be considered since the sampling transients contain very high frequency components. If a low-pass filter exists between the signal source and the attenuator, its output impedance must be considered. Most filters have a high VSWR above the cut-off frequencies which means transient reflection errors may be introduced.

DRIVE

The Peristaltic CCD's (PCCD) developed for this application employ a four phase propagation gate structure. A four phase ($4-\theta$) clock is required to transport charge in the device. Each forward transition is accomplished by dropping the barrier in front of the charge packet and raising the well behind it. The following discussion covers the requirements and considerations regarding the development of the $4-\theta$ clock/driver system.

4- θ CLOCK GENERATION

The $4-\theta$ clock signals required for the CCD's are generated using a pair of D-type Flip Flops connected as shown in Figure 5. When a clock frequency of 4 times the shift rate is applied to this clock generator, the four outputs will produce the waveforms shown in Figure 6. Each θ_n is 1/4 of the incoming clock frequency, and is delayed 1/4 period with respect to θ_{n-1} . The logic family used must be consistent with the frequency of operation. To operate at a shift rate of 62.5 MHz, an input clock frequency of 250 MHz is required. The only logic family capable of handling these frequencies is Emitter Coupled Logic (ECL). New entries in the ECL family include D-Flip-Flops capable of toggling at frequencies up to 700 MHz. With this method of four phase generation, the clock frequency can be changed and still retain the quadrature relationship of the four θ_n 's. This is important when considering time-expansion operation where two or more frequencies of operation are necessary. Also to be noted here is the fact that θ_1 and θ_3 are complementary as are θ_2 and θ_4 .

GATE DRIVER CHARACTERISTICS

Gate Driver

Once the gate driver timing signals are generated as above, a driver must be used to provide CCD gate drive of the required amplitude. The load on the driver is primarily capacitive in nature. In order to specify the driver characteristics, it must first be determined what the drive requirements of the CCD are.

Driver Speed

When operating at 62.5 MHz shift rate, the period of the driver waveform is 16 nsec. The optimum waveform is shown in Figure 7. In the figure, $T_0 = 16$ nsec. The transition times, t_r and t_f , must be $T_0/2$, or 8 nsec, maximum. It has been recommended by the device manufacturer that a minimum transition time be 5 nanoseconds. This is to insure that a well collapse (or barrier rise) does not occur so quickly as to spill charge over the channel stops or into adjacent charge packets. The end result of such operation would result in reduced dynamic range and charge transfer efficiency. This minimum

rise time puts an upper limit on the current drive necessary to drive the capacitive gate load.

Current and Voltage Requirements

Considering the waveform of Figure 7, the recommended peak-to-peak swing ($V_H - V_L$) is in the range of 12 to 15 volts for the devices used. With the high density gate structures, it is necessary to put every other gate on a different level, physically further away from the substrate. In order to compensate for that portion of the field lost in the additional insulating layer, upper gates must have a 15 to 25% greater voltage swing than that for lower gates. The driver design will be based on the larger voltage swing of 15 volts.

The current drive required of the driver is a function of voltage swing, rise/fall time, and the capacitive loading of the drive gates. The gate loading of the devices used at GARD was about 25 pf. The current required for the slewing of the gate voltage is given by:

$$I = C \frac{\Delta V}{\Delta t}$$

where C is the gate capacitance = 25 pf

ΔV = the peak-to-peak swing = 15 volts

Δt = transition time = 6 nsec

The required current is, therefore,:

$$I = 25 \times 10^{-12} \times \frac{15}{6 \times 10^{-9}} = 62.5 \text{ ma.}$$

The additional loading of the transmission path (cable or printed circuit) and stray capacitance could add as much as 10 to 15 pf to the driver load. This will increase the driver current requirement to 100 ma per CCD gate. The driver must be able to source as well as sink this current to provide both rise and fall times in the 6 nsec range.

Delay Stability

The driver must provide an output waveform with a constant delay with respect to the input waveform. This insures that the

4-Ø drive signals at the CCQ remain in quadrature over the entire frequency range of interest. For a set of four drivers, the delays should not differ by more than ± 1 nsec. If the stability of each driver is within ± 0.5 nsec over the entire frequency range, any mismatch in the driver delays can be compensated for by using delay lines at the inputs of the drivers.

Transient Response

The transient response of the driver must be such that the clock can be halted, or a frequency change can be made, without having any output aberrations which may destroy the barriers separating individual charge packets. This is important in the time expansion application where the input mode is at 62.5 MHz shift rate and the output is at a much lower rate. When the last high frequency clock pulse is received, the drivers will respond by changing two of the phase drive lines. After this change, the outputs should remain in their respective output states until the next clock pulse is received. This requirement prevents the use of tuning out the capacitive CCD gate load to minimize gate drive requirements.

DRIVER DESIGN CONSIDERATIONS

Power and Thermal Calculations

As indicated in an earlier section, the current required to slew the gate is 100 mA. Assume that this current is drawn from a 17 volt power supply and that the rise time takes up 6 out of each 16 nanoseconds. During the fall time, the driver current is sunk to ground, hence only a small amount of power is required. The average power at 62.5 MHz, not considering driver inefficiency, is:

$$\begin{aligned} P_{avg} &= V_{PS} \times I_{peak} \times \text{duty cycle} \\ &= 17 \times 0.1 \times \frac{6}{16} \\ &= .637 \text{ watts} \end{aligned}$$

The driver, however, will not be 100% efficient. Therefore, driver power of .7 to .8 watts will be required. For four drivers to support a single CCD, the power required will be 3.2 watts at 62.5 MHz. Because the driver is driving a reactive load, very little power is dissipated by the CCD gate;

virtually all of the 3.2 watts is dissipated in the 4-Ø driver circuit. Fortunately, the time expansion mode requires that the drivers be operating at the 62.5 MHz rate less than 10% of the time. The overall average power is, therefore, greatly reduced. The drivers must be designed, however, to withstand peak power of 3.2 watts for periods up to 10 milliseconds.

Physical Layout

The physical layout must take into consideration both the power requirements and the capacitive loading of the driver. The driver should be located as close as possible to the CCD so as to minimize the additional driver loading due to the transmission path. The CCD is sensitive to temperature; so it is important to isolate it from external heat sources.

An increase in chip temperature will increase the dark current (thermal well filling) of the CCD. This is not of great concern at high shift rates since a given charge packet will not be in residence in the chip for a sufficient length of time to be distorted by thermal filling, but a thermal filling at low shift rates can be significant. The driver circuitry, located close to the CCD, must be carefully laid out to avoid excess heat transfer to the CCD.

Circuit Techniques

Commercial MOS drivers with ECL-compatible inputs are available. Such a device is the Texas Instruments SN75366. This device is specified as having a typical transition time of 17 nanoseconds for a 15 volt swing when loaded with 390 pf. The current output to meet this transition time is:

$$I = C \frac{de}{dt} = 390 \times 10^{-12} \times \frac{15}{17 \times 10^{-9}} = 344 \text{ ma.}$$

This current is sufficient to slew a 40 pf load in 6 nsec indicating a more than adequate output stage, but an evaluation of sample devices indicates that the chip is not capable of high frequency operation due to limitations in the input or pre-driver stages.

DISCRET COMPONENT DRIVER IMPLEMENTATION

Since the single-chip CCD driver could not satisfy the stated requirements, a driver will have to be developed with discrete hardware. A block diagram of such a circuit is shown in Figure 8. In evaluation of circuit techniques for its design, the following factors must be considered:

- (1) Interfacing with ECL logic levels of the 4-phase generator.
- (2) Driver output configuration.
- (3) Speed-up techniques.

Each of these will be individually discussed.

ECL Interface

The interface with the ECL logic swing of -0.9 volts to -1.6 volts is not trivial. The logic swing of 0.9 volts is not great enough to reliably switch the base-emitter junction of a bipolar transistor whose emitter is tied to a firm reference voltage. Variance in both the ECL voltage swing as well as transistor forward junction voltage with temperature make this method unreliable.

Commercially available ECL to TTL translators can be used. Such a device as the MC10125 converts ECL levels to TTL levels using a Schottky output stage. Operation at 62.5 MHz, however, is at the maximum limit of this device resulting in a sine wave output which may not achieve the maximum TTL logic swing. Also, the variance in the delay of these devices is not consistent with the driver requirements.

The remaining technique is to use a differential amplifier as the input stage using the center swing voltage of the ECL family (V_{BB}) as the reference input. V_{BB} can be generated with an ECL chip which will track the ECL swing to compensate for temperature variances. The differential transistor input can be purchased in one package. Therefore, the variance in base-emitter junction drop of one will be offset by a similar variance in the other. The resultant input structure will be stable and ECL-compatible at all temperatures.

Driver Output Configuration

At low frequencies, the number of active components can be reduced by using

a single transistor and a passive pull-up resistor to drive the CCD gates. However, to obtain the necessary rise time, the pull-up resistor value (for a time constant of 2 nanoseconds) is:

$$R = \frac{\tau}{C} = \frac{2 \times 10^{-9}}{40 \times 10^{-12}} = 50 \text{ ohms}$$

As a result, the output transistor would not only have to pull down the capacitive load of the CCD, but also the resistive load of the pull-up resistor. This also adds a DC component to the power required by the drivers and contributes to the heat which will be generated in the vicinity of the CCD's.

The only available approach is a form of push-pull or totem-pole output structure, in which significant power is consumed only during output transitions. Medium-power RF transistors are used in the final stage driven by low-power high-speed switching transistors connected in a Darlington configuration. The pull up and pull down transistors must be driven in a complementary manner. The necessary complementary signals can be obtained using the two outputs of the differential amplifier or with the use of a single stage phase inverter.

Speed-up Techniques

The switching time of the driver can be greatly reduced by preventing all transistors from going into saturation. A saturated transistor can take up to 400 nsec to turn off due to junction storage time. An effective method of preventing transistor saturation is through the use of Schottky clamping. The negative feedback provided by the clamp will allow the transistor to approach saturation but never enter it. As a result, the turn-off time can be made comparable to turn-on time.

Secondly, the use of speed-up capacitors in parallel with the resistors in transistor base circuits can improve turn-off and turn on time as well. When the transistor is turned on, the base is initially driven harder; when turned off, the base is driven below the emitter voltage to aid in removing charge from the base-emitter junction area.

Using the techniques discussed above, a circuit can be developed to meet the requirements. The combined circuit is shown in block diagram form in Figure 8. Other considerations are to keep the geometry as small as possible, while also being cognizant of power dissipation requirements.

OUTPUT

In the time expansion application of the PCCD which has been discussed, the output is required to operate at a greatly reduced speed, namely 125 KHz. This feature greatly reduces the degree of design difficulty and opens the door to a variety of approaches. A discussion of the various output approaches is beyond the scope of this paper. However, the output structure and operation for the PCCD discussed above will be described. The general considerations mentioned will apply to most output approaches operating in the same speed range. In the particular application discussed, the output of the CCD is to be digitized by an A/D converter. Since a CCD present valid output data for only 25% of the output clock period, it is important that all output circuits respond quickly to allow sufficient time for the A/D to complete the conversion before the output data becomes invalid.

CCD OUTPUT

The output of the PCCD is buffered by an on-chip FET. A reset FET is employed to remove the charge from the previous sample prior to shifting the next sample for read out. An equivalent circuit of the output structure is shown in Figure 9. Both devices are N-channel depletion-mode types. The output FET operates in a source-follower configuration. Hence, the output FET drain will be connected to some positive DC bias voltage. The output FET source is connected to a negative supply voltage via a load resistor. In the source-follower mode, the output voltage will be approximately the same as the gate voltage, which is a function of the amount of charge on the gate. This gate acts as a capacitor. The charge being propagated in the devices used are electrons. Hence, a larger charge packet will result in more negative output voltage. The reset FET source is connected to the output FET gate. This FET also operates in a source-follower mode. When a positive pulse signal is applied to the reset FET gate, the output FET

gate is reset to about the same potential as that of the reset FET gate unless it is driven into saturation, in which case the reset level is dependent on the reset FET drain voltage. The reset FET drain is connected to some positive voltage, usually the same as the N⁺ diffusion ring on the CCD. A description of each of the supporting external circuits for the output circuit follow. It should be remembered that the CCD's discussed in this paper were used in a time expansion mode exclusively. Hence, the output circuitry need not be the type that can operate at the high input frequencies, but only at the read out frequency of 125 KHz.

RESET CIRCUITS

The reset FET gate pulse must be properly timed with the four CCD gate drives. A properly timed reset occurs when both θ_1 and θ_2 are in the high state or the gate potentials are as shown in Figure 10. It is also strongly recommended by the device manufacturer that, during the high speed input of the CCD, the output be in a state of constant, or DC, reset, so the reset FET will remove the charge which is now entering the output at a high rate. The reset pulse width, during read out, is not critical, but the falling edge of the reset pulse must occur before the rising edge of θ_3 . The last propagation gate of the CCD is θ_3 . When θ_3 gate voltage goes to the high state, the θ_3 barrier drops and charges from the next sample begin to flow to the output FET gate. A portion of this charge will be removed by the reset FET should the reset signal remain in the high state after the rise of θ_3 , thus distorting the charge packet.

The reset pulse amplitude is very critical if the reset FET is not driven into saturation. This is because the reset FET is then operating as a source follower and when turned on will have reset the output to a voltage determined by the reset pulse voltage itself. Following the reset, the output voltage will become more negative as the next charge packet is shifted in. Provided that the CCD is correctly biased, this voltage change will be proportional to the amount of charge shifted to the output FET gate. Hence, a change in the amplitude of the reset FET gate pulse will result in an offset of the entire output voltage levels including the portion of the output

waveform containing the usable output signal. Considering the fact that the output signal from full well to empty well is seen on the output FET source as a ΔV of less than 0.5V, it is imperative that the reset FET pulse amplitude be carefully regulated. This can be accomplished by clamping the reset FET gate to a precision reference or using a common emitter transistor as a reset driver. In the later case, the collector load can be a precision resistive divider on a well regulated voltage as shown in Figure 11. The precision resistors R₁ and R₂ can be selected in such a way as to result in the desired reset voltage when the driver transistor is turned off. The reset FET may be operated in saturation in which case the output reset level becomes relatively independent of the gate pulse voltage. The reset level in this case will be the bias voltage on the reset drain, which must then be well regulated to insure accurate reset. The "on" resistance of the saturated reset FET must be small enough to insure total dissipation of the signal charge within the duration of the reset pulse. An additional constraint on the reset FET is that it be capable of dissipating the residual charge which is dumped into the output diffusion during the input loading mode of the CCD. Failure to dissipate this charge will result in a back flooding of charge at the output which will completely destroy the initial signal charge packet.

SIGNAL OUTPUT

As mentioned above, the output of the CCD is a source-follower FET. The output waveform is shown in Figure 12. The useable signal output range of the CCD is about 0.2 to 0.4 volts. As shown in the figure, the output waveform has an overall voltage swing about an order of magnitude greater than the useable signal range. This must be contend with by the output interface circuitry and will be discussed later. Certain characteristics of the output FET must be considered here. The voltage gain of the output MOS-FET is constant over the operating temperature range, typically about 0.9. The output offset voltage is not as stable. As is typically the case with MOS-FET's, the output FET gate to source voltage has a temperature coefficient, TC, which is a function of drain current⁵. This TC can be as large as 1.5 mv/ $^{\circ}$ C. Considering an operating temperature range of 50 $^{\circ}$ C, this

results in an output offset shift of up to 75 mv as a function of temperature. This is about 25% of the dynamic range of the CCD output and, therefore, is a cause of concern. For a given FET, a particular drain current exists where the gate to source voltage has a zero temperature coefficient. At drain currents below this point, the V_{GS} has a positive TC, and higher drain currents yield a negative TC. It has been empirically determined that the drain current for zero TC of V_{GS} was about 0.1 ma for the devices used. The drain current is predominantly determined by the output voltage, the source resistance and the supply voltage V_{SS} . The supply voltage must be sufficiently negative to accommodate the negative signal voltage swing which in this case is about -8 to -10 volts. To operate at .1 ma, the source resistor R_s is:

$$R_s = \frac{V_s - V_{SS}}{I_{source}} = \frac{-5 - (-8)}{.1 \text{ ma}} = 30 \text{ k}\Omega$$

With this high impedance, the time constant of the output circuitry, assuming a 10 pf load resulting from stray capacitance, is:

$$\tau = R_s \cdot C_{out} = 3 \times 10^4 \times 10^{-11} = 0.3 \mu\text{sec}$$

This is compared with the time when data is valid on the CCD output, which is less than 1/4 of the output shift period (in this case, 2 μsec). Hence, the time constant of the output circuit is a significant portion of the time when CCD data is available. To remedy this situation, the value of R_s must be reduced to lower the time constant which raises the bias current of the FET, resulting in a negative temperature coefficient V_{GS} .

One of two approaches can be taken to remove this temperature dependency. The first would be to correct for the output offset with external circuitry, which is a difficult task at best. Another method is to design the output FET such that the operating drain current yields a V_{GS} temperature coefficient of zero. The latter approach, while not possible in all applications, is very desirable.

As indicated previously, the dynamic range of the output is only .2 to .4v p-p.

Since the ultimate goal in this application is to digitize this analog signal, amplification is required to produce a signal dynamic range of 10 volts p-p to be consistent with available analog to digital converters. To achieve this, an external amplifier gain of 20 to 50 is required. Also, the offset of 5 volts must be removed so the resultant amplifier output is +5 volts. It can be seen that with the high gain of the amplifier, the 5 volt swing on the input during reset will cause the amplifier to go into nonlinear operation. Care must be taken in the amplifier design to prevent device saturation when the reset pulse overdrives the input. If this saturation is not prevented, the amplifier will not settle to the desired output value within $T_0/8$ or 1 μsec . This latter requirement is necessary so the remaining 1 μsec , during which the CCD output presents valid data, may be allocated to the A/D for digitization time.

THERMAL FILLING AND RADIATION EFFECTS

The extent of filling of the CCD by thermal, or dark, current is a function of CCD chip temperature and shift rate. For a given chip temperature, the amount of charge in a given packet which is due to dark current is directly proportional to the time that the charge packet is in residence in the CCD channel. In this application of time expansion, the amount of time that a charge packet is in the CCD channel during the high-speed input mode is insignificant compared to the time required for the CCD read out. It will be assumed that the loading time is zero.

As the charge is shifted out at a relatively slow rate, the first charge packet will not be affected by thermal filling. As the read out progresses, subsequent charge packets will have been in residence in the channel for progressively longer periods of time. This can be seen by viewing the output of a CCD with zero input signal. The first sample is at cutoff, indicating an empty well, subsequent samples will become more negative, indicating increasing amount of charge, forming a negative sloping line. As the read out frequency is reduced, the slope of the line increases. Eventually, a frequency is reached where the last sample read is a full well. Ideally, it is desirable that the output shift rate be high enough that the slope of the output signal is essentially

zero. In all probability, such a frequency may not be consistent with moderate speed A/D converters, hence greatly increasing the cost of digitizing hardware. In addition, variance in dark current from one device to another makes compensation difficult.

The effects of gamma radiation are similar to those of thermal filling. When the CCD is exposed to such radiation, substrate atoms are ionized and the resultant electrons are able to enter the potential wells in the CCD channel. The extent of this well filling is not predictable, but it is reasonable to assume that all wells will experience the same amount of additional charge. If the gamma radiation pulse is incident on the CCD when half of the samples have been read, the remaining half of the samples will have a DC offset with respect to the first half.

A differential channel CCD can be used to remove the effects of thermal and radiation well filling. This is accomplished by using a two channel CCD on the same substrate, driven by the same clock signals. The input signal is applied to only one channel; the remaining channel will have only a DC level on its input. As a result, the only variation in the output of the second channel will be due to thermal and radiation effects. The two channel outputs are connected to a differential amplifier, possibly integrated with the output amplifier for signal gain. The radiation and thermal filling will be common to both channel outputs; consequently their effects will not be seen on the output of the amplifier.

CONCLUSION

The supporting peripheral circuitry required to operate a high speed CCD has been designed and implemented with discrete standardly available devices. The developed circuits enable the devices to approach their present full performance capability in a working system application. The cost-effective implementation of the major elements of the support system, such as propagation drivers and input circuits, suggest the CCD approach to many very high speed analog applications is a viable one. Standard high speed ECL logic families were found to be adequate for developing and timing the various clocking and control sig-

nals required. Because the time expansion application was of major concern, high-speed output circuitry was not considered extensively. The design and interface techniques required to develop such circuitry, however, are similar to those described.

Areas in which improvement could benefit overall system performance and ease of production are sample and hold amplitude accuracy and propagation gate driver delay consistency. Methods of increasing the isolation between sample and hold output and the high level CCD propagation gate signals are currently being investigated. More accurate control of propagation gate timing will improve accuracy of the potential equilibrium input method and insure maximum charge handling capability of the CCD (improved dynamic range). Differential channel CCD's have been successfully operated at lower speeds⁶. Significant advantages to a similar approach at high speed operation are anticipated. Greatly increased input common mode rejection should result if identical input structures are used. Thermal and radiation filling as well as EMI effects on the output signal will be greatly reduced if channel balance is maintained. Compensation of output device offsets and temperature drifts should be more easily achieved. GARD is currently developing a dual channel PCCD system operating at the speeds described.

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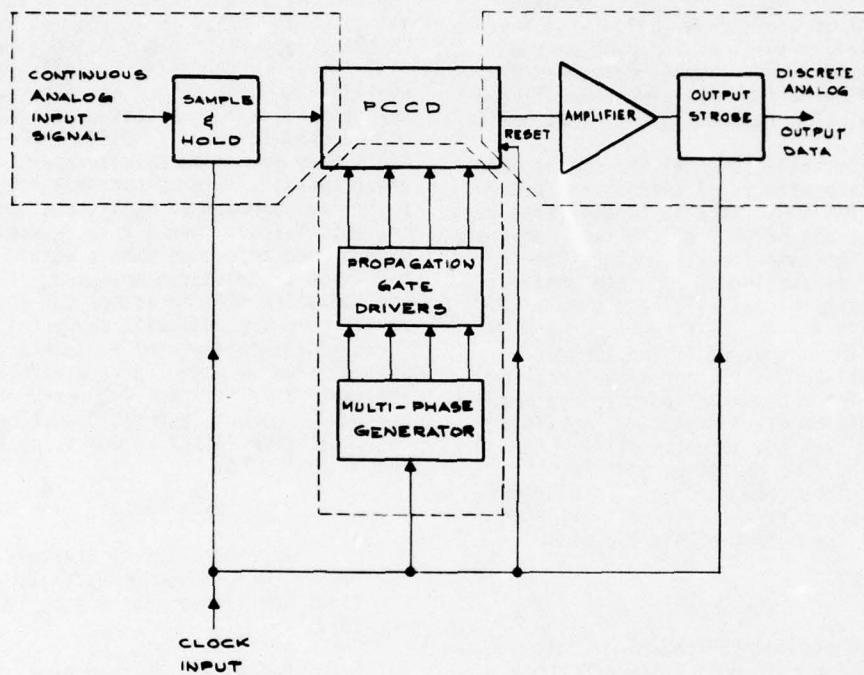


Figure 1. Functional CCD Analog System, Block Diagram

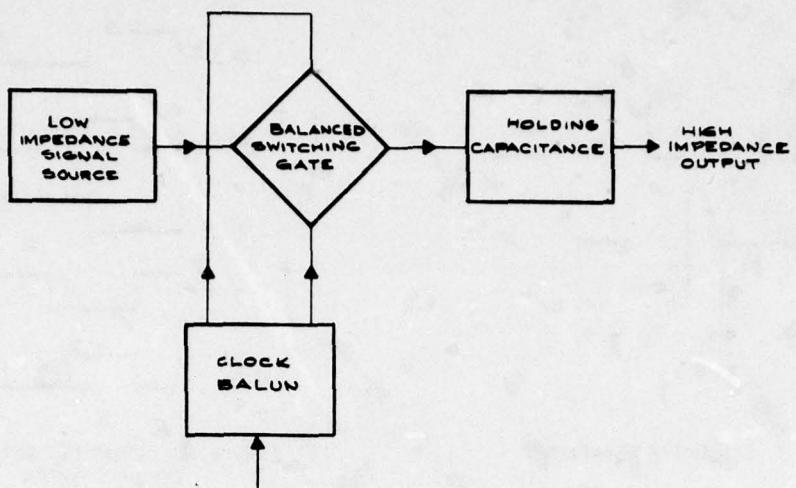


Figure 2. Track and Hold Circuit, Block Diagram

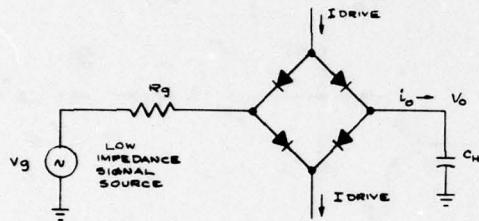


Figure 3. Track and Hold Circuit for Charging Analysis

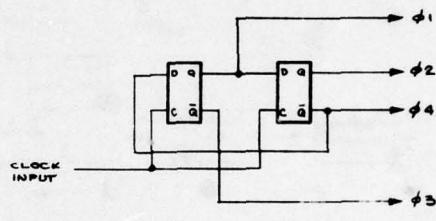


Figure 5. 4-Phase Generator, Logic Diagram

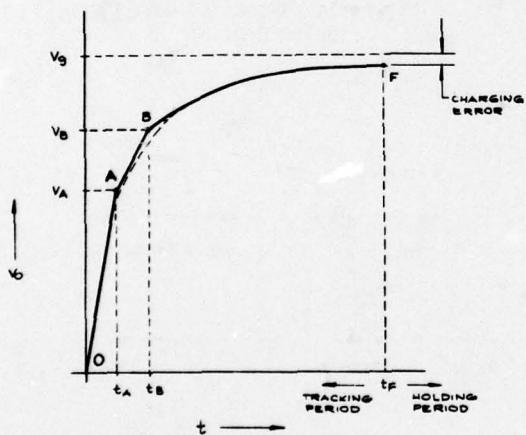


Figure 4. Track and Hold Charging Curve

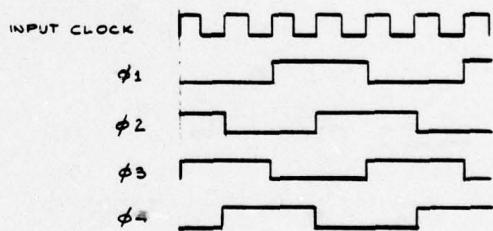


Figure 6. 4-Phase Generator Output, Timing Diagram

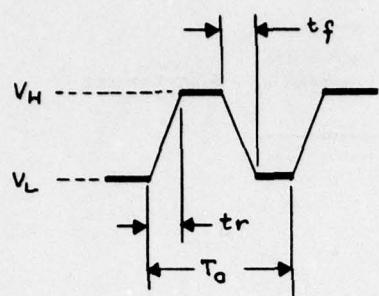


Figure 7. CCD Drive Waveform

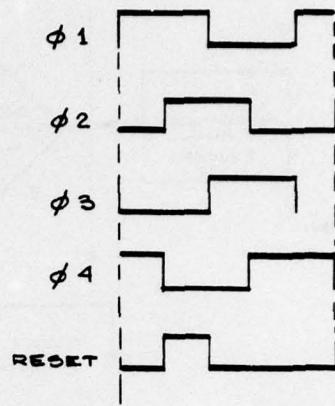


Figure 10. Reset FET Gate Driver,
Timing Diagram

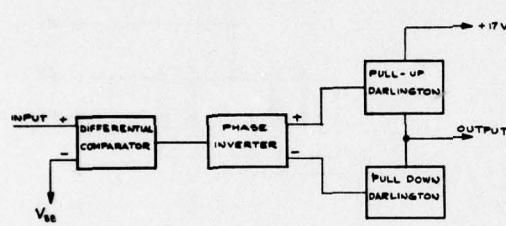


Figure 8. CCD Clock Driver,
Block Diagram

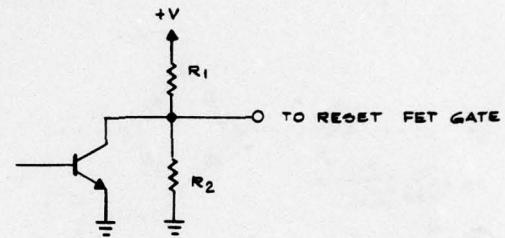


Figure 11. Reset FET Gate
Drive Circuit

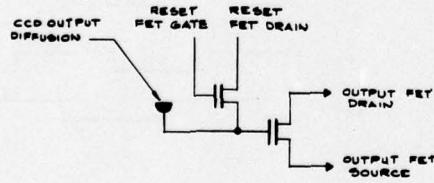


Figure 9. CCD Output Circuit

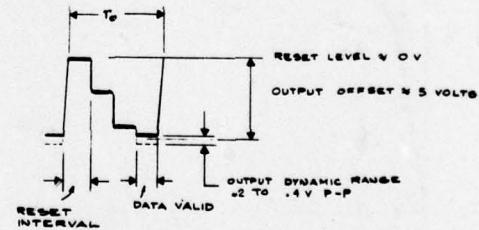


Figure 12. CCD Output Waveform

A CCD MEMORY FOR RADAR SIGNAL PROCESSING

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ABSTRACT

The results of an Air Force Avionics Laboratory program to develop a CCD digital memory device are discussed. Chip design and performance characteristics are given and compared with other known CCD devices. The use of the 16K bit CCD memory for radar signal processing is discussed and a specific system example is shown. CCD memory cost is projected and compared with other leading semiconductor memory approaches.

INTRODUCTION

The Air Force has a significant number of applications for 10^6 to 10^8 bit memories which do not require non-volatile operation. Among these are synthetic aperture radar processors, scan converters, radar change detectors, high speed swapping discs in communications systems, and buffer memories for video sensor bandwidth compression. In 1972 the Air Force Avionics Laboratory initiated a program with Fairchild Camera and Instrument Co. (Ref 1) to develop a low-cost general purpose digital CCD memory chip that would offer significant cost and performance advantages for such systems. That program has now concluded with the demonstration of a 16K bit device and the partial development of a 32K bit device, both of which have potential application in military and commercial systems.

DISCUSSION OF CHIP DESIGNS

The Fairchild devices employ a novel memory organization to achieve fast access time along with low power dissipation. This organization is known as the Line-Addressable Random Access Memory (LARAM) approach. (Fig. 1) As implemented with a 1-1/2 phase CCD structure, this organization achieves bit densities comparable to either the serpentine or SPS types while reducing chip access time and clock load capacitance by an order of magnitude. The principle of

operation involves clocking a string of bits into a selected register via a common input bus. The clocks are then halted and the information stored in a static fashion as in an MOS RAM type device. As long as the memory returns to this register before the leakage charge exceeds the unity threshold, any other register may be selected at random and undergo a READ, WRITE, or RESTORE operation. When the original register is again selected, the information is clocked out, sensed, and either recirculated or replaced with new data as appropriate. The key to obtaining a compact chip layout is the 1-1/2 phase CCD structure, which permits the single selectable clock line to run the entire length of each register.

16K BIT CHIP DESIGN

A block diagram of the 16K chip is shown in Fig. 2. The chip is organized as four parallel sections of 4K bits each. Each section has its own data input and output pin. A decoder for each section selects one of the thirty-two registers in that section, resulting in only four registers being clocked on the chip at any one time. The active power dissipation is thus reduced, allowing clock drivers on the chip itself, resulting in a simpler device to the memory user. On-chip control logic can switch the chip into either a WRITE mode,

an NDRO READ mode, a R/M/W mode, or a data REFRESH mode. In the REFRESH mode the data is recirculated on-chip with the I/O circuits powered down.

Data rate is variable from 400 KHz to 5 MHz except in the R/M/W mode where the maximum data rate is 3 MHz. Data can be read successively into the same register or into adjacent registers with no loss of speed, although power dissipation will be higher in the latter mode due to the higher duty cycle of the address circuits. Data rate is continuous in all chip modes and all addressing patterns. Access time to a random register is 200 nanoseconds. The average access time is 12.8 microseconds, and the maximum access time to a random bit is 25.6 microseconds.

A picture of the chip is shown in Fig. 3. The chip is 201 by 219 mils, and is packaged in a standard 22 pin dual-in-line package. The chip dissipates 200 mW at a 5 MHz data rate, and less than 50 mW in the REFRESH mode. Only one 12V clock is required, which has a 200 pF capacitance load. All pins except the 12V clock are fully TTL compatible with no pull-up resistors required. The device has tristate outputs to facilitate paralleling the chips in a memory system.

32K BIT CHIP DESIGN

A block diagram of the 32K bit device is shown in Fig. 4. The device is identical in design and operation to the 16K bit device, except that it has only one input pin and one output pin for the entire chip. This is achieved by means of an additional on-chip decoding circuit which selects one of the eight simultaneously clocked registers for routing to the output buffer. The other seven registers are automatically recirculated on-chip. A picture of the device is shown in Fig. 5. The entire chip is 240 X 240 mils, and is packaged in an 18 pin ceramic DIP with 0.4 mil pin spacing. Clock capacitance is only 200 pF for a single clock line.

CHIP CONSTRUCTION FEATURES

Both devices share the same CCD structure, sub-circuit designs, and fabrication sequence as the Fairchild 9K CCD memory already on the market (CCD450). The CCD registers are two-phase n-channel buried

channel structures with overlapping polysilicon gates. A dual nitride-oxide gate dielectric is used, which places all gate electrodes on the same level of gate dielectric. Ion implantation through the first level polysilicon CCD electrodes generates the required asymmetry for two-phase operation. Dielectric isolation is used in the MOS support circuits to obtain higher packing density. The fabrication sequence requires nine photomasks, of which only two involve critical mask alignments.

Sub-circuits common to both devices include level shifters, decoders, line drivers, sense amplifiers, control logic, and I/O circuits. A dual differential sense amplifier is used as in the TI 4K RAM, with slight modification for sensing charge rather than current. Amplifier sensitivity is further increased by a novel capacitance decoupling circuit, which reduces the loading of the CCD outputs on the amplifier input node. The sense amplifier compares the charge levels in the selected register with a reference level in a dummy register located in each memory subsection. Since the reference level can be adjusted by geometric factors, threshold voltage tracking is achieved without the need for dedicated circuits. This feature, plus conservative design rules, permits wide operating margins and a higher device yield.

The present status of 16K chip development is characterized by the capability to produce small numbers (>100) of fully working prototypes at occasionally excellent yields (>30%). A large number of additional devices are fully functional except for one line or one section, indicating that further yield improvement is possible. Dark current is still a problem and, if not corrected, could restrict the temperature range to less than 50°C. Experiments with variations in process steps show promise for reducing the number of dark current spikes as well as the residual level of leakage charge, indicating that a temperature range of 0°C to 50°C may still be possible. Device modification and yield improvement is continuing under an AML contract (Ref. 2) as well as under company produce development funds. Sample quantities should become available to users by the early fall of 1975, with limited production quantities available approximately six months later. The device is expected to be competitive in a sizeable commercial market.

The development of the 32K bit device lags the 16K device by approximately six months. This is attributable to the greater complexity of the device, the tighter design rules, and larger chip size involved. It is possible that this device will be made available commercially also, although market volume maybe higher for the 16K device.

COMPETING 16K BIT DEVICES

Two other 16K bit CCD memory devices have been announced to date, the Intel 2416 device and the Bell Northern CC16M1 device. The Intel device is available commercially whereas the BNR device is basically a developmental prototype. However, both devices have characteristic features which can be contrasted with the 16K LARAM device.

INTEL 2416

A block diagram of the Intel CCD is shown in Fig. 6. The chip is organized into blocks of 256 bits which communicate with a single set of I/O pins through a 1 of 64 decoder, giving the chip a one bit swath. The decoder operates like a 64 bit RAM which transfers one bit at a time from each of the 256 bit registers. On-chip control logic determines whether the chip is in a NDRO READ, WRITE, R/M/W, or standby SHIFT cycle. Cycle time for the RAM decoder is 460 ns. for a READ or WRITE cycle and 620 ns. for a R/M/W cycle. Random access time for the READ cycle is 250 ns. to the first bit of a block. The minimum shift cycle period is 750 ns. This gives a maximum chip access time of less than 200 microseconds to any random bit, and a maximum internal shift rate of 1.33 MHz in the search mode.

The decoder can be used to read consecutive bits out of the same 256 bit block or consecutive bits out of successive adjacent registers. The first alternative requires one RAM cycle and one SHIFT cycle for each bit transferred, limiting the maximum data rate to 800 KHz for the READ and WRITE modes or 730 KHz for the R/M/W mode. The second alternative permits a higher 2 MHz data rate for the READ and WRITE mode and a 1.33 MHz rate for the R/M/W cycle; however, in this case the data rate is not continuous because each time the RAM is completely loaded, a SHIFT operation must take place to transfer the data to the CCD registers. Minimum refresh considerations

require further that a SHIFT operation occur at least every 16 RAM cycles at 70°C.

A picture of the chip is shown in Fig. 7. It is 143 X 237 mils long and is packaged in a standard 18 pin plastic DIP. The device has four 12 to 14V clock inputs, two with a 500 pF load capacitance and two with a 700 pF load capacitance. Total power dissipation is 600 mW at 1 MHz, which decreases to 150 mW in the 125 KHz standby SHIFT mode. Chip I/O lines are TTL compatible, although pull-up resistors are required. The chip inverts data from input to output.

BELL NORTHERN CC16M1

The BNR device (Fig. 8) is organized as four parallel registers of 4K bits each, with separate data input and output pins for each 4K block. Each block consists of two parallel SPS registers of 2K bits each which operate in a push-pull fashion. The SPS registers have a 16 bit input register and 32 parallel 64 bit registers half of which are loaded on alternate clock phases. The data rate at each I/O pin is 1 to 10 MHz, which implies an average access time of 0.2 to 2.0 milliseconds for each 4K block. The chip dissipates only 325 mW at a 10 MHz data rate and only 85 mW at a 1 MHz rate.

The chip generates all its own internal clocks and timing from a single 2-phase clock input. Clock swing is 0-12V and capacitive loading is only 60 pF on each clock line. On-chip control logic switches the chip to either a WRITE, R/M/W, NDRO READ, or an on-chip RECIRCULATE mode. Data and control lines are fully TTL compatible, with no pull-up resistors required. Chip size is only 137 by 170 mils. The device is packaged in a standard 16 pin DIP.

COMPARISON OF 16K DEVICES

A comparison of the three 16K devices is shown in Table 1. The widely ranging characteristics reflect the fact that the devices are directed at different market objectives. The Intel device is directed primarily at the head-per-track disk and drum market, where its faster access time should yield significant system advantages. The Bell Northern device is directed mainly at the MOS shift register market, where it can be used in CRT refresh, terminal storage and communications buffering type

applications. The Fairchild device is intended to be a general-purpose shift register type of device which will compete in both of the memory areas cited, but whose unique accessing capabilities might allow the exploitation of new memory system architectures.

Selection of the appropriate device depends strongly on the type of system contemplated. In a computer-type memory system, only a single bit, word, or block of information is accessed at any given time. The primary measure of memory performance is how fast the data can be made available to the CPU. Since only a small fraction of the system is active at any given time, standby power is the dominant feature. The larger the memory becomes, the more standby power must be emphasized.

For a serial buffer or signal processing type of system the primary measure of memory performance is the data transfer rate. Random accessibility is not a major advantage since the data sequence is rarely re-ordered. Most importantly, the fraction of devices active at any time is usually quite high, making the active device power the dominant factor. This is especially true in serial signal processing systems, where all devices might be active at any given time.

Fig. 9 plots the total power dissipation versus serial data rate for some candidate serial devices. The standby power is seen to be quite similar for all the devices, reflecting the fact that leakage mechanisms are similar for these NMOS type devices. At clock frequencies near one megahertz, however, the power dissipation differs greatly, reflecting differences in chip organization and in the ratio of capacitive loading to DC loading per bit. Clearly, the power savings can be substantial for large serial data systems if the new CCD memories are used.

Keeping these comparisons in mind the BNR device would likely be preferred for shift-register memory applications due to its high data rate, low power dissipation, small package size, wide temperature range, ability to string registers, and potential for low chip cost (ie. small chip size and standardized process). The Fairchild device would rank a close second with its more

complicated overhead requirements, smaller temperature range, larger package size, and more complex fabrication process. The Intel device would rank a distant third, with a heavy penalty attached to its discontinuous data rate, single bit swath, data inversion, and increased overhead requirements. Cost considerations based on volume sales capability could influence the preference somewhat if low system cost is a primary objective.

A different order of ranking results if a disk-type memory system is considered. Here, the Intel device is most highly preferred for its fast access time, single bit swath, short time to refresh, small package size, higher temperature range, and lower cost potential. The Fairchild device compares favorably, but is penalized somewhat for its four bit swath, lower temperature range, more complicated fabrication process, and either a long or an unconventional refresh cycle. The BNR device ranks third for its slow access time and long time to refresh. All three devices can be improved somewhat for a disk-type memory application through simple design modifications. Such modifications might include the sharing of a common I/O pin, decoding on-chip for a single bit swath, and in general, simplifying the chip interface requirements.

APPLICATION OF CCD's TO RADAR SIGNAL PROCESSING

Synthetic aperture radar systems are notorious for the digital memory capacities they require. A block diagram of a typical system is shown in Fig. 10. Essentially, the system collects high frequency radar returns at a low duty cycle, stretches them to achieve a lower bandwidth at a continuous duty cycle, filters the data to extract the imaging information, and presents the information to a display or recorder. Two memories are generally required, one in the processor and one with the display. With high resolution systems, these memories can reach capacities of 10^6 to 10^8 bits or more.

Figs. 11 and 12 show the detailed memory organization for a particular SAR processor known as Synthetic Aperture Precision Processor High Reliability (SAPPHIRE). This processor is currently being developed by Goodyear Aerospace Corporation under ASD/ABAL

sponsorship. (Ref 3.) The small rectangles in Fig. 12 represent 1 Kbit blocks of data. Each block stores data from consecutive radar returns and presents it to the complex multipliers sixteen returns at a time. In the accessible memory, each block receives new data every sixteenth return in an interleaved pattern. The entire memory is 23.6 megabits in size and dissipates 2350 watts.

Fig. 13 shows how the Fairchild 16K CCD can be used to replace the Intel 2401 2K bit shift register in the accessible portion of the SAPPHIRE memory. Since the non-accessible portion is purely serial storage, direct CCD substitution is a straightforward matter. The entire memory is therefore replaceable with CCD storage with no re-organization required. It is expected that the CCD version will dissipate one tenth the power, occupy 1/3 to 1/4 the volume, and weigh 1/2 to 1/3 as much as the present MOS shift register version. In production, it should cost 1/3 to 1/4 as much as the MOS unit.

COST POTENTIAL OF CCD MEMORY

The cost of CCD memory is bounded by the cost of MOS RAM's to less than 0.1 cents per bit. It is expected that CCD's can achieve even lower costs because roughly four times as many bits can be placed on the same size chip using the same process and design rules.

The projected cost of CCD memory is shown in Fig. 14. This projection by an independent consulting firm agrees closely with estimates from potential CCD manufacturers and large volume memory users. Table II presents a second independent assessment of CCD memory market size. It is still too early to tell whether CCD's will fulfill these optimistic predictions, but the potential is definitely there. Actual system experience will provide the answer over the next two to three years.

The following individuals and companies are acknowledged for their discussions of the status of CCD technology and for furnishing detailed descriptions of device operation: Gordon Moore and Sun-lin Chow of Intel Corp.; Mark Guidry, Gil Amelio, Henry Pao, and Kamil Gunsagar of Fairchild; and Doug Colton, Bill Coderre, and Neil Waterhouse of Bell Northern. Thanks also go to J. Decaire for a critical reading of the

manuscript and to Mrs. Penny Carpenter for typing the final version.

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3. Contract F33657-74-C-0604, entitled "Synthetic Aperture Precision Processor High Reliability (SAPPHIRE)", July 1974 to December 1975.
4. Quantum Science Corp., in Electronic Design 22, October 25, 1974, p. 43.
5. H.C. Wainright & Co., in Electronic News, February 5, 1975.

TABLE 1. COMPARISON OF 16K CCD MEMORY CHIPS

<u>CHARACTERISTICS</u>	<u>FAIRCHILD CD460</u>	<u>INTEL 2416</u>	<u>BNR CC16M1</u>
Organization (Swath/select/block size)	4/random/128	1/random/256	4/serial/4K
Operating modes	R,W,R/M/W,RECIRC	R,W,R/M/W,SHIFT	R,W,R/M/W,RECIRC
On-Chip recirculate	YES	YES	YES
Off-Chip recirculate	R/M/W (latch Req'd)	NO	YES
Required power supplies	+125V, +5V, -5V	+12V, -5V	+12V, +5V, -5V
Clock voltages	12V	12V	12V
Clock phases	2	4	2
Clock capacitance	120pF, 15pF	2 @ 500pF 2 @ 700pF	2 @ 60pF
Clock rep rate	0.5 to 5.0 MHz	0.1 to 1.3 MHz	0.5 to 5.0 MHz
Data transfer rate (per pin)	0.5 to 5.0 MHz	0.2 to 2.0 MHz*	1.0 to 10 MHz
Worst case access time	25.6μs	192μs	0.4ms
Average access time	12.8μs	96μs	0.2ms
Time to refresh	0.8ms	49μs	0.4ms
No. refresh clock cycles	4096	64**	2048
Temperature range	0°C to 55°C	0°C to 70°C	0°C to 70°C
Chip power (max)	200mW @ 5 MHz	300mW @ 2 MHz	325mW @ 10 MHz
Standby power	50mW	24mW	85mW @ 1 MHz
Output structure	Tri-state TTL Compatible	Open drain Pull-up resistor req'd	Tri-state TTL Compatible
Chip size	219 X 201	237 X 144	137 X 170
Package size	22 pin ceramic	18 pin plastic	16 pin ceramic
Process	ISO-NMOS(BC)	NMOS(SC)	NMOS(SC)
Start-up clear req'ts	8192 cycles	4096 cycles	43 cycles
Unique features	--	inverts data	--

* The data rate is interrupted every 16 cycles for a SHIFT operation.

** 128 cycles are required to restore the addresses to their initial state.

TABLE 2. MEMORY MARKET *

	<u>1973</u>		<u>1978</u>	
	<u>Qty.</u> <u>(Bill.</u> <u>Bits)</u>	<u>Value</u> <u>(Millions)</u>	<u>Qty.</u> <u>(Bill.</u> <u>Bits)</u>	<u>Value</u> <u>(Millions)</u>
Semiconductor				
Bipolar	16	\$250	80	\$ 500
MOS	45	208	280	565
SOS	--	2	15	65
CCD	--	--	60	45
TOTAL	61	460	435	1175
Magnetic				
Core	62	280	50	135
Plated Wire	8	135	15	155
Buble	--	--	10	20
TOTAL	70	415	75	310
Other	5	95	5	65
TOTAL	136	\$970	515	\$1550

Note: Total market, including captive production

*Source: Ref. 5

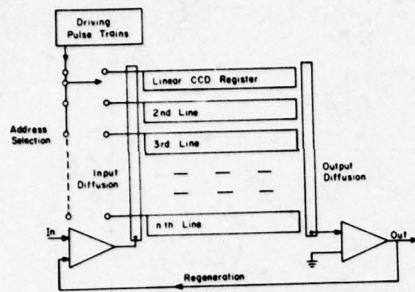


Fig.1. LARAM principle.

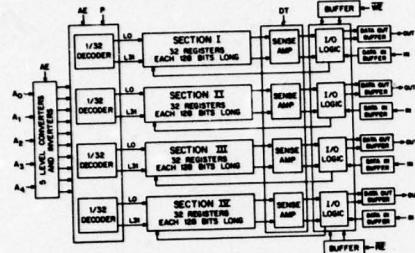


Fig.2. CCD460 block diagram.

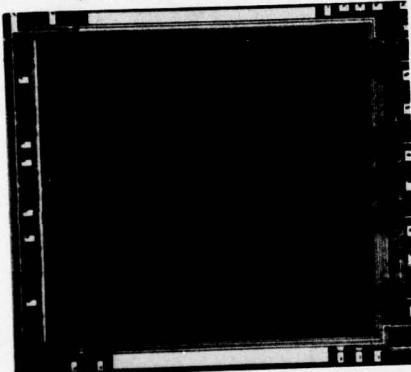


Fig.3. CCD460 chip.

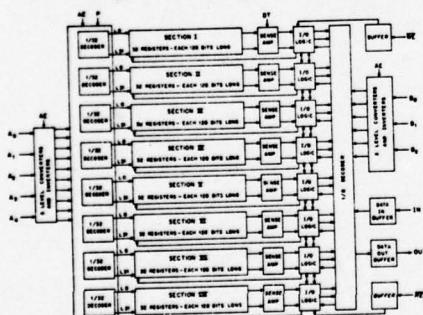


Fig.4. 32K block diagram.

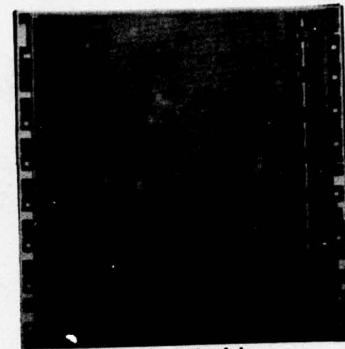


Fig.5. 32K chip.

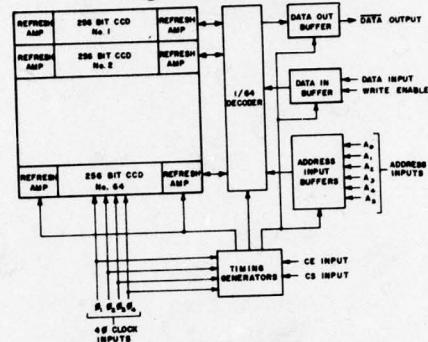


Fig.6. Intel 2416 block diagram.



Fig.7. Intel 2416 chip.

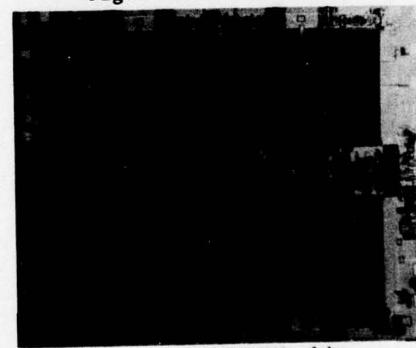


Fig.8. BNR CC16M1 chip.

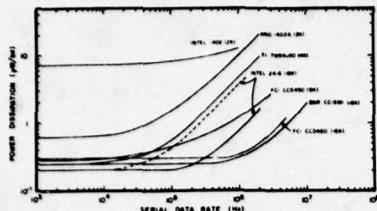


Fig.9. Active power vs. data rate.

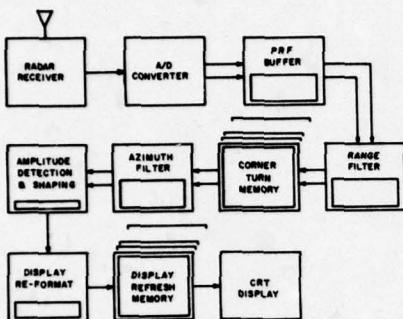


Fig.10. Typical SAR block diagram.

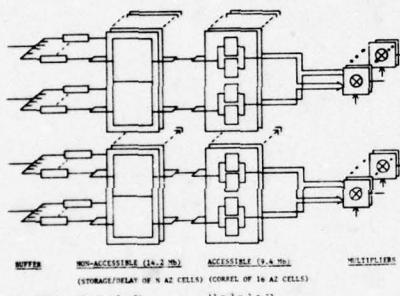


Fig. 11. SAPPHIRE memory organization.

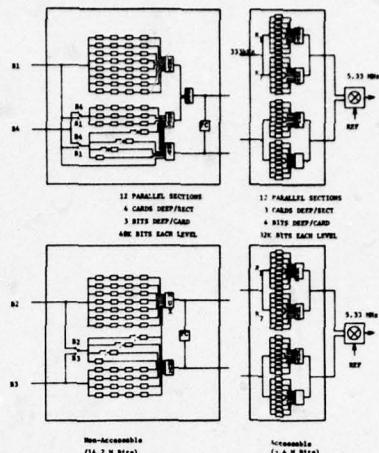


Fig. 12. SAPPHIRE circuit boards.

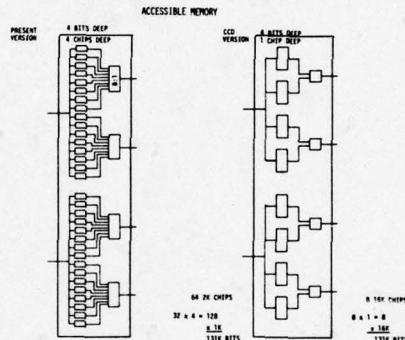


Fig. 13. CCD vs. MOS version.

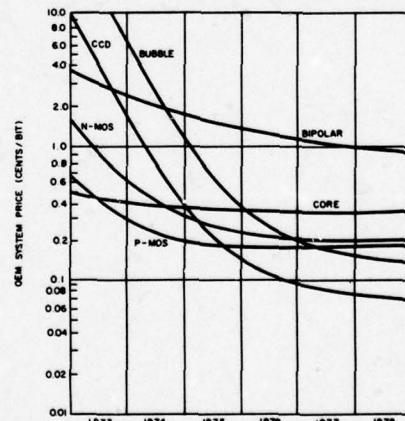


Fig.14. Projected CCD cost.

A 16 KILOBIT HIGH DENSITY CCD MEMORY

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ABSTRACT

The organization and performance of a 16,384-bit charge-coupled device (CCD) memory are described. The aim was to provide lower cost per bit of storage consistent with high data transfer rates, moderate access times and relatively low system operating power. The chip has dimensions of $136 \times 169 \text{ mil}^2$, to fit a standard 16-pin package, and is organized as four separate shift registers of 4096 bits, each with its own data input and data output terminals. A two-level polysilicon gate process was used for device fabrication. Three functional modes are provided: recirculate, read and recirculate, read and write, controlled by chip select and write enable control inputs which apply to all four registers together.

A condensed serial-parallel-serial (CSPS) organization was found to provide the highest packing density and lowest system cost per bit, but requires various clock waveforms. Most of these are generated on-chip, some operating at the serial transfer frequency and some at the parallel transfer frequency. Only two external clocks are required, driving capacitances of 60 pF each at one-half the data transfer rate. Operation at data rates of 100 KHz to 10 MHz have been demonstrated experimentally, the overall operating power at 10 MHz being less than $20\mu\text{W}/\text{bit}$.

1. INTRODUCTION

For the design of systems requiring digital memory, including memory hierarchies for large and small computers, the principal performance parameters, in order of importance are: access time (also called latency in serial memories), reliability, maximum frequency of data transfer, power per bit during normal operation, and standby power per bit in the case of volatile memories.

Comparison of the various available

technologies with regard to cost per bit as a function of access time leads to a relationship as shown in Fig. 1, illustrating the "access gap" in which there has been no technology which is both available and cost-effective within the computer memory hierarchy. Magnetic cores, bipolar and MOS RAMs have been fast but too expensive, while drums and disks were cheaper but too slow. MOS shift registers have found wide applications where small amounts of memory were

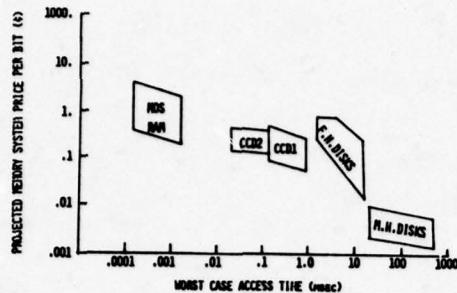


Fig. 1 - MEMORY SYSTEM PRICE VS ACCESS TIME

needed, for very small systems or for buffering mechanical devices such as disks whose speed cannot be usefully varied, but their cost per bit has been greater than for RAMs by a factor of two or more, when the access gap really needs something less expensive.

Discussions with many systems designers have indicated that the CCD serial memory technology can play a useful role in filling the access gap, eventually at lower system cost per bit than RAMs, yet offering performance that cannot be achieved using drums or disks. Many of the uncertainties which are inherent in cost predictions can be avoided by taking the MOS RAM technology as a benchmark, and taking into account the relative packing densities, process complexities, and expected yields. It is not to be expected that CCDs will compete directly with RAMs or with moving head disks, but the arrival of CCD technology will encourage re-evaluation of the trade-offs which determine the relative amounts of mainframe and disk storage in present-day systems. To allow for residual uncertainties, and to overcome inertia in establishing new products, a projected factor-of-two cost advantage over RAMs has been suggested as the minimum which is necessary to induce semiconductor manufacturer and systems designers to take CCDs seriously. The development of the 16K CCD memory to be described here was aimed at projecting a fourfold system cost advantage over RAM

systems, even if this required the acceptance of longer access times than those already achieved in CCDs, including block-addressable memories [1]. A number of such devices have been developed by various manufacturers and laboratories; most of them provide access to relatively small blocks of serial data, of typically 256 or 128 bits, although differing in maximum data rates, operating power, and system overheads for clocking, data transfer and data refreshing. The new 16K device described here, designated CC16M1, achieves a higher packing density by using an improved form of serial-parallel-serial organization using relatively large arrays of 2048 bits each, two such arrays being paralleled for each block of 4096 bits. Despite this large block size, the worst-case access time is only 410 μ sec at a data transfer rate of 10 MHz. However, this organization requires a larger number of clock waveforms, which therefore must be generated on-chip in order to minimize the number of external connections and to keep the system overheads low.

II. ORGANIZATION OF CCD CHIP FOR HIGH DENSITY STORAGE

Comparison of various alternatives led to the selection of a serial-parallel-serial (SPS) organization, which offers several advantages. Especially, these include greatly reduced clock power at high data transfer rates, since the SPS structure reduces the number of transfers experienced by each charge packet to a small fraction of what it would be for a purely serial shift register. Also, for any given set of geometrical layout rules, serial-parallel-serial (SPS) organizations offer high packing density because only one sense amplifier is required for a large array, such as the 2048-bit array chosen for the present design. This allows space for designing the sense amplifier to detect extremely small amounts of charge, and the CCD storage electrodes can be small, both for this reason and because the electrode dimensions are not limited by any need to pack the sense amplifier into the repeat spacing of every one or two parallel rows.

The packing density in the CC16M1

was considerably increased by the introduction of two improvements to the SPS structure. One of these was a two-phase interlaced organization of the serial-parallel and parallel-serial transfers, by which the serial registers are loaded and unloaded twice during every clock period of the main parallel array. Alternate rows of the parallel array are serviced on one occasion, and the alternate remaining rows are serviced on the other. Each serial register is required to store only half as many bits as there are parallel rows, which permits a reduction in the pitch spacing of the rows, as well as halving the number of high-speed transfers.

An even more significant increase in density was obtained by adapting the basic principle of the multiplexed electrode-per-bit (ME/B) organization, [2]. As originally described, serial strings of data are allowed to occupy adjacent storage locations, rather than occupying every other location, as in two-phase clocking, or every third location, as in three-phase clocking. The bits in each string must then be moved one at a time, making use of a single vacant location. The operation requires the application of a sequence of individual clock waveforms (ripple clocks) to the set of storage electrodes, and although such a sequence can be generated by ring counters situated along the edges of the array, this tends to limit the pitch repeat spacing of the electrodes of the parallel array to the density which can be achieved in MOS ring counters. Also, although the repetition frequency of each clock is low, the clock edges must be fast, because the transfers must take place one at a time.

In the CC16M1 these problems were avoided by identifying an optimum organization, adapting the ripple clock principle to short data strings of only three bits each, each string being separated from the next by a vacant location. A set of four clocks is then sufficient to drive all the storage electrodes of the main parallel array, and each transfer gate could also be driven from the same waveform as applied to the following adjacent storage electrode, as is done in ordinary two-phase clocking. However, another set of

four clocks is actually used for the transfer electrodes, since this enables "full-bucket" charge storage, increasing the amount of charge reaching each sense amplifier, with resulting increase in noise margins. All eight clock waveforms are distributed on buses along the edges of the storage arrays, from centrally-located clock drivers.

This combination of an interlaced serial-parallel-serial organization with a ripple-clock scheme characterized by the storage of short strings of data provides a high density of storage, for which the name "condensed serial-parallel-serial" or "CSPS" organization is suggested.

The choice of CSPS as the optimum organization for CCD memories is only justified if the array size is sufficiently large, otherwise the area occupied by the serial registers and sense amplifiers, and the power they consume, become disproportionately large. Fig. 2 illustrates the

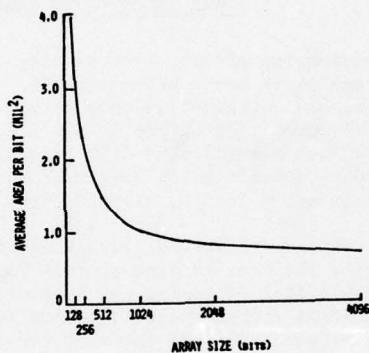


Fig. 2 - AVERAGE AREA PER BIT VS ARRAY SIZE IN CSPS ARRAYS

relationship between array size and average area per bit, for CSPS arrays having the same ripple spacing and multiplexing factors, cell dimensions, sense amplifier, and input and output buffers as used in the CC16M1. The averaging takes into account the areas occupied by the above circuit features, but does not

include the area occupied by the clock drivers, clock distribution buses, and other support circuitry, since these facilities can be shared by a number of arrays and therefore do not greatly influence the choice of size for each individual array. Fig. 3 illustrates the

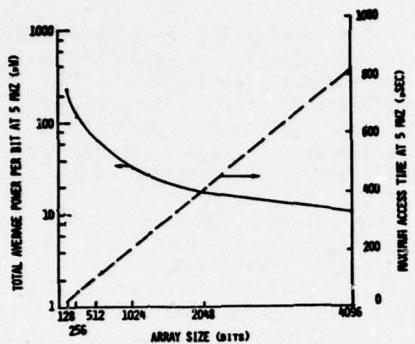


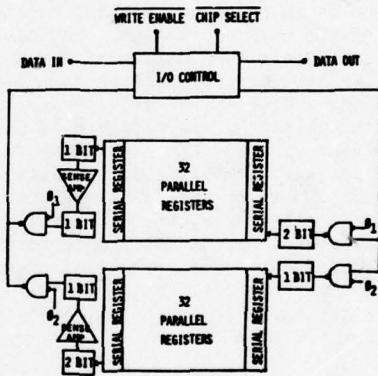
Fig. 3 - TOTAL AVERAGE POWER BIT AND MAXIMUM ACCESS TIME AT 5 MHZ RELATIVE TO ARRAY SIZE

corresponding effect of array size on average power consumption per bit. Once again, the contribution made by the shared support circuitry is not included. It may be seen that the CSPS organization is more favourable for larger arrays, containing at least 1 kilobit each.

In the geometrical layout which was chosen, the area of each storage location is 0.43 mil^2 , including the area of the associated transfer electrode and isolation between adjacent parallel rows. Allowing for the absence of a data bit in every fourth location, the effective area occupied by each bit stored in the parallel part of the array is 0.57 mil^2 . A multiplexing factor of 32 was chosen for the number of parallel registers in each array. Since two arrays are paralleled to make up each block, the effective multiplexing factor is 64 relative to the external data stream, so that at a data rate of 10 MHz the parallel clock frequency is only 156 KHz. Providing two paralleled arrays is considerably more favourable than providing a single array with 64 parallel

paths and the same overall block size, since the number of serial transfers experienced by each bit is halved, and the serial transfer frequency is also halved. An array size of 2048 bits was chosen, providing an average area per bit of 0.65 mil^2 for each CCD array, equivalent to $0.8 \text{ mil}^2/\text{bit}$ when the array support circuitry is included. Only a small advantage in area per bit and power per bit would have been achieved by choosing a larger array size than 2048 bits, while the access time would have lengthened in proportion. However, another reason for this choice was that it led to a quad-4K configuration on the 16K chip, which was convenient since a standard 16-pin package provides enough pins to permit individual input and output connections to each block, in addition to those required for the d.c. power rails, two external clocks and two control inputs.

Fig. 4 shows the organization of one



interleaving between the two arrays while enabling them to operate internally in the same phase with common clocks. The bit delay which follows each sense amplifier forms part of each data output buffer amplifier, and permits driving the output buffer at high speeds, while the sense amplifier is not loaded by excessive capacitance.

III. SUPPORT CIRCUITRY AND CHIP LAYOUT

A block schematic diagram of the on-chip clock generation circuitry is shown in Fig. 5. The external clocks θ_1 , θ_2

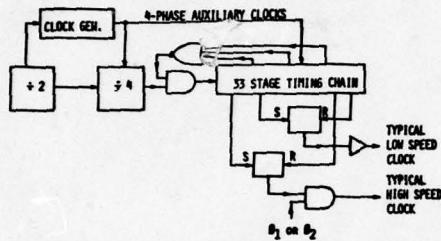


Fig. 5 - ON-CHIP CLOCK GENERATION CIRCUITRY

drive a divide-two counter, which in turn generates a set of four-phase clocks for operating the internal circuitry. A divide-4 circuit and feedback logic provide an impulse at the parallel clock rate into a 33-stage timing chain, which in turn provides impulses at the proper times to each of the clock waveform generators. Because of the three feedback tapings on the timing chain, the divide-4 circuit actually functions as a divide-16 counter. Each clock generator can be represented as a set/reset flip-flop, which is set by an impulse from one point on the timing chain, and reset from another point. Those clock generators which operate on the main parallel arrays must drive high capacitances, but are not required to switch at high speed. The clock generators which are associated with transfers into and out of the serial registers drive only small capacitances, but must generate fast edges to synchronize with the serial transfer processes. There-

fore, the MOS transistors employed in the output driver of each clock generator are all of comparable size, with channel breadth about 30 times the channel length. These provide more than adequate driving capability for the 16K memory. The counters, timing chain and clock generators have been designed to clear rapidly any illegal states which might be picked up as a result of external clock irregularities. The circuitry also recognizes a "start-up mode" whenever d.c. power is applied while both external clocks are low, which does not occur during normal operation. Following recognition of the start-up mode, the internal clocks will commence with predictable phases relative to the first turn-on of either of the external clocks, and input data can be supplied within 43 or 45 clock cycles, depending on which external clock turns on first. The sense amplifier at the output of each 2K array is a differential-input flip-flop, which was specially designed for this task because the requirements differ from those in MOS RAMs.

The CC16ML is provided with two control inputs, CHIP SELECT and WRITE ENABLE, and associated circuitry designed for operation up to 10 MHz data rate in three functional modes: RECIRCULATE, READ and RECIRCULATE, READ and WRITE. In READ and WRITE mode, the 4K blocks function as "straight-through" digital delay lines, which may be serially interconnected to form larger blocks with no penalty in maximum data rate. It was considered to be important that the CHIP SELECT would operate from ordinary 5-volt TTL signals, since these signals must be generated individually for all the memory devices which are OR-tied to common data buses. WRITE ENABLE requires a full clock level, but this is not a serious disadvantage because this signal can be supplied to a group of devices from a common driver. The physical layout of the memory arrays and support circuitry is shown to scale in Fig. 6

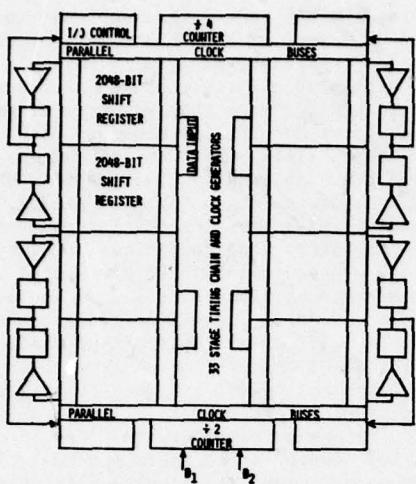


Fig. 6 - CHIP LAYOUT DIAGRAM OF THE
16,384 BIT CCD SHIFT REGISTER

APPLICATION IN SYSTEMS

The CC16M1, by requiring only two clocks, and handling continuous data streams at high speeds, has been designed for simplified application in memory systems. Suitable applications are likely to take advantage of the reduced access time compared to all fixed-head disks, with which a memory system built around the CC16M1 could, in volume production, be cost-competitive. Other applications, such as in video or radar signal processing, require large amounts of serial memory and in recognition of such applications the device was designed to permit serial interconnection between blocks on the same and on other chips, with no loss in maximum data rate. The 4x4K organization of the device is expected to be optimum for smaller systems. For large systems, there would be a preference for a decoded, block addressing (one out of four) scheme, so that only one bit of any word is stored on any chip. This would best be implemented using block addressing into a larger number of smaller blocks, which will be a logical extension of the present scheme. However, an alternative logical extension to chips of 64K size, with or without block-addressing, will be seen by many as being of greater importance in reducing system cost.

Acknowledgement

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**A Fast Access Bulk Memory System using CCD's/
A Recorder Buffer Memory using CCD's**

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ABSTRACT The 8K CCD shift register memory developed at Bell-Northern Research has been applied to two prototype memory structures. A disc replacement system using parallel storage and a block addressable serial storage buffer have been developed to study optimization of design techniques to achieve a wide range of data handling rates, system flexibility, and low power bulk memory systems.

Bell-Northern Research has developed programs to assess the feasibility of using CCD shift registers in bulk memory systems. An 8K CCD memory device was used in two systems, a disc replacement that could be used on a PDP-11 Unibus, and a block addressable buffer memory capable of handling a wide range of data rates. The first memory system, with a capacity of 64K words (1 M bit) was designed as a direct replacement for the DEC RS64 disc memory. It was used as a vehicle both to study the problems and system parameters associated with a CCD memory system and to compare operational performance with that of the disc memory.

The second system, which was contracted for by NASA Langley, required particular optimization techniques in applying CCD's to achieve wide data rates and low power operation. A discussion of these systems follows a description of design considerations using the 8K CCD shift register memory.

CCD DESCRIPTION

The designs of the memory systems discussed in this paper were influenced by the configuration and operational requirements of the 8K CCD that was developed at Bell-Northern Research. The charge coupled device configuration determined the design of the addressing network, the clock timing, and the read/

write sequence. The 8K CCD is structured as 32 recirculating dynamic shift registers (tracks) of 256 serial data bits each. In any system addressing scheme the 8 least significant address bits form a virtual address of the data location within each track and is determined by the count on an 8 bit counter. The 0 address is arbitrarily set the first time data is entered and is matched to that of the counter. The next 5 bits are applied to the address decoder inputs on the device; this permits random access to any track within one bit time. Bits of greater significance control access to the chip itself through the decoded chip enable (CE) inputs.

Two clock phases, ϕ_1 and ϕ_2 , are required to transfer data along the shift registers, while a third clock, ϕ_3 , controls peripheral circuitry on the chip. A typical CCD timing chain, considered to begin with the rising edge of ϕ_2 , is shown in Figure 1. It is important to note that a READ operation always precedes WRITE. The CE and Address which are set up for the READ during one timing chain (output data becomes valid during ϕ_3) is stored on chip in preparation for the WRITE command and DATA INPUT which occur during ϕ_2 of the next cycle (see Figure 1).

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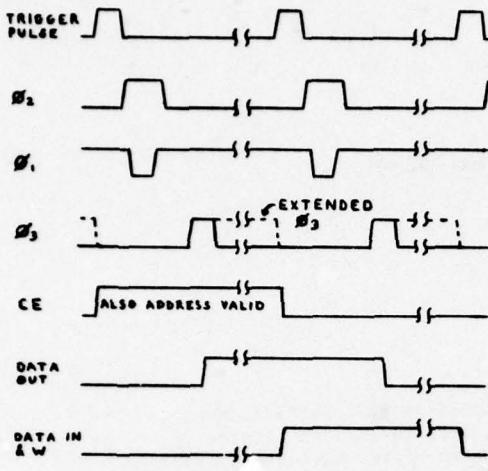


Fig. 1 Typical CCD Read/Write Cycle Waveforms.

Clock and control signal loading and level variation are critical parameters in CCD operation. The 8K clock phases Φ_1 and Φ_2 have a worst case loading of 700 pf. each. Rise and fall times are required to be at least 25 nsec, but not greater than 50 nsec for high transfer rates. To meet the requirements of high capacitive loading and high speed, MH0026 MOS clock drivers were chosen for both memory systems with a limitation of 4 CCD's per driver established. The Φ_3 clock has a capacitive loading of 150 pf. so that a driver can operate a greater number of devices. Since the address, CE, W, and data input lines have relatively small capacitive loads, 10 pf. or less, simple drivers such as TTL open collector gates or TTL-to-MOS drivers can be used to drive a larger number of devices.

A typical range of operation for the 8K CCD is shown on the Schmoo plot in Figure 2. The range remains relatively constant throughout the frequency specification for the device; that is, 10 KHz to 1 MHz. As a greater number of CCD's are driven by the same clock driver, the clock rise and fall times increase and the Schmoo plot tends to shift toward a higher substrate voltage requirement. Since the CCD has a broader range of

operation at 12 volts V_{DD} than at 10 volts, a better yield of devices is obtained at the higher operating point, despite a power penalty.

It must be kept in mind, however, that the majority of the power dissipation is in the drivers and not in the CCD itself. Driver power dissipation is derived from the standard power calculation:

$$P = P_{AC} + P_{DC} = CV^2f + VI \text{ (Duty factor)}$$

which contains a substantial DC component.

It is shown later how to manipulate the drivers and the timing chain to reduce driver power dissipation.

The power supply operating point for the disc replacement memory was selected as

$$(V_{DD}, V_{BB}) = (12, -5)$$

For the buffer memory low power operation was mandatory so that its operating point was selected as

$$(V_{DD}, V_{BB}) = (10, -3)$$

A device operating window of $\pm 5\%$ around the operating point was used over the required frequency range in selecting components; see Figure 2.

CCD DISC REPLACEMENT MEMORY

The first system that was designed to incorporate the 8K CCD was a disc replacement system with a capacity of 1 M bit. A block diagram of the CCD memory system is shown in Figure 3. The memory emulates the RC11/RS64 disc system and interfaces directly on the PDP-11 Unibus. The CCD Memory controller is much simplified compared to the RC11 yet retaining the same essential features.

The 1 Megabit memory is organized as 64 K words consisting of 16 parallel data bits and 1 parity check bit. An increase in word size requires only the addition of sufficient memory devices in parallel with the existing memory and extension of the address buses providing

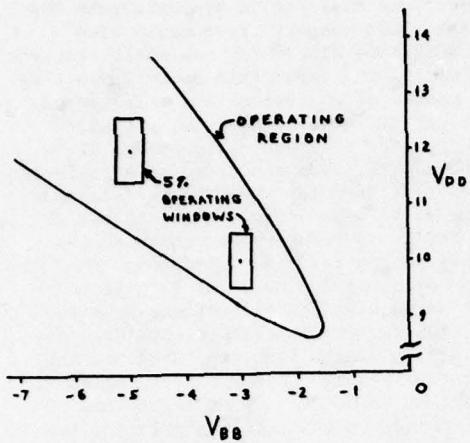


Fig. 2 Typical Operating Range of the 8K CCD.

for extremely flexible system design. Software access is permitted to any 32 word sector. Since all data is recirculating in 256 word loops maximum access time to commence transfer is 255 clock periods. Therefore at an operational clock rate of approximately 800 KHz, the average latency time is about 150 μ sec.

Three modes of operation are required:

1. Idle mode: to maintain data the CCD's are idled at 20 KHz and chip enable is inhibited.
2. Race mode: When a data transfer request is enabled the idle mode timing pulse is cleared and the virtual address of the data position on a track is incremented. This address is then compared with the 8 least significant bits in the disc address register in the controller. In case of mismatch the timing chain is triggered, data shifted one bit, the virtual address counter again incremented and a fresh comparison made.
3. Transfer mode: When the virtual address matches the start of transfer address that was set up in the controller, a WAIT condition is set up before the CCD timing chain is again generated.

From this point there are some differences between the WRITE and READ cycles. (see Figure 1).

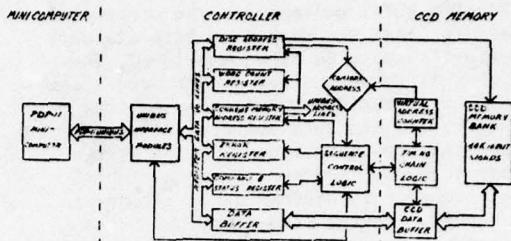


Fig. 3 Block Diagram of the Disc Replacement Memory

During a write cycle, the address match signal commands the INTERRUPT CONTROL MODULE to request (NPR) word transfer. When bus control is granted, the MASTER CONTROL MODULE brings the contents of the core location (as specified by the Current Memory Address register) into the controller data buffer. When this has been completed, bus control is relinquished and a TRANSFER REQUEST pulse is sent to the CCD memory logic. Upon receiving this signal, the memory logic reads the contents of the data buffer and triggers the CCD timing chain, thereby storing the data in the CCD memory. When the WRITE operation is finished, the CCD memory returns a TRANSFER REPLY pulse back to the controller. This pulse is then used to increment the three parameter registers in the controller; the current memory address register, the disc address register, and the word count register. After an appropriate delay to allow for propagation of the increment pulse, the RACE signal is again asserted and the cycle is repeated. The virtual memory address is now in step with the current word address pointer so that the WRITE cycle will repeat until the word count register overflows, indicating that the required number of transfers has been made. Since the controller addresses 32 word sectors, the number of transfers will always be a multiple of 32. At the end of a transfer cycle, the memory goes back to its slow speed IDLE mode.

During a READ cycle, when address match is detected, a TRANSFER REQUEST

signal is generated which triggers the CCD timing chain to enable a data shift and READ. As soon as the output data from the CCD becomes valid, it responds with a TRANSFER REPLY pulse which the controller uses to latch the data word into its data buffer. Once this is accomplished, the UNIBUS is requested for an NPR word transfer. When BUS CONTROL is granted, the contents of the data buffer are transferred into the core location specified by the current memory address register. When the transfer is acknowledged, the bus is released. At the same time, the three parameter registers are incremented. After allowance for propagation delay, the memory logic is again signalled to go back to the RACE mode. As with the WRITE cycle, the read cycle continues until the word count register overflows. Transfer rate for the CCD disc replacement memory is governed by the PDP-11 UNIBUS and is approximately 300K words per second.

Since the CCD memory is a prototype system, only simple error detection schemes, latency error and parity error were incorporated. A latency error signal is raised if during the data transfer mode an address match is completed but a TRANSFER REQUEST signal is not received with 50 usecs. The CCD timing chain must then be triggered to keep the dynamic memory refreshed, causing RACE mode to be reestablished.

During a WRITE cycle, a parity bit is generated from the data input and is stored as a 17th bit of the word. When data is read, the output data is used to generate a parity bit which is compared with the stored 17th bit. If they do not match, a parity error signal is asserted.

PERFORMANCE RESULTS

The three modes of operation of the CCD disc replacement memory demonstrate a capability not possible with magnetic disc memories. Not only can the memory stop temporarily at an address location to wait for a transfer request from the processor, but it can race to its start address at the beginning of a data transfer. The low speed during idle mode is used to conserve power.

Operating power of the CCD memory including controller and memory logic and

drivers was measured at approximately 100 watts. This compares favourably with the RC11/RS64 disc which nominally requires 250 watts and this ratio would improve as the number of equivalent discs increases. This design, however, was not optimized with respect to power consumption, since standard TTL, components and open collector gates were used for board interface and input drive lines (other than clocks) to the CCD's. Modular construction of the memory boards resulted in redundancy of open collector drivers. It is expected that a redesign using low-power Schottky TTL, CMOS devices, and TTL-to-MOS drivers for all CCD input lines would reduce the operating power of a 1 M bit system to less than 25 watts. Other techniques of saving power consist of manipulating the CCD timing chain and switching off the clock driver's power supply to reduce their D.C. power dissipation as will be discussed later.

Functional tests of the system included writing and retrieving text files from the CCD memory. Software programs on the PDP-11 were written to write data test patterns into the CCD memory. Every CCD chip that was used was previously tested for pattern sensitivity and frequency of operation on a Macrodata MD-104 memory tester. A continuous program of READ/COMPARE following the initial WRITE of test data was carried out with zero errors detected after weeks of continuous operation in which stored data was read and compared.

BLOCK ADDRESSABLE BUFFER MEMORY

Experience in the development of the CCD disc replacement memory enabled considerable design improvements to be applied to a different CCD memory structure. A buffer memory capable of accepting serial data with rates from 150 KHz to 4.8 MHz was developed under contract with NASA Langley. A low power memory with a randomly-accessible memory block structure was specified. A block diagram of the memory is shown in Figure 4. A typical use for this memory would be to accept bursts of data arriving from sources which may be clocked at widely differing rates, temporarily storing the data in separate blocks, then transmitting at a fixed rate selected blocks of data to a permanent store. Since serial data must

be stored in each memory block in a first-in-first-out basis, a CCD shift register memory is particularly suited for this application.

The system described is a feasibility model representative of a larger operation memory. Some of the problems that had to be overcome in the memory design were:

1. Accepting data rates over the range 150 KHz to 4.8 MHz with a CCD specified to operate only to 1 MHz.,
2. Synchronization of incoming data bursts with the virtual start address of partially filled memory,
3. Blocks of memory to be randomly accessible.
4. Power consumption for 100 K bits of data to be less than 2 watts in idle mode and under 6 watts in access mode.

In order to reduce the CCD clock rate and also maintain synchronism between independently accessed storage blocks four way multiplexing of the input data was used with high speed RAM's operating as a variable length input buffer to the banks of parallel CCD's. Thus data presented to the system at extremes of 4.8 MHz to 150 KHz is fed to the CCD memory at 1.2 MHz and 37.5 KHz respectively. Input data bursts of integrals of 1 K bits were used and all non-accessed CCD blocks were triggered at 1/4 the data rate to ensure that both stored data was kept alive and at the end of the data input the idle CCD's would have been clocked an integral number of 256 transfers to bring all blocks back into virtual address synchronization again.

Input data is collected in 4 bit nibbles from where it is written in parallel into 4 high speed RAM's. This action proceeds with the RAM address starting at zero and incrementing it after every 4 parallel bits have been written in. When the CCD virtual address reaches zero the RAM address is reset to zero and the data contained at that address is transferred in parallel to the 4 CCD inputs. Fresh input data then replaces this data at address zero following which both RAM and CCD addresses are incremented and the

READ/WRITE cycle repeated. The size of the RAM buffer is set at 4 x 256 bits and is determined only by the track length of the CCD and the level of multiplexing.

Special provisions are made to minimize the power dissipation. Low power Schotky TTL and CMOS logic are used with silicon on sapphire CMOS static RAM's to meet the necessary speed/power criteria. Specially selected CCD's with lower V_{DD} (10 volts cf. 12 volts nominal) were used with optimised timing waveforms. The major source of power dissipation lies in the clock drivers when their output is held low. Referring to Figure 1 the most important technique in saving power is a modification of the usual θ₁, θ₂ and θ₃ clock timing chain. The nominal 150 nsec. θ₃ width was expanded to a maximum consistent with the cycle time and in addition, this pulse was used to gate off the power supply to θ₂ which is held "low" over this period. Thus θ₁ and θ₃ drivers are held "high" in their low dissipation state while θ₂ driver dissipation is reduced by turning off the supply for a large part of each cycle, this is particularly beneficial during low speed or idle operation. Figure 5 shows a comparison of driver power dissipation as a function of frequency. All CCD address lines etc. are held high when the CCD is not being addressed and clocks to CCD's not containing data are held static.

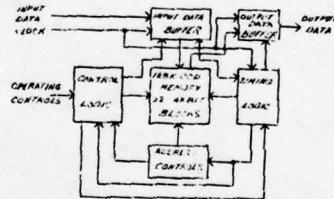


Fig. 4 Block Diagram of Buffer Memory.

Conclusion:

Bell-Northern Research has demonstrated the feasibility of applying CCD shift registers in both parallel and serial organized memory structures. The disc replacement memory was used primarily as a vehicle for studying the problems associated with driving large numbers of CCD shift register memories that have highly capaci-

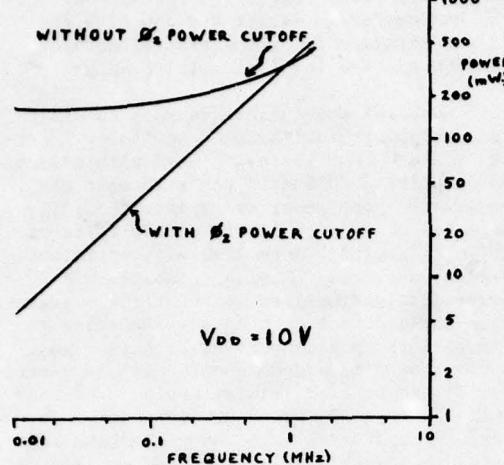


Fig. 5 Φ_2 Driver Dissipation vs. Frequency With and Without Power Cutoff Circuit.

ive clock loads. The memory is a parallel structure that demonstrates a latency period at least an order of magnitude less than magnetic disc memories. The data throughput is optimized to match the data transfer capability of the processor and

DEC Unibus. Total non-optimized system power is less than half that of the equivalent magnetic disc. Expansion of memory capacity and word length is facilitated by the parallel storage structure. Power consumption of this memory could be reduced greatly by a redesign using techniques that were incorporated into the second system design, a serial storage buffer memory. The buffer memory demonstrated the capture of data with a widely varying bandwidth, flexibility of access to any ordered set of memory blocks, and the feasible operation of a bulk memory system with extremely low power. Both of the systems were designed to provide ease of expansion of memory capacity, in size and number of words and blocks. The amount of peripheral circuitry and power consumption need be increased only slightly to handle large increases in memory capacity. It is expected that developments of CCD chips with larger capacities, higher data rates, and lower clock line capacitances will make CCD's increasing attractive in the design of memory systems.

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COST PERFORMANCE ASPECTS OF CCD FAST AUXILIARY MEMORY

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ABSTRACT Charge coupled devices (CCD's) have been mentioned as potential fast auxiliary memories in multiprogrammed computer systems with virtual memory. Declining MOS RAM costs will tend to allow computer designers to put more random access memory in their systems. However, due to program locality only a portion of the memory is actively used. If CCD's cost $R (> 1)$ times less than RAM's, the size of the random access main memory can be reduced and a CCD paging store can be provided as a back up. Active program segments can now be brought into the RAM as and when needed. Often the question has been raised in industry as to what value of R is needed to justify this application of CCD's.

A queueing network analysis is presented in this paper. The model developed is used to establish a criterion for cost-effectiveness. A relationship is derived between RAM/CCD cost ratio R and the page exception characteristics of the program environment. A rough rule of thumb is suggested. It states that cost-effectiveness is achieved provided the page miss ratio is less than σ , where σ is the ratio of the processor cycle time to CCD block read time. This criterion is applied to known miss ratio characteristics to obtain a critical value of R ranging from 1.2 to 2.0 for $\sigma = 0.005$ and 0.002 respectively. This indicates that a projected cost ratio of two to four can make fast auxiliary CCD memories attractive for block read times ranging from 200 to 500 microseconds.

INTRODUCTION

Several memory technologies with diverse cost-performance characteristics have emerged as potential storage media in digital computers. At the high performance end of the product spectrum, core memory, MOS and bipolar random-access-memory provide a medium for active program storage. Cheaper backing store is or soon will be available with magnetic disks, charge coupled

devices (CCD), electron beam addressable memories (EBAM), and magnetic bubble domain devices (MBD). Due to the significant price and performance difference between primary and secondary memory technology, computer designers have used multi-level storage hierarchies where the objective is to keep the current information in the fastest devices and the rest of the information in

Table 1
Cost-Performance of Competing Technologies (Circa 1978)

Technology	Access Time to First Bit	Typical Serial Block Size (Bits)	Maximum Serial Transfer Rate	Parallelism of Data Transfer Path	Cost/Bit (¢)
MBD	0.5 - 1.5 ms	256 - 2048	100 - 500 kHz	4 - 8	0.02 - 0.1
CCD	0.1 - 1.0 ms	256 - 1024	1 - 10 MHz	up to 8 or 16	0.02 - 0.1
MOS RAM	200 ns	1	2 MHz	8 - 64	0.05 - 0.2
EBAM	30 µs	1024 - 8192	10 MHz	1 - 8	0.02 - 0.1
FHD	Slow Med Fast	17 ms 8 ms 4 ms	1024 - 8192 1024 - 8192 1024 - 8192	2 - 5 MHz 4 - 6 MHz 4 - 24 MHz	0.015 - 0.020 0.025 - 0.030 0.100

the slower and less expensive devices. The individual cost and performance characteristics and the user environment (program behavior) will affect the optimal memory system design. This paper presents an overview of the cost-performance characteristics of some of the technologies and identifies the computing environment best suited to them. Moving head disks (MHD) are generally too slow for active program auxiliary storage. They are a secondary memory to store inactive program segments or files. Fixed head disks or head per track drums have been used as fast auxiliary memory between primary and secondary memory.

COMPETING TECHNOLOGIES

The different technologies can be functionally classified into Random Access and Block Access Memories. In RAM's, each bit of storage is indi-

vidually accessible; in BAM's, the smallest accessible unit is a serial stream of bits. Table 1 summarizes the typical cost-performance characteristics of memory systems using various technologies [cf. 1]. Some of the non-quantitative features of these technologies are discussed below. The traditional BAM market is served by magnetic disks while core memories are most commonly used as RAM's.

Magnetic Bubble Memories

Magnetic Bubbles* provide non-volatile block access storage, competing directly with fixed-head disks. If the projected cost estimates are met, MBD's should virtually capture all the market for small capacity (< 10M bits), low access time FHD's. They also pose a serious threat to the medium per-

*This paper is concerned only with large bubbles (5 µ in diameter).

formance FHD's because they offer greatly improved performance at comparable prices. The market for large FHD's (> 100M bits) with relatively slow access times will not be significantly affected as they have a price advantage of a factor of two or three over MBD's. An important feature of MBD's is their modular expansibility. Users will be able to upgrade relatively easily the capacity of their storage to meet increasing requirements. Their non-volatility gives them an edge over CCD's. However, in fast auxiliary memory applications, volatility could be tolerated due to the existence of backup storage in the form of a moving head disk. Note that a three-level hierarchy is not necessary for MBD's and FHD's in small computer systems. The stopability and asynchronous operation of MBD's can be exploited in future computer architectures.

Charge Coupled Devices

CCD memory has the best potential for very high speed operation. Most current computers are not designed to handle fast peripheral devices, and novel architectural ideas are needed to exploit their high performance. Future super computers (a la IBM 360/195, Texas Instruments ASC, and CDC 7600) could take advantage of this technology. The best application area is in small capacity and/or high performance storage. CCD's are easy to interface and can be made modularly expandable. Their cost per bit will be approximately two to four times less than the prevailing MOS RAM cost [2]. In conjunction with a RAM buffer, CCD's can be used to provide cost-effective fast auxiliary memory in computers where a large low-cost virtual

address space is desired at an accompanying small degradation in overall computer speed. The pervasiveness of this market will depend strongly on the price ratio of CCD's to RAM's. CCD's can also be used very effectively as an intermediate level storage between fast RAM's and slow, inexpensive moving-head disks.

Fixed-Head Disks

Fixed head disks can be broadly classified into three categories: low capacity/high performance, high capacity/low performance, and medium. The high performance disks usually provide multiple heads per track to reduce the access time. Increase in transfer rate can be achieved by using more than one read/write head in parallel. The average FHD has only one head per track and accesses a single track at any given time by electronically selecting a read/write head. The price increase associated with multiple heads per track and parallel transfer is significant and restricts the capacity to less than 20 megabits. Advances in integrated head assemblies could drive the cost of FHD's down. These disks should eventually be displaced by a less expensive technology like magnetic bubbles or high density MOS RAM's. The high capacity, low performance FHD's will be replaced by MBD's in applications where higher performance at a comparable cost is needed. The modularity of MBD's will also affect the market. If the projected 20 millicent price/bit is achieved for MBD's, the medium FHD market will be seriously threatened. CCD's offer competition at the high performance end if volatility can be tolerated.

Electron Beam Addressable Memories

Electron Beam Addressable Memories (EBAM) are a potential candidate for high capacity fast auxiliary memory. The storage medium is capable of retaining data for over a month in the absence of power. In order to achieve a low cost/bit storage capacity has to be in the vicinity of 100 million bits. This would restrict the applicability of this technology to applications requiring large capacity, low access time and high data rates.

Random Access Memories

Core is being slowly replaced by semiconductor random access memory. Though MOS has little speed advantage over core, declining costs of LSI memories will make MOS RAM prices comparable to core prices. For this reason core memories will not be considered in this paper. The single transistor per cell MOS RAM has the best potential for high density random access main memory. Declining RAM costs will affect the market for the serial access memories. As RAM costs go down computer designers will tend to put more RAM in their systems, thereby reducing the need for fast, expensive serial access memories. The total system cost-performance may well be better served by an inexpensive medium performance secondary storage.

SYSTEM PERFORMANCE

This section describes a methodology for evaluating the effect of various memory hierarchy alternatives on the overall system performance measured in terms of the instruction execution rate. A simple model of a multiprogrammed computer system

with a two-level hierarchy will be presented.

Multiprogramming refers to allowing the central processor (CPU) to switch from task to task in order to achieve good utilization of all resources. Typically, a given task is allowed to execute until it requires information from the backup storage or any I/O peripheral. While information is being transferred from secondary storage to primary memory, the CPU performs a task switch and starts execution of another task which references only the primary memory. The degree of multiprogramming is the number of jobs, tasks or processes actively using the main memory resources of the computer system. A discussion of the optimal degree of multiprogramming and its effect on system performance is beyond the scope of this study.

As mentioned earlier, declining RAM costs will tend to increase the size of main memory. However, due to program locality [cf. 3] only a portion of main memory is actively used. The availability of low cost paging devices may offer a cost-effective alternative to the system designer. A smaller main memory can be used in conjunction with a paging store or fast auxiliary memory (FAM) to achieve the same performance as the case in which the entire program resides in main memory. Criteria for cost-effectiveness are explored in this section.

Consider a multiprogrammed computer system C. In this system the entire program is loaded into main memory from a peripheral device like moving-head disk or tape unit. A program is executed until interrupted by the occurrence of an I/O

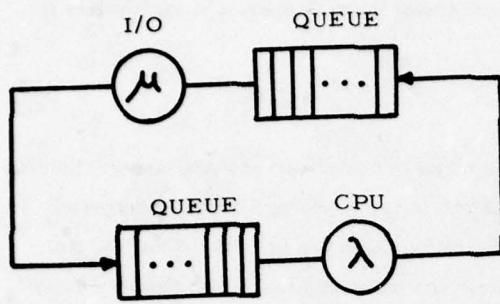


Figure 1 : Queueing model of a multi-programmed computer system

request to a peripheral device or program termination. Figure 1 shows a queueing model of such a system. This analysis assumes the service times of the CPU and I/O servers to be distributed exponentially with mean $1/\lambda$ and $1/\mu$ respectively.*

The CPU utilization, U_c , is given by

$$U_c = \frac{1-p}{1-p} \frac{M}{M+1} \quad [\text{cf. 4}],$$

where $p = \frac{\lambda}{\mu}$, and M is the degree of multiprogramming. M is assumed to be equal to 8 for this analysis. The average execution interval is given by

$$\frac{1}{\lambda} = 1 \times t_u$$

where t_u is the average time interval between successive memory accesses, and, 1 is the number of memory references between I/O requests.

*This assumption is widely used in the analysis of the performance of computer systems. It simplifies the mathematics involved while providing useful insight into the dynamics of the queueing phenomena.

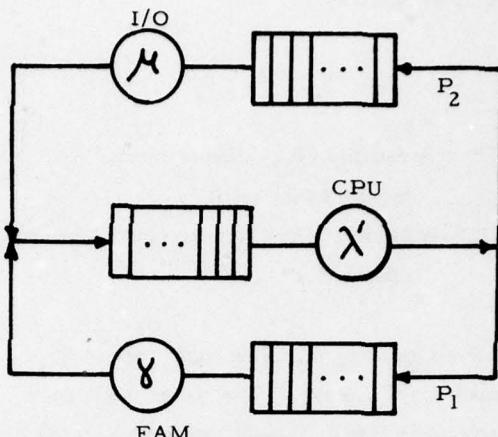


Figure 2 : Queueing model of a paged multiprogrammed computer

An alternate system design, C' , that uses paging, can be modeled by the queueing network is shown in Figure 2. The cost per bit of main memory is $R (> 1)$ times the cost per bit of the paging store or fast auxiliary memory. In this system execution is terminated by an additional event called page fault. The main memory in this system is smaller than the program size. Only a fraction, f , of the program resides in main memory. A page fault occurs when the program references a page not currently in the resident set. Page faults are characterized by the probability of their occurrence -- sometimes also referred to as miss ratio, α . The average number of memory references between page faults is $(1-\alpha)/\alpha$. The rate, δ , at which the CPU accesses the paging store is given by

$$\delta = \frac{\alpha}{1-\alpha} \times \frac{1}{t_u} .$$

Thus, in Figure 2,

$$\lambda' = \lambda + \delta ,$$

P_1 = Probability { Execution terminated due to page fault } = δ/λ' ,

P_2 = Probability { Execution terminated for other I/O } = λ/λ' .

The service rate, γ , of the paging device is equal to $1/T$, where T is the sum of the latency and transfer times. General expressions for the equilibrium distribution of jobs in such networks have been obtained by Gordon and Newell [5]. The use of these expressions gives the utilization, U'_c , of system C' as

$$U'_c = \frac{\sum_{i=1}^M (x^i - y^i)}{\sum_{i=1}^{M+1} (x^i - y^i)}$$

where $x = \frac{\lambda}{\mu}$, and $y = \frac{\delta}{\gamma}$.

Note that when a page fault occurs it may be necessary to restore a currently resident page into the paging device before a new page is brought into main memory. In this analysis, such a page fault will be considered equivalent to two page faults. Also, by definition, when α approaches zero the page fault rate δ goes to zero.

Let α^* be the miss ratio for which U'_c is within 5% of U_c . Let the corresponding fractional size of the resident set be f^* (<1). Then, the system C' has the same cost as system C, if the per bit

cost ratio of the main memory to paging store is

$$R^* = \frac{1}{T-f^*} .$$

Note that this simplified analysis does not include the cost of implementing a memory management scheme for the paging activity. Thus, the cost advantage has to be greater than that mentioned above in order to justify the added complexity. The value of R^* can be calculated from known miss ratio characteristics of program environments.

The value of α^* is a function of U_c , the utilization of the unpaged system, and the product $\gamma \cdot t_u$, denoted by σ . Figure 3 is a plot of U'_c against α for $\sigma = 0.001$ and U_c varying from 0.5 to 0.9. Similar curves can be plotted for other values of σ . Based on these curves an approximate rule of thumb can be stated that the critical miss ratio, α^* , is almost equal to the value of σ for less than 10% degradation in performance. The corresponding value of f^* is a function of program behavior.

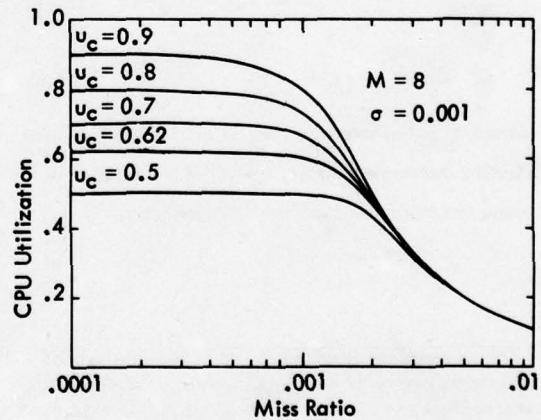


Figure 3. Performance of a Paged System

Table 2.
Critical Miss Ratio

u_c	Critical Miss Ratio α^*		
	$\sigma = .005$	$\sigma = .002$	$\sigma = .001$
0.9	0.003	0.0013	0.0007
0.8	0.004	0.0015	0.0008
0.7	0.005	0.0020	0.0010
0.6	0.006	0.0023	0.0012
0.5	0.007	0.0030	0.0015

CCD memories are expected to be between a factor of two to four times less expensive than equivalent MOS RAM's [2]. Let us assume that the memory management scheme is implemented in hardware at a cost of 10% of the original memory cost. If R is equal to 2 then cost-effectiveness is achieved for environments where $f^* < 0.65$. Table 2 shows the value of α^* that must be achieved at the above mentioned value of f^* .

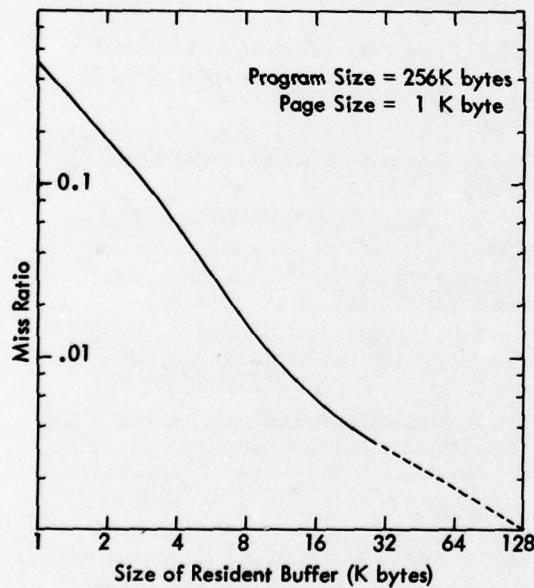


Figure 4. Mattson's Miss Ratio Characteristic

Table 3.
Minimum Cost Ratio for Cost-Effectiveness

u_c	Minimum Cost Ratio R^*		
	$\sigma = .005$	$\sigma = .002$	$\sigma = .001$
0.9	1.29	1.92	5.18
0.8	1.23	1.69	3.51
0.7	1.21	1.47	2.5
0.6	1.19	1.38	2.02
0.5	1.18	1.29	1.69

For a given program environment this analysis can be used to predict the minimum cost ratio R^* required for cost effectiveness. Figure 4 shows the miss ratio characteristics of Mattson [6]. Table 3 shows the minimum value of R for various system configurations. Once again, a 10% cost is attributed to memory mapping; i.e., $R^* = 1/(0.9 - f^*)$. Since the critical cost ratio ranges from 1.2 to 5.0 , CCD's are likely to be attractive paging devices if the projected cost ratios of two to four are achieved for $\sigma > 0.002$. For typical values of t_u equal to 0.5 and 1 microsecond, this corresponds to a block read time of 250 to 500 microseconds. For CCD register lengths of 1K bit this can be achieved with data rates near 5 MHz.

Further performance improvements can be obtained by maintaining some of the frequently used files such as system tables and directories, compilers, and utility programs in a fast access device such as CCD's. This reduces the request frequency to the file system which is usually a moving-head disk with access times ranging from 30 to 100 milliseconds. Thus, the CCD now acts as a buffer between the CPU and the file system. Table 4 shows the

Table 4
Performance Improvement due to Buffering
of Systems Software

CPU Utilization u'_c					
q	0.9	0.8	0.7	0.62	0.5
0.0	0.9296	.8516	.7641	.6825	.5533
0.1	.9610	.9058	.8321	.7544	.6194
0.2	.9817	.9795	.8971	.8319	.6995
0.3	.9930	.9782	.9492	.9053	.7925
0.4	.9979	.9929	.9814	.9602	.8875

q = Probability of finding system software
in CCD buffer

improvement in utilization due to the CCD buffer when the buffer satisfies a fraction q of all requests to the file system. This improvement is insensitive to the access time of the buffer provided it is at least a factor of 10 better.

The two approaches outlined in this section can be combined to increase the effective size of the main memory. Any performance degradation due to paging can be compensated by the improvement due to permanent residence of certain systems software on the fast paging device.

CONCLUDING REMARKS

The analysis presented in this paper makes many simplifying assumptions in order to derive some general results. There are many page allocation strategies for multiprogramming systems with virtual memory [7]. These strategies are used effectively to obtain the most efficient use of system resources [8]. Some of the issues involved are optimal page size, optimal degree of multipro-

gramming, time slicing, dynamic memory allocation, page replacement strategies, and scheduling. These problems can be analyzed for more specific system architectures.

A cost ratio of two to four for block read times of 200 to 500 microseconds is likely to result in lower memory system cost using a fast auxiliary memory. The amount saved depends on the size of the memory. The ultimate attractiveness of that cost saving depends on its magnitude relative to the overall system cost.

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A CCD - BASED TRANSIENT DATA RECORDER*

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ABSTRACT The recording of analog transient data in a digital form at high bandwidth presents technical challenges in many areas. A variety of techniques lend themselves to the task at hand. Each technique presents unique challenges derived from overall system performance requirements. One particularly attractive technique involves the use of an Analog Shift Register (ASR) for time conversion in order to minimize high-speed components.

After appropriate filtering, transient data is sampled and sorted in the ASR at a high rate as analog samples. After the transient, data is shifted from the ASR at slow rate through an analog to digital converter to a digital memory for temporary storage. Upon remote command, the data is then read nondestructively and transmitted at a convenient rate to a remote location for permanent storage and analysis. The transient data recorder being developed will sample and store 1,000 six-bit words of 100 MHz data with a sampling aperture of +50 picoseconds. Since data is slowed after acquisition in the ASR, the remainder of the recorder is comprised of standard TTL integrated circuit logic.

The ASR consists of eight interleaved CCD's. Each CCD is capable of storing 128 data samples acquired at input rates ranging from 312.5 Ksamples/sec to 62.5 Msamples/sec. Operating eight CCD's in an interleaved fashion provides storage for 1024 samples of analog data acquired at combined rates of 2.5 Msamples/sec to 500 M samples/sec. The necessary CCD was not available initially but was developed under subcontract to GARD, INC. by Rockwell International, Electronics Research Division. Two other papers presented at this conference provide details on the CCD itself⁵ and the circuitry required to operate it in the manner required⁶. After acquisition, CCD operation is slowed to a convenient output rate of less than 100 Ksamples/sec per CCD or 800 Ksamples/sec per ASR.

INTRODUCTION

The purpose of a data acquisition system is generally to provide information about a system to the user. The nature of the information required varies widely. Simple yes/no or go/no-go data is often appropriate for operational control. Elaborate tables and graphics resulting from sophisticated data processing procedures are sometimes required for scientific research. While the data requirements for operational control and scientific research may vary by orders of magnitude, there is an important element common to both. The user in both

cases wants to see only relevant data.

The control operator may need to know how many times a process exceeds its threshold temperature as well as when each instance occurred. A simple printout stating the number of occurrences followed by a list of the time of day when each instance occurred is appropriate. The operator has little use for a tabulation of temperature data listing entries every minute. Further, he cannot afford the time required to delve through copious data separating meaningful results from meaningless records. Clearly, the

* This work was performed by GARD, INC., a Subsidiary of GATX Corporation, under Contract to Sandia Laboratories, a prime Contractor of the Energy Research and Development Agency (ERDA).

required sorting of records is better accomplished by the data acquisition system operating in accordance with some rules set down by the operator.

The scientific researcher is often faced with a similar situation. The phenomena under study may be characterized by short bursts of relevant data separated by relatively unimportant background phenomena. While the background phenomena are essential in establishing "steady-state conditions" or "base-line" data immediately before and after the event of interest, their continuous presentation to the user serves no useful purpose. Once again, some sorting of relevant and irrelevant data is required of the data acquisition system.

In general, when the information rate or meaningful, relevant data rate is significantly non-constant, the data acquisition system is required to continuously monitor the phenomena and extract the relevant data for the user. Depending on the application, continuous data may or may not be filed historically by the system. Initially, most users request complete historical records as back-up or reference for the extracted data. This procedure can result in copious data if the phenomenon of interest requires wide-band recording techniques. For example, consider the pulse data presented in Figure 1, which is typical of numerous phenomena. The pulse spans roughly 500 μ s. The user has chosen to sample this waveform at 50 Ksamples/second or at 20 μ s intervals, producing samples of each point indicated. The pulse is represented with approximately 26 samples. In addition to the pulse itself, the user has requested approximately half a pulse width of baseline before and after the pulse, raising the total data required to approximately 50 points, or 1 ms (1000 μ s) of recording. Now consider how much data must be recorded to obtain the 50 samples required if real time processing is not employed. Assume this data represents a shock wave generated by an explosive detonation occurring 1000 feet from the point of measurement. Assume the detonation is used as the time reference for the experiment. The shock wave will travel at the speed of sound traversing the 1000 feet in roughly one second. Barring all other considerations, then, at least one second of data must be

recorded to acquire the pulse and its time reference. Given some uncertainty in the speed of sound (which is a function of air temperature, humidity, and barometric pressure), perhaps two seconds of good recording time will be used. Note that in the recording period only 1 ms (50 samples) of data plus the instance of occurrence is truly relevant. That is, 50 out of 100,000 samples recorded are relevant, or 99.95% of the data is irrelevant. To this point other factors which extend the recording period have not been addressed. For example, if the recorder requires some sort of speed stabilization, it may begin as much as one minute before detonation. If some other data occurs five seconds after detonation, then the total period extends another four seconds. If, on the other hand, the data occurrence is largely unpredictable, then the recording must span a large enough period to record the data whenever it occurs. It takes little imagination to envision the percentage of irrelevant data growing from 99.95% to 99.995%, or even greater. Still, in this example, the data is recordable with conventional techniques. General purpose equipment can record and/or sort out the relevant data either in real time or from the tapes after the event.

Generically, data acquisition systems which sample and record the kind of data discussed are called transient data recorders. Transients have been traditionally defined as "fast" events occurring randomly in time. From the examples presented, it is appropriate to regard transient data as data characterized by short periods of highly concentrated information spaced by long periods of low information density. The function of a transient data recorder is to detect and record information concentrated in short periods together with sufficient base-line and time data to provide a reference for the user. Transient recorders are usually characterized by data identification via real time data processing and electronic memory sufficient only for the transient itself and data denoting its time-of-occurrence. Note that a transient recorder is not necessarily a wide-band device.

SYSTEM REQUIREMENTS

Now let us consider the data typical for the system under consideration. The data is generally of the same shape as the

pulse already discussed (see Figure 1). However, it is more than 10,000 times faster. The data contains significant frequency components from DC to 100 MHz. Sampling is required at 500 Msamples/second, or at 2 ns intervals. The trailing edge of the waveform is often more than ten times longer and can contain additional wide band data requiring 500 to 1000 samples. Since the user requires a system accuracy of $\pm 2\%$, $\pm 1/2$ LSB, the data must be resolved to 64-levels and encoded to six-bits. Whereas the previous data was manageable with conventional recording equipment, the required sampling rate and subsequent data rate are so high that unconventional techniques are required. In addition to these functional requirements, the recorder must remotely operate in a severe environment characterized by temperatures varying from $+100^{\circ}\text{F}$ to $+1300^{\circ}\text{F}$, shock up to 30g's ($1/2$ sinewave, 11 ms), and pressures from sea level to 10,000 feet. It must operate through a combined radiation environment of 10 Rad prompt dose acquired at 10^7 Rads/sec plus 10^7 neutron/ cm^2 , fission spectrum. EMP is considered best described as up to 2 amperes of sheet current containing significant frequency components up to 100 MHz flowing over the module. The recorder must be small (approximately 400 in^3) and low in power dissipation (less than 40 watts). Since the module may be expended in one out of four uses, it must be low in cost. Sampling rate, signal offset, and pre-history (or time-offset) are all remotely programmable. More details on the specification are presented in Table 1.

APPROACHES

The classical approach to transient data recording centers about an analog-to-digital converter linked to digital memory as shown in Figure 2. Data is first filtered to eliminate aliasing, and then accurately sampled and held in analog form for conversion to digital. The linear phase filter is not an off-the-shelf item, but can be fabricated from standard components to conform to the size and power constraints. The sample and hold must maintain an aperture or time uncertainty of sampling of 50 ps (in order to maintain six-bit accuracy for 100 MHz) while operating at 500 Msamples/second. The requisite sample/hold approaches the state-of-the-art but is not large and does not require excessive power.

The 500 Msample/second, six-bit analog-to-digital converter is currently beyond the known state-of-the-art. The general approach taken to converters approaching this speed and resolution is to simultaneously apply the signal to parallel fast-setting analog comparators as shown in simplified form in Figure 3. Each comparator is biased at one of the 63 resolvable levels. The signal is held until all circuitry is settled and the coded output is stored. Additional speed is obtained using additional interleaved rows of comparators. A recent developmental six-bit converter using two parallel rows of converters was operated at 200 Msample/sec¹. The converter with Sample/Hold requires 175 watts and is housed in a rack mountable enclosure judged to occupy more than 3000 in^3 . While its production cost is not known, the circuitry makes extensive use of both custom and standard ECL logic which does not suggest low cost.

Clearly this converter is too slow (200 Msample/sec vs. 500 Msample/sec), too large (3000 in^3 for converter plus sample/hold vs. 400 in^3 for the total system), dissipates too much power (175 watts vs. 40 watts for system), and is not likely to be low cost.

Following the converter is storage for 1000 words of six-bit data, which must be loaded at 500 Msamples/sec. From manufacturers data sheets it appears that an array of 48 ECL memory chips² will meet requirements. However, each chip requires 90 mA, typical, @ -5.2V with inputs and outputs open. This amounts to 0.468 watts per chip or more than 22 watts for the 48 chip array. Note that this power does not include the addressing or control functions.

It is clear that the classical high speed transient data recorder falls far short of the design goals. The overwhelming weak point is the analog to digital converter. Therefore, a method which circumvents the high speed, parallel analog to digital converter must be used.

One unconventional form of analog to digital converter is the scan converter. The scan converter can be thought of as similar to a sophisticated oscilloscope. Wideband data (up to 1 GHZ) is written in x, t form onto a special target which retains the trace. The target is then scanned

at slow speed in such a manner that for each increment of time, the value of the input (X) is encoded. Commercially available equipment³ offers input bandwidth to 500 MHz at low levels (1 GHz at high levels), with resolution at 400 by 320 lines converted to a 512 by 512 digital array. The conversion results in 512 samples resolved to nine bits which are stored in digital memory. The basic unit dissipates 243 watts and occupies approximately 2500 in³. From the manufacturers literature, there is no indication that the unit is hardened for shock or radiation. However, it will operate over a temperature range of 0°C to +40°C and up to an altitude of 15,000 feet. Although not usually sold as a stripped channel the quoted price is roughly \$25,000 in singles. Clearly the scan converter is much more suitable for the application at hand. Still it is approximately six times larger than required and dissipates more than six times the power allocated. While its cost is quite reasonable for the performance offered, it is still more expensive than desired. Table II compares both the scan converter and a transient data recorder utilizing the parallel converter previously discussed. Certainly there is other equipment which could be discussed. The two transient data recorders chosen are considered to be representative.

In general, Table II suggests that even the unconventional techniques available today are too large, consume too much power, and in general fall short of the conversion and/or storage requirements. In both cases considered, most of the power and volume is associated with the converter section as well as the conversion performance.

The principle reason that power is high, volume large, and performance stretched to the limit is that data is being converted at extremely high rates. An approach which minimizes high rate data handling may be expected to minimize size and power.

THE SELECTED APPROACH

With the goal in mind of minimizing size and power, let us review Figure 2. The filter is passive and dissipates little power. The sample/hold circuitry is generally low power and small. The next step

(conversion) is the problem. The link between sample/hold and conversion is an obvious place for improvement. Data traversing this link is in sampled analog form as shown in Figure 4. It resembles an irregular staircase comprised of uniform width samples. If a device could be found that would accept data in this form, store it briefly, then play it back at a sufficiently slow rate, the remainder of the circuitry could be dramatically simplified.

Generally, this device is referred to as an analog shift register operated in fast (input)/slow (output) mode. It is located between the sample/hold and the converter as shown in Figure 5. It must be able to accept sampled, analog data at varying rates up to 500 Msamples/sec, store at least 1000 samples and then output the data at a rate \leq 1 Msample/sec with less than 1% total distortion.

ANALOG SHIFT REGISTER ALTERNATIVES

Two candidate analog shift registers were considered: the bucket brigade device (BBD) and the charge coupled device (CCD).

At the time of the selection, a 10-cell BBD with JFET switching between capacitor cells was being operated at 50 Msamples/sec, with a cell transfer efficiency of 97%. A 160 cell device was planned. If the 160-cell BBD was operated in the same manner as the 10-cell BBD, ten parallel channels would yield 1600 sample storage loadable at 500 Msamples/sec. If the cell to cell transfer efficiency remained at 97%, then the 160-cell transfer efficiency would be 0.97^{160} or 0.0076. Then less than 1% of the input signal would reach the output. This situation would put extreme demands on dynamic range and require involved data reduction procedures.

Another device considered was the peristaltic charge coupled device (PCCD)⁴. A 128-cell device had been operated at 100 MHz with transfer efficiency exceeding 0.9999. Eight PCCD's in parallel would provide storage for 1024 samples loadable at ranges up to 800 Msamples/sec. Transfer efficiency for 128 cells would be 0.9999^{128} or .987 nearly full signal.

For these and other performance considerations, the PCCD was chosen over the BBD to implement the scheme shown in Figure 5. Since the PCCD was not commercially available and the developer was not interested in working on the system under consideration, a custom PCCD was developed for this system by Rockwell International under subcontract to GARD, INC. and is the subject of another paper⁵.

The remainder of the paper relates how the PCCD was integrated with appropriate support elements to build a system complying with the stated requirements.

SYSTEM CONFIGURATION

The configuration of the system is shown in the block diagram of Figure 6. The major areas of the Transient data recorder are the filter, Sample/Hold, Analog Shift Register, Analog to Digital Converter, memory and the control logic. Special attention is given to the integration of the ASR and its peripheral equipment, timing and operation requirements, and packaging.

A filter is included in this system, as in most data acquisition systems, to limit the bandwidth of the processed signal to less than half the sampling frequency in order to eliminate frequency folding, and to reduce unwanted noise. Since eight sampling frequencies are used eight filters are required. The filters are plugable units with the capability of having any three in the system at one time. Status register control determines which will be selected. Due to the high sampling rates of this system, special filters had to be developed.

The sampling rates required by this system are beyond available state-of-the-art sample/hold and A/D conversion systems. For this reason, a sample and shift method was devised that provides time expansion of the sampling which permits the A/D conversion to be done at a much slower rate. A CCD analog shift register is operated as fast input/slow output temporary storage. The CCD used in this system is a 128 cell, 4-phase peristaltic device. To satisfy both the sampling frequency of 500 MHz and storage capacity of the system, eight sample/hold/CCD combinations were operated in

parallel. This provides a 1024 word storage capability and requires that the CCD's need operate only at 62.5 MHz at the fastest sampling rate.

The sample/hold circuitry is a conventional voltage sampling design with a linear switch and a hold capacitor but because of the frequency of operation, special design considerations had to be made. The eight S/H's are operated in sequence. However, to eliminate distortion caused by the operation of other S/H, only one S/H gate is permitted to start sampling at any given time.

After 1024 samples have been taken and temporarily stored in the CCD analog shift registers, the CCD's are then read out at a slower rate, multiplexed, and sent to the A/D in the proper sequence. A slow output rate of 100 KHz is obtainable with the CCD's used. The composite rate out of the multiplexer is 800 KHz requiring an A/D with a conversion time of 1.25 usec or less. There are a number of A/D converters in the 1 usec to 800 nsec range that are economically priced and small in size. The particular A/D used in this application is an 800 nsec conversion time device. The relatively slow conversion rates of the A/D also permits use of standard "off-the-shelf" MOS, bipolar or CMOS/SOS (when available) memory IC's to be used for system storage.

The system is remotely operated with all external commands stored in non-volatile internal status registers which in turn control all features of the recorder, including the sampling rate, which varies from 500 MHz to 2.5 MHz, the filter selection, and the offset. The operation sequence from sampling of the incoming signal through A/D conversion and storing of digital information in the memory is all controlled internally. The system can operate either in the normal record mode as described above or in the self-check or function check mode. The function check is an internally generated transient pulse that checks the operation of the system. The trigger commands which start a recording cycle can be generated externally or internally. The trigger commands consist of ARM, which enables all circuits, START, which begins the operation of circuits

that have some finite warm-up time but that require sufficient power to warrant limited use (e.g., the CCD drivers), and TRIGGER, which starts the record cycle.

ASR INTEGRATION

The mode of operation of the shift register in the system (i.e., fast input/slow output) indicates that the most difficult interfacing is involved with the input of the CCD and the peripheral circuitry that must operate at the fast frequency. As was intended, the slow output frequency tends to make the interfacing of the output an easier task. Of special concern here is interfacing of the CCD with the Sample/Hold circuitry, the input structure and the phase drivers.

When the sampling gates are off, they must present a high impedance to the hold capacitor to prevent the stored charge from dissipating. In this case due to the high frequency of operation the hold capacitor must be small requiring a very high hold impedance to prevent any leakage. The hold capacitance for the S/H in this system is the input gate capacitance of the CCD. This requires special care in processing of the CCD to insure that the input capacitance is of a small value and constant from CCD to CCD in order to match all eight CCD's. It further means that the input gate is terminated in a high impedance which makes it susceptible to system noise. Coupling within the CCD must be reduced as low as possible to prevent phase drive signal noise from being coupled to the input.

The input of the CCD is a critical point of this system. There are tight specifications on input linearity, accuracy, thermal stability, and dynamic range. Such things as linearity and accuracy cannot easily be compensated for within the system. The high frequency of operation and the range of frequencies involved put further restrictions on the input. The use of 8 CCD's requires that all parameters be closely matched in performance. The CCD input structures considered for this application were gated charge, gated impulse method, and Tompsett type inputs. The gated charge method controls a barrier under an input gate with the input signal. This allows charge to flow over the barrier in amounts

proportional to the input signal. This method was discarded because of its relatively poor linearity and thermal stability characteristics. The gated impulse method allows charge to flow for a specific length of time which is dependent upon a pulse width. This method was not used because of the difficulty in accurately controlling pulse widths at these frequencies. The input selected was a 3 gate Tompsett type input. The primary reasons for selecting this type were its improved linearity and thermal stability over the gated charge method. The timing diagram for the selected input is shown in Figure 7. The input signal is applied to gate 2 which controls the height of a barrier. Gate 3 is biased to a fixed well level. Both gate 1 and gate 3 are heavily bypassed to provide isolation for the high impedance of gate 2 from the possible interference from the diffusion and phase drive signals. The gate 2 barrier provides a wall for the fixed well of gate 3 determining the size of the well. The input gate area is flooded with charge; the input diffusion is then shut off and excess charge backflows out of the gate area. This leaves only the well under gate 3 full of charge. The charge can then be transferred to the first transfer gate of the CCD. Since the barrier under gate 2 must always be low enough to pass sufficient charge, the dynamic range is reduced with this method. This can be compensated for by enlarging the area under gate 3. Care must be taken in the design of the input to insure that the sufficient time is available for charge fill and backflow.

The CCD used in this application is a 128 cell, four phase peristaltic device which has been operated successfully at 80 MHz. The drive gate capacitance is approximately 25 pf and the voltage swing on the drive gates is approximately 15 volts. The ideal wave shape for a drive gate is trapezoidal with some finite rise and fall time, since it functions as a push clock (i.e., pushing charge in front of it). At the fast frequency of operation of 62.5 MHz, the rise and fall times are limited to 5 to 8 nsec. This rise time is held through all operating frequencies. Drivers with these characteristics are not readily available, so they were fabricated from discrete components. Of prime concern was

the power dissipation of the drivers. Both power supply requirements and thermal energy dissipation became a problem if the drivers were allowed to operate for an extended period. For this reason, the START command was incorporated into the system. The CCD does have some warm up time required because thermal filling will saturate the cells when it is not in operation. The START command is programmed to occur 50 to 100 μ sec prior to the start of recording which sufficiently clears all charge from the CCD's but does not create a power problem. Sufficient filter capacitance was included in the driver to supply power for the limited operation time. This eliminates restrictions put on the system by power supply response times.

The output of each CCD is fed to an amplifier with offset and gain control. These controls are required to provide adjustments for matching of the eight CCD's. Gain is required to increase the signal level to accommodate A/D input levels. Each CCD amplifier is then fed to a multiplexer which recombines the eight parallel paths back to one sequential data path.

TIMING AND OPERATION

The timing for the CCD phase drivers, the S/H drivers, the CCD input diffusion, the CCD output reset, and the CCD output multiplexer is all controlled by a common eight phase generator. At the highest frequency, a sampling aperture time of +50 picoseconds must be maintained to meet the system specifications. This made it necessary to use extreme care in the selection of components for and the layout of the timing circuitry. Further timing restraints were placed on the system by the fact that the S/H design, when optimized for the highest frequency, would not operate satisfactorily over the full range of sampling rates. The solution was to maintain the S/H at a higher frequency for the lower operating frequencies of the CCD's (see Figure 8). At the lower sampling rates multiple samples and multiple input cycles are being performed during one CCD phase drive cycle but only one is present when the CCD input transfer gate is ready to accept a sample. This tightens the timing constraints of the slower sampling rates which would normally be much less critical than the upper

frequencies.

The operational sequence of the system is controlled by a 1024 counter synchronized with the eight phase generator. When a START command is received from external control, the appropriate sample rate clock is gated to the eight phase generator which provides drive to the CCD's and S/H. Upon receipt of a TRIGGER the 1024 counter is set to zero and enabled. The CCD's are loaded in sequence until the 1024 counter indicates that each has received 128 samples. The clock frequency is then synchronously changed to a slower read out frequency which also controls the multiplexer (thru the eight phase generator), the A/D converter and the memory. The CCD data is read out at the slower rate, multiplexed and sent to the A/D in the proper sequence.

A slow output frequency of 100 KHz is attainable without significant thermal well filling. With eight CCD's in parallel, the composite output frequency from the multiplexer is 800 KHz. At this frequency both the A/D converter and memory are economical, small in size, and easy to control.

PACKAGING

The TDR is packaged in an enclosed module that is 29 in. long x 7 in. high by 1.6 in. wide. The overall layout is shown in Figure 9. The high frequency of operation, the timing constraints and a few special interrelationships between components (such as the CCD input gate acting as the hold capacitance for the S/H) dictated that all components in the sample and shift assembly had to have as little distance between them as possible. The solution found to this was a three layer arrangement. The eight S/H circuits were arranged symmetrically around the incoming data at the center of the top board. The timing circuitry and CCD peripheral circuitry was arranged symmetrically around the eight phase generator on the bottom board. The eight CCD's, their bias networks and output amplifiers were arranged on eight small cards perpendicular to the main cards. The eight cards were so arranged that the CCD input gate was at the top of the CCD card directly below its respective S/H gate. The bottom of the CCD card was then adjacent to its peripheral circuitry. The S/H timing

and drive signals from the lower board were transferred across the CCD board on micro-strip. The advantage of modular CCD boards is that since all adjustments for matching of the eight CCD's are on these boards, the CCD's can be matched prior to installation in the system and replacements of CCD's can be accomplished without modification to the larger boards.

Because the module is closed, the thermal load becomes significant. The most heat-sensitive component is the CCD, since at higher temperatures thermal well filling is increased, limiting the slow read out frequency. Most of the heat is generated in the timing and CCD peripheral circuitry. Because of the close proximity of these circuits, special precautions had to be taken. Heat sinks are mounted on the side of the module closest to the heat generating boards. Air at a rate of approximately 50 CFM will be passed over these fins. Thin silicon rubber sheets are placed between the boards and the module walls to increase conduction. Heat reflectors are used between the timing and CCD peripheral board and the CCD's. This reflects the heat back to the heat generating board and out to the heat fins. In a less hostile environment, the module could be opened allowing for convection or air flow thru the module. This would eliminate the need for the heat sinks, silicon rubber, and reflectors described above.

RESULTS AND CONCLUSIONS

A system breadboard has been built and operated. Testing has indicated that the CCD will not operate in the intended transient radiation environment. A redesign is presently being done on the CCD to incorporate radiation hardness. Calculation on the proposed design indicate that the new devices will be able to withstand 50 rads gamma. The proposed design will include a differential channel along with thinning techniques and selection of materials. The differential channel will help compensate for thermal and noise effects in the system as well as well filling due to radiation.

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5. Y. T. Chan, "Extremely High Speed CCD Analog Delay Line", International Conference on the Application of CCD's, October, 1975.
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TABLE I
TARGET SPECIFICATION

Data Conversion	
Sampling Frequencies (MHz)	500, 250, 100, 50, 25, 10, 5, 2.5
Input Filter Freq., 3 db (MHz)	100, 50, 20, 10, 5, 2, 1, .5
Aperature	± 50 ps
Resolution	6 bits
Accuracy	1%; 2% on system
Storage Capacity	1000 samples
Triggers	Internal and external
Size	7" x 2" x 29" (406 in ³)
Power Dissipation	40 watts
Environment (Operational)	
Radiation (gamma)	10^7 rads/sec 10 rad total gamma dose
(neutron)	10^7 neutrons cm ²
Shock	30g, 11 m sec in each direction
Pressure	sea level to 10,000 ft.
Humidity	93 \pm 5 per cent
Temperature	+10°F to 130°F
DIP	2 amps sheet current, to 100 MHz

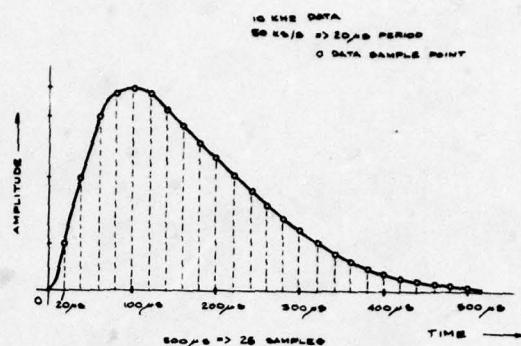


Figure 1. Sampling of Typical Pulse Data



Figure 2. Conventional Transient Data Recorder

Table II
TRANSIENT DATA RECORDER COMPARISON

	Parallel Converter	Scan Converter	Requirement
Maximum signal bandwidth (MHz) (5:1 quantizing ratio)	40	1000 high level 500 low level	100
Maximum sampling rate (# samples/sec)	200	100,000	500
Resolution (bits)	6	9	6
Storage (samples)	1000 or more	500	1000
Volume (in. ³)	4000	2500	400
Power dissipation (watts)	220 est'd	240	40
Cost (\$K) Singles 32	80 est'd 50 est'd	25K 16K	10

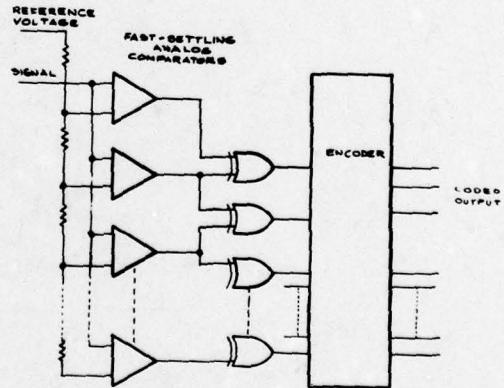


Figure 3. Typical Parallel Converter

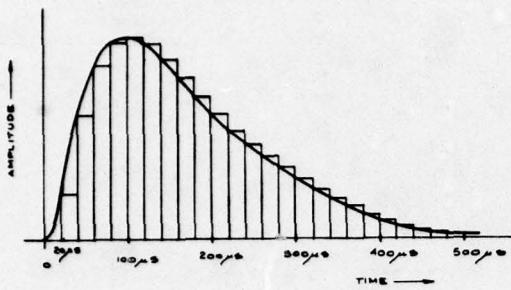


Figure 4. Analog Samples of Pulse Data



Figure 5. ASR Transient Data Recorder

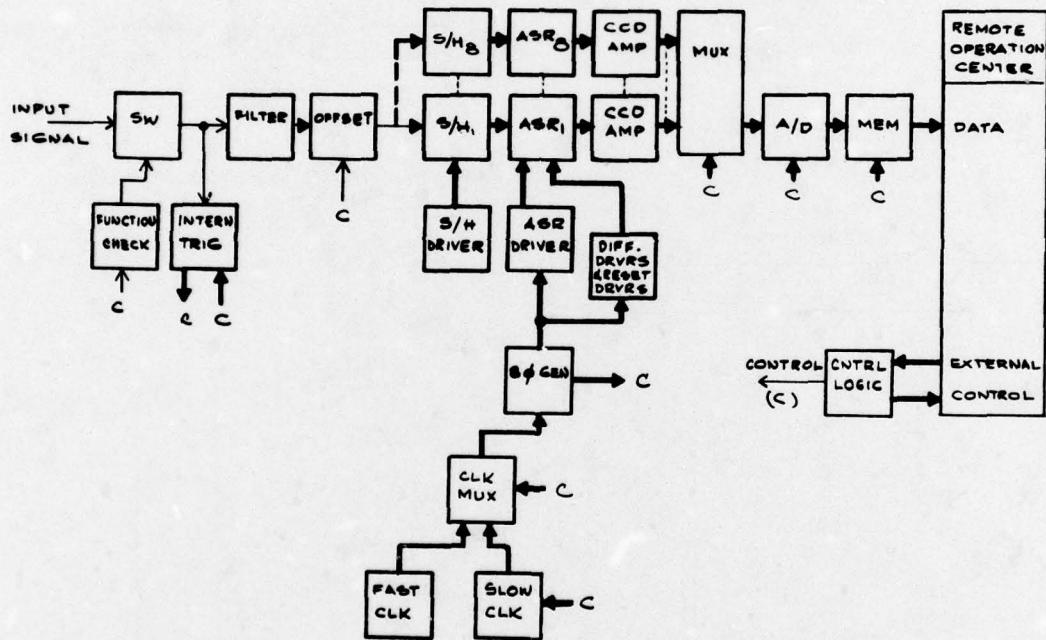


Figure 6. Transient Data Recorder Block Diagram

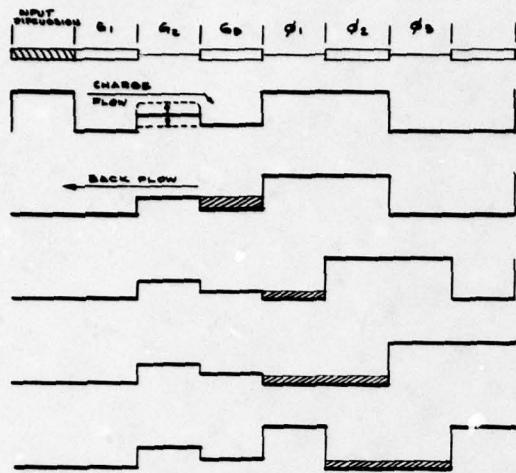


Figure 7. CCD Input Timing

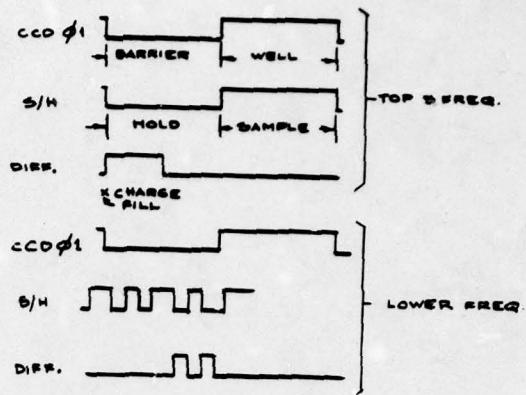


Figure 8. Sample and Shift Timing

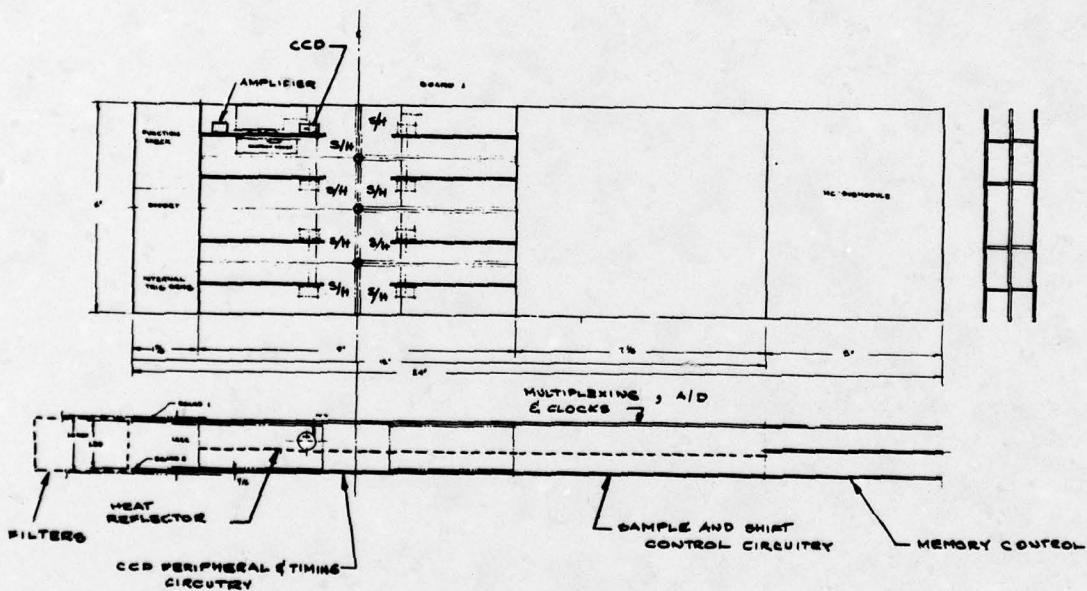


Figure 9. Transient Data Recorder Assembly

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INTERNATIONAL
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ON THE
APPLICATION OF
CHARGE-COUPLED
DEVICES

